Analog Integrated Circuits and Signal Processing, 36, 263–266, 2003

A Low-Noise, High-Gain Single-Ended Input Double-Balanced Mixer

JIN-YOUNG CHOI,[1,*] AND SANG-GUG LEE[2]

[1] *School of Electrical, Electronic and Computer Engineering, Hongik University, Jochiwon, Yongi Gun, Chungnam, 339-701, South Korea*
[2] *School of Engineering, Information and Communications University, 58-4, Hwaam-dong, Yusong-gu, Daejon, 305-348, South Korea*
E-mail: jychoi@hongik.ac.kr; sglee@icu.ac.kr

Received 4 January, 2003; Accepted 6 March, 2003

Abstract. A noble single-ended input, double-balanced mixer topology is proposed. The mixer adopts a transconductance stage that amplifies the input and then converts it into differential currents leading to overall performance advantage compared to prior CG(common-gate)-CS(common-source)-based transconductance-stage mixer topologies without requiring additional power dissipation or extra transistor. The key specifications are compared with those of reported similar topologies, based on simulations.

Key Words: mixer, single-ended input, double-balanced, MOSFET mixer

1. Introduction

The super-heterodyne receiver has been most widely used for modern radio communication system. The mixer is a key functional block in it, which converts the RF input signal into IF. With down-conversion mixer, often the double-balanced topology with differential input is preferred for LO suppression at the output. In this case, due to the single-ended configuration of the image rejection filter, single-to-differential conversion is required prior to the mixer. Therefore, a double-balanced mixer with a transconductance stage that incorporates single-to-differential conversion is desirable.

The MICROMIXER [1] has been introduced as a highly linear single-ended input double-balanced mixer. Figure 1 shows the CMOS version of MICROMIXER. In Fig. 1, M_3 is the common-gate transistor providing non-inverted signal to the switching stage (M_5, M_6, M_7, M_8), while M_2 and M_4 compose a cascode topology generating inverted signal. M_1 is added for the symmetric biasing of the transconductance stage. A wideband matching can be achieved with MICROMIXER by controlling the transconductance of M_1 and M_3. Various variants of input matching schemes are proposed in [1]. The MICROMIXER can provide unlimited input capacity due to the gain expansion available in class-AB operation of the common-gate and cascode stages, which leads to high linearity. However, the MICROMIXER suffers from the low conversion gain as well as poor noise performance. The resistive termination at the input by the diode connected transistor M_1 degrades the gain and noise performance. The unity current gain of the common-gate transconductance stage is another source for the noise and gain degradation. With common-gate stage, the mixer output noise current shows up directly at the input without suppression. Understanding the mixer power gain as a combined effect of current and voltage gain, the unity current gain of the common-gate stage affects negatively as well. The addition of resistive components at the input of the MICROMIXER, for the wideband matching purposes, can also degrade the gain and noise of the mixer considerably. In Fig. 1, Z_M represents the circuit components for a possible impedance matching.

Piazza [2] proposed a modification of MICROMIXER, from the schematic shown in Fig. 1, by opening the diode connection in M_1 and connecting the gate of M_1 to the gate of M_{B1}. In the modified version, the original diode connected transistor M_1 is converted into a current source such that the noise and gain characteristics of the mixer gets improved considerably. In spite of the good linearity and reasonable noise and gain performances, however, depending on the application, the noise and gain characteristics of Piazza's

*Corresponding author.

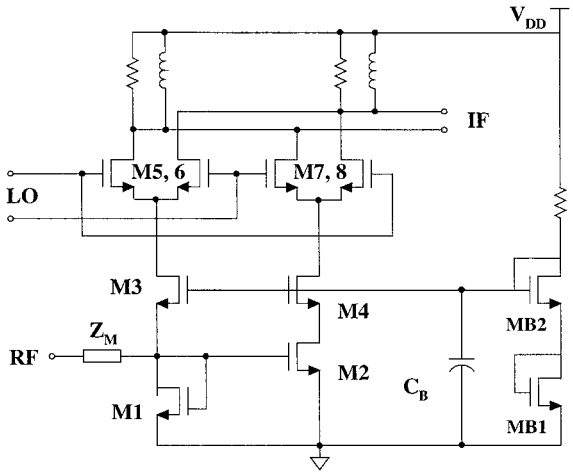


Fig. 1. A CMOS-version MICROMIXER schematic.

topology might not be satisfactory due to the common-gate transconductance stage.

2. Proposed Topology

Figure 2 shows another modification of the MICROMIXER proposed by this work to improve the conversion gain and noise performance. In Fig. 2, the diode connected transistor M_1 of the MICROMIXER is converted into a common-source stage such that M_1 provides current gain to the common-gate transistor M_3. In addition, the common-source transistor M_1 suppresses the noise current at the input, which comes from the output port of the mixer, leading to lower mixer noise figure. Note that the improvement in conversion gain and noise performance comes with no additional power dissipation or extra transistor. The common-source input configuration of the proposed mixer allows reactive gain and noise matching [3] without requiring additional components, for example, using the bond wires of the package, which are represented as L_G and L_S in Fig. 2. The input impedance matching through L_G and L_S provides additional voltage gain from the input to the gate of M_1, by the series resonance of the inductors and the gate-source capacitance of M_1. With the previous topologies, the g_m value of M_3 (and M_1 as well in MICROMIXER) can be restricted by the input matching requirements, but the proposed topology obviates the requirements. In Fig. 2, the biasing circuit guarantees the same drain current through transistors M_1 and M_2 if the gate-drain voltages of M_3 and M_4 are the same as that of M_{B2}, which is zero.

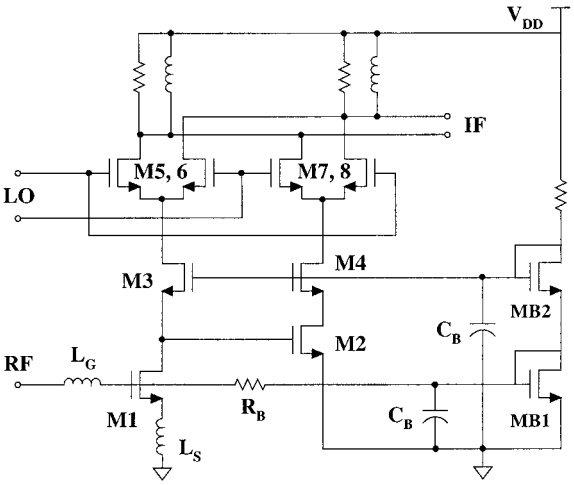


Fig. 2. The proposed mixer schematic.

3. Performance Comparison

The performance of the proposed mixer is evaluated and compared with prior topologies [1, 2] based on 0.35 μm CMOS technology for 2.4 GHz band. The simulation used calibrated (measurement based) transistor and passive component models including bond-pad. Table 1 summarizes simulation results of three down-conversion mixers. The simulation used $f_{\mathrm{RF}} = 2.4$ GHz, $f_{\mathrm{IF}} = 200$ MHz, $V_{\mathrm{DD}} = 3$ V, and $I_{\mathrm{DD}} = 4.9$ mA. For all three mixers, the size of transistors for M_1–M_4 are 400 μm and M_5–M_8 300 μm. The DC bias conditions are the same for all three mixers. The outputs are resistively loaded and the high value inductors are added to bypass the DC voltage drop across the resistors. In Table 1, the input matching of the proposed mixer is realized following the simultaneous gain and noise matching technique using bond wire inductors [3], while with the other two, the input matchings are done either by a series resistor or L-C combination. The two different matchings are tried on the previous topologies considering the performance dependencies on matching circuit. As can be seen in Table 1, compared to the previous topologies, the proposed topology shows clear advantage in conversion gain and noise figure, and inferior linearity. In order to compare the overall performance of the mixers, the last row in Table 1 shows a performance parameter defined as [conversion

Table 1. The mixer performance comparison: $f_{RF} = 2.4$ GHz, $f_{IF} = 200$ MHz, $V_{DD} = 3$ V, $I_{DD} = 4.9$ mA.

	MICROMIXER [1]		Modified MICROMIXER [2]		
Specification	Resistive matching	Reactive matching	Resistive matching	Reactive matching	Proposed mixer
Conversion gain	−8.6 (dB)	−4.0 (dB)	−4.6 (dB)	−1.1 (dB)	5.4 (dB)
Noise figure	18.9 (dB)	14.3 (dB)	15.9 (dB)	12.0 (dB)	8.1 (dB)
Input IP3	7.8 (dBm)	6.6 (dBm)	9.5 (dBm)	7.4 (dBm)	−2.3 (dBm)
CG − NF + IP3	−19.7	−11.7	−11	−5.7	−5

gain − noise figure + input third-order intercept point]. The simulation results in Table 1 do not guarantee the optimum performance of each topology, however, it provides the glimpse of the performance trends. It can be said that the proposed topology can certainly provide better conversion gain and noise figure, and yet, the overall performance is better or at least comparable to the previous CG(common-gate)-CS(common-source)-based transconductance-stage mixer topologies, without requiring additional external components and power dissipation.

In the proposed mixer, there is inherent voltage amplification between the input terminal and the gate node of M_1 under matched condition, which can be harmful to the linearity. From Fig. 2, the amount of voltage amplification between the input and the gate of M_1 is equal to the quality factor Q_{in}, which is given by [3]

$$Q_{in} = \frac{1}{\omega_0 C_{gs}(R_S + \omega_T L_S)} \tag{1}$$

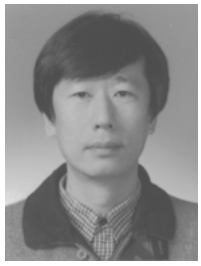
where R_s is the input source resistance, C_{gs} the gate-to-source capacitance of M_1, ω_0 and ω_T the operating frequency and the transistor cutoff frequency, respectively. From the Eq. (1), it is clear that Q_{in} can be quite large if C_{gs} is small. This indicates that if the input transistor size is small in the proposed mixer, the voltage amplification can be large, leading to poor linearity. With larger transistors, the voltage amplification at the input can be reduced to improve the linearity. However, the overall conversion gain of the mixer stays nearly the same as the voltage amplification and transistor g_m compensate with each other in the L_G, M_1, and L_S combination [3]. This means that, for a given current density, the linearity and noise figure of the proposed mixer tends to improve by increasing the transistor size, which increases the power dissipation. From Eq. (1), it can also be expected that the voltage amplification at the gate of M_1 can be quite large at low RF frequencies, leading to poor linearity. This indicates that the proposed mixer topology may require very large size transistors for low frequency application, a possible disadvantage. Therefore it can be said that the proposed mixer is more suitable for high frequency applications.

4. Conclusions

A noble single-ended input, double-balanced mixer topology is proposed. The proposed topology adopts a common-source stage in front of the conventional CG-CS transconductance stage, which leads to good conversion gain and noise performances, without requiring extra components or power dissipation. The overall performance of proposed mixer is compared with previously reported similar topologies through simulation based on a 0.35 μm CMOS technology. The proposed topology is shown to provide better overall performance. The trade-off between the power dissipation and linearity/noise performance of the proposed mixer is also discussed.

References

1. B. Gilbert, "The MICROMIXER: A highly linear variant of the Gilbert mixer using a bisymmetric class AB input stage." *IEEE J. Solid-State Circuits*, vol. 32, pp. 1412–1423, 1997.
2. F. Piazza and Q. Huang, "A high linearity, single-ended input double-balanced mixer in 0.25 μm CMOS." in *Proc. 24th European Solid-State Circuits Conference*, 1998, pp. 60–63.
3. T.H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press: New York, 1998.



Jin-Young Choi was born in Seoul, Korea in 1956. He received the B.S. degree in electrical engineering from the Seoul National University, Korea, in 1979, and the M.S. and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1986 and 1991, respectively. His doctorial research was in the area of thin-film SOI MOSFET device modeling. In 1991, he joined Samsung Electronics Memory Division, Korea, where he was engaged in high-speed SRAM development. In 1992, he moved to the Hongik University, Jochiwon, Korea, where he is now an associate professor. His recent research interests include the high-frequency modeling of CMOS devices, CMOS RF circuit design, and analysis & design for ESD protection.

Sang-Gug Lee was born in Gyungnam, Korea in 1958. He received the B.S. degree in electronic engineering from the Gyungbook National University, Korea, in 1981, and the M.S. and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1989 and 1992, respectively. In 1992, he joined Harris Semiconductor, Melbourne, Florida, USA, where he was engaged in silicon-based RF IC designs. From 1995 to 1998, he was with Handong University, Pohang, Korea, as an assistant professor in the school of computer and electrical engineering. Since 1998, he is with Information and Communications University, Daejon, Korea, where he is now an associate professor. His research interests include the silicon technology-based (BJT, BiCMOS, CMOS, and SiGe BICMOS) RF IC designs such as LNA, mixer, oscillator, power amp, etc. He is also active in the high-speed IC designs for the optical communication such as the TIA, driver amp, limiting amp, CDR, mux/demux, etc.