Design of Full Band UWB Common-Gate LNA

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***Abstract*—A two-stage, common-gate in cascade with cascode, ultra wideband low noise amplifier (LNA) topology is proposed for 3.1 to 10.5 GHz full band application. The common-gate first stage is adopted and optimized for low noise figure (NF) at high frequencies. The LNA implemented in 0.18 μm CMOS shows more than 10 dB input return loss, maximum gain of 16 dB, and NF of 3.8$\sim$4.0 dB over the full frequency band while dissipating 5.3 mA from 1.8 V supply.**

***Index Terms*—Common-gate, low noise amplifier (LNA), ultra wideband (UWB).**

I. Introduction

RECENTLY, the need for ultra wideband (UWB) circuits is in steady rise for high data rate and multi-band applications. A number of UWB low noise amplifiers (LNAs) for 3$\sim$5 GHz band (mandatory mode) have been reported with respectable performance in CMOS technology [2]. The UWB LNAs for full frequency band (3$\sim$10 GHz), for higher data rate, have also been reported based on CMOS technology. Most reported full band UWB LNAs are implemented as a common-source or cascode topology, each of which provides acceptable gain and input matching while dissipating rather low power. However, these common-source or cascode UWB LNAs tend to show unacceptably high noise figure (NF) at high frequencies (near 10 GHz) due to the strong cutoff frequency dependence [1]. This letter presents a two-stage, common-gate in cascade with cascode topology, UWB LNA which can provide nearly constant NF over the full frequency band of 3$\sim$10 GHz.

II. Circuit Design

The common-gate topology is well known for its constant wideband input impedance of $1/g_m$ where g_m is the transconductance of the transistor. However, with technology scaling, due to the increase in drain-source conductance, the input impedance of the common-gate stage tends to deviate from the ideal $1/g_m$ and shows stronger dependence on output loading, which makes the wideband matching difficult. However, as will be described later, the strong dependence on output loading can be used to satisfy the input matching and low NF simultaneously. Traditionally, the common-gate topology is known to have higher NF than that of the common-source or cascode. But, lately, with technology scaling, the common-gate topology is starting to be recognized as an alternative to the common-source or cascode for the LNA, especially at frequencies near 10 GHz or higher [3]. The purpose of this work is to design an optimized common-gate in cascade with cascode UWB LNA which shows UWB input matching and low/nearly-flat NF over the full frequency band of UWB system.

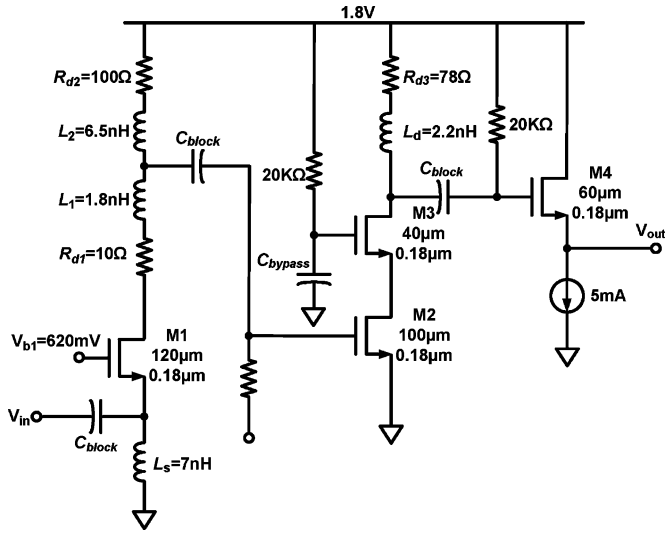

Fig. 1. Proposed schematic of the two-stage, common-gate in cascade with cascode, UWB LNA.

Fig. 1 shows the proposed LNA which consists of a common-gate first-stage, a cascode second-stage and a buffer. The buffer is added for measurement purposes only. From Fig. 1, the input impedance of common-gate topology can be given by

$$Z_{\rm in}(s) = (C_{gs1}\|L_s)\|\left\{\frac{1}{g_{m1}}\left[1+\frac{Z_{\rm Load}(s)}{r_{ds1}}\right]\right\} \qquad (1)$$

where g_{m1} and r_{ds1} are the transconductance and output resistance of the common-gate transistor, respectively, $Z_{\rm Load}$ the load impedance seen at the drain of the transistor M_1, C_{gs1} the parasitic capacitance of M_1, and L_s the RF choke. In (1), $Z_{\rm in}$ becomes a stronger function of $Z_{\rm Load}$ with technology scaling due to the reduction in r_{ds1}. From (1), at frequencies and for the values of C_{gs1} and L_s, the impedances presented by C_{gs1} and L_s are negligibly high. Therefore, $Z_{\rm in}$ can be matched to the source resistance R_S by satisfying the condition $1+Z_{\rm Load}/r_{ds1} = R_{Sgm1}$.

In this work the LNA is designed for $R_S = 50\ \Omega$, therefore, e.g., for $1/g_{m1} = 25\ \Omega$ which is the value chosen in this design, the 50 Ω input resistance can be obtained. The challenge is how

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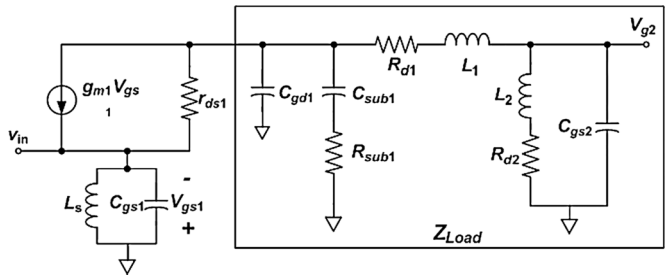

Fig. 2. Small-signal equivalent circuit for the common-gate stage including the load and the parasitic at the drain.

to maintain the condition of $Z_{\rm Load} = r_{ds1}$ over a wide range of frequencies. Fig. 2 shows the small-signal equivalent circuit for the common-gate stage including the load and the parasitic at the drain. In Fig. 2, C_{sub1} and R_{sub1} represent the drain to substrate parasitic of transistor M_1. In the proposed design, the condition for $Z_{\rm Load} = r_{ds1}$, is achieved by the multiple resonance. From Fig. 2, at low frequencies (near 3 GHz), the parallel combination of $C_{gs2}||L_2$ at the output and $C_{gs1}||L_S$ at the input are resonated simultaneously. The value of R_{d2} is adjusted for $Z_{\rm Load} = r_{ds1}$ at resonance where $R_{d1} - L_1$ presents negligibly low impedance, leading to 50 Ω impedance at the input. At high frequencies (near 10 GHz), the combination of C_{gd1}, C_{sub1}, L_1, and C_{gs2} presents second parallel resonance at the drain of M_1. At high frequencies, $R_{d2} - L_2$ can be considered open. Again, the value of R_{d1} can be adjusted for $Z_{\rm Load} = r_{ds1}$. At the second resonance, the voltage across C_{gs2} is delivered to the input of the cascode amplifier. Note that, due to C_{gs1}, the frequency of the second resonance seen from the input will be slightly down shifted. Therefore, by the proper adjustment of the two frequencies of resonance and the resistor size, input matching can be achieved over the full frequency band of interest. Due to the resonance based design at the low and high frequency bands, the common-gate stage gain in the mid-band can have a droop. As shown in Fig. 1, this mid-band gain reduction can be compensated by the cascade of a shunt-peaked cascode amplifier, which is the same as the stagger tuned method [6]. In the cascode amplifier, the value of the inductor L_{d2} is chosen to provide peak gain near the center of the pass-band leading to nearly flat overall wideband LNA gain.

In the proposed LNA architecture, the NF is dominated by the common-gate stage. From [4], the NF of a common-gate stage is given by

$$F = 1 + \left(\frac{\gamma}{\alpha}\right)\left(\frac{r_{ds}}{r_{ds} + R_{\rm Load}}\right) \tag{2}$$

where $\alpha = g_m/g_{do}$ is the ratio of the transistor transconductance to the channel conductance at zero $V_{\rm DS}$, γ the channel thermal noise coefficient, r_{ds} the drain-source resistance and $R_{\rm Load}$ the output load resistance. From (2), the NF is a function of r_{ds} and $R_{\rm Load}$. When $r_{ds} \gg R_{\rm Load}$, the NF of a common-gate topology is given by $F = 1 + \gamma$ (approximately 2.2 dB), which is considered as the minimum achievable value [5]. However, with technology scaling, the reduction in r_{ds} can lead to reduction in NF below $1+\gamma$ [4]. In the proposed common-gate topology, r_{ds} and $R_{\rm Load}$ are designed to be approximately the same over the frequency band of interest. Therefore, from (2), the NF of the proposed common-gate topology reduces to $F \approx 1 + \gamma/2$. In the proposed LNA, simulation shows nearly flat NF up to 12 GHz, which can be explained by the $Z_{\rm Load} \approx r_{ds}$. This is the advantageous NF characteristic of the common-gate topology, which is not feasible with cascode or common-source topology. Note that many of previously reported UWB LNAs adopt band-pass filters at the input, which lead to more than two inductors. Considering the limited quality factor of the inductors, especially the on-chip, the proposed LNA can provide additional NF advantage as it adopts only one inductor at the input.

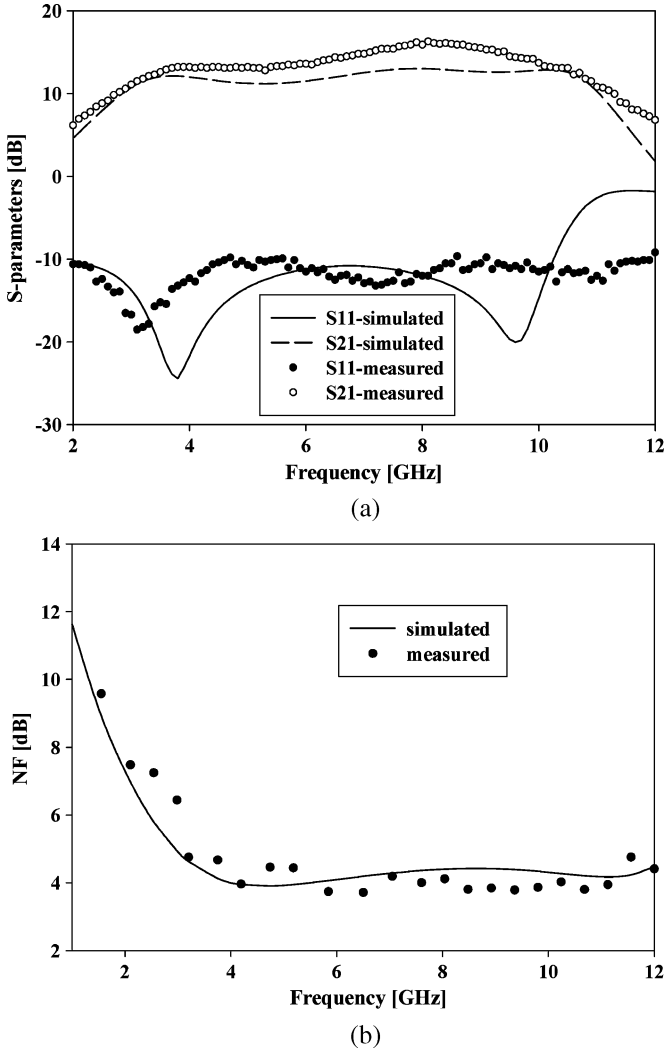

Fig. 3 Simulated and measured results of the proposed UWB LNA (a) S21 and S11 and (b) NF.

The proposed two-stage LNA is optimized for the full band 3.1$\sim$10.5 GHz UWB application and implemented in 0.18 μm CMOS technology. The selected 0.18 μm technology provided six metal layers and the on-chip inductors are implemented with top layer of 2 μm thickness without pattern ground shield. The LNA is designed to dissipate 5.3 mA from 1.8 V supply excluding buffer. Fig. 3(a) shows the simulated and measured gain and input matching characteristics. In Fig. 3(a), the measurement show more than 10 dB matching over 2$\sim$12 GHz band and flat gain response over 2.9$\sim$11 GHz band with maximum

TABLE I
COMPARISON OF WIDEBAND CMOS LNA PERFORMANCES: PUBLISHED AND THE PRESENT WORKS

Reference	Gain (dB)	Max. NF (dB)	BW (GHz)	S11 (dB)	PD (mW)	Topology	Technology
[1]	9.3	5.2*	2.4~9.5	< -9.9	9	LC-filter based	0.18 μm CMOS
[2]	9.8	3**	2~4.6	< -9	12.6	Feedback	0.18 μm CMOS
[7]	13	3.3	2~10	< -7	9.6	Feedback	0.18 μm SiGe BiCMOS
[8]	12.4	6.5	0.4~10	< -9	12	Common-gate	0.18 μm CMOS
[9]	9.3	5.5	2~11	< -10	17	Feedback	90nm Digital CMOS
[10]	8.5	5.3	1.3~10.7	< -10	4.5	Common-gate	0.18 μm CMOS
This work	**16**	**4.0**	**2.9~11**	**< -10**	**9.5**	**Common-gate**	**0.18 μm CMOS**

*: average NF in interest BW, **: NF at 4 GHz

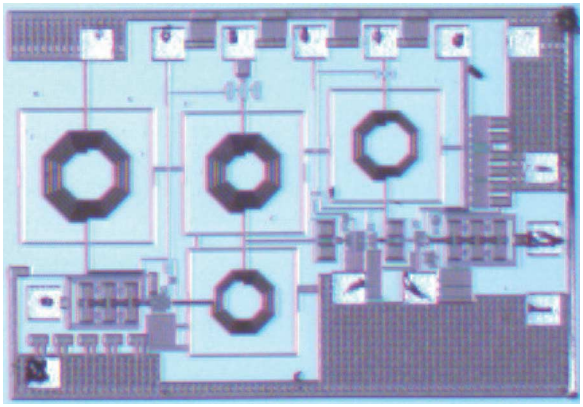

Fig. 4 Microphotograph of the proposed full band UWB LNA.

gain of 16 dB. The measurement results show reasonable agreement with simulations. Fig. 3(b) shows the simulated and measured NF characteristic. In Fig. 3(b), the measured NF range from 3.8 to 4.4 dB over the frequency band of 3 to 12 GHz. Again the measurement results show reasonably good agreement with simulation, and as expected, the NF stays flat up to 12.6 GHz which is different from that of the cascode topology. Fig. 4 shows the micrograph of the fabricated chip with the size of $1.2\times0.82\ \mu m^2$ (see Table I) [7]–[10].

III. CONCLUSION

A two-stage, common-gate/cascode UWB LNA that adopts a common-gate topology as a first stage is presented. The performance advantage of the common-gate topology with technology scaling for high frequency application is discussed and wideband design techniques for input matching and low NF are proposed. The wideband input matching of the common-gate topology is achieved by adopting dual parallel resonance at the output, and low/flat NF, especially at high frequencies, is achieved by presenting high impedance at the output. The proposed full band UWB LNA is implemented in 0.18 CMOS technology. Measurement shows higher than 10 dB matching at the input, maximum gain of 16 dB, and NF of 3.8∼4.0 dB over the full frequency band of UWB system (3.1∼10.6 GHz) while dissipating 5.3 mA from a 1.8 V supply.

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