

84 dB 5.2 mA digitally-controlled variable gain amplifier

H.-H. Nguyen, Q.-H. Duong and S.-G. Lee

A digitally-controlled topology that reduces power dissipation to half that of the conventional one while occupying smaller die area and obtaining higher linearity is presented. In the 0.13 μm CMOS process, the VGA occupies an active area of 0.46 mm^2 and dissipates an average current of 5.2 mA at 1.5 V. The gain-variation range is -32 to 52 dB with a gain error of less than ± 1 dB. The IIP3, P1dB, NF at 52 dB of gain, and 3 dB bandwidth are -37 to +13 dBm, -42 to -2 dBm, 6.2 dB and 200 MHz, respectively.

Introduction: The variable gain amplifier (VGA) plays an important role in maximising the dynamic range of wireless communication systems, medical equipment, hearing aids, disk drives etc. [1-3]. There are two possible approaches to realising the VGA: one is to build a digital VGA with discrete gain step controlled by digital signals [1], and the other is the analogue VGA with continuous gain variation over control voltage or current signals [2]. This Letter presents a new digital VGA topology which reduces power dissipation to half that of the conventional topology while occupying smaller chip size and featuring higher linearity.

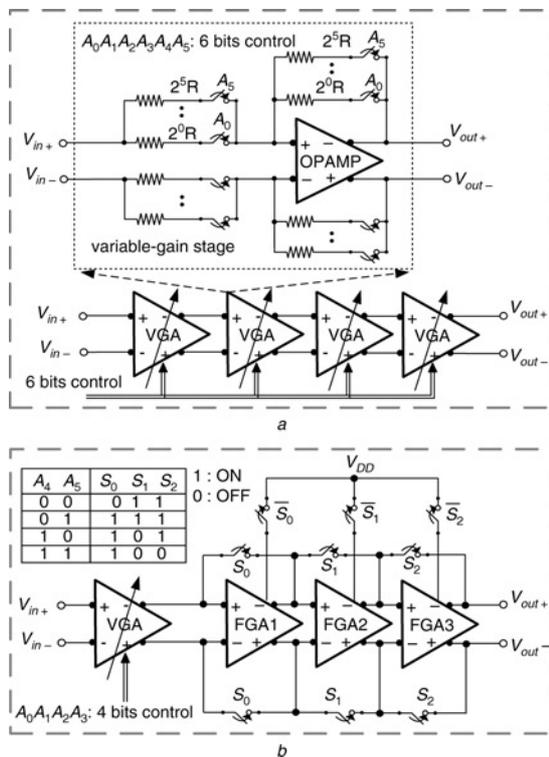


Fig. 1 Conventional and proposed VGA topologies
 a Conventional cascaded VGA topology
 b Proposed VGA topology

Proposed VGA topology: Fig. 1 shows the conventional and proposed digital VGA topologies. In Fig. 1a, the conventional VGA topology is composed of a series of variable-gain stages with resistor or capacitor switches [1]. Normally, conventional digital VGAs use a pseudo-exponential function expressed as $e^x \approx [(1+x)/(1-x)]^{1/2}$ for decibel-linear gain control characteristics, which is limited to less than 20 dB with linearity error of less than ± 1 dB [1]. Consequently, the VGA uses many gain stages to satisfy the required dynamic gain range as shown in Fig. 1a [1-3]. The use of many gain stages with a large number of switches and resistors as shown in Fig. 1a results in a big chip size or high cost. Note that, all gain stages in Fig. 1a stay ON during operation. However, the proposed topology in Fig. 1b uses only one variable-gain stage and three fixed-gain amplifiers (FGA1,2,3) and obtains the same gain range as that of the conventional topology while reducing power dissipation by half and occupying smaller chip size. In Fig. 1b, the gains of FGA1, FGA2 and FGA3 are

set at -21, 21, and 21 dB, respectively, and the gain-variation range of the variable-gain stage is controlled from -10 to 11 dB. The switches S_0 , S_1 , and S_2 are used for bypass or to power-down the desired FGAs. The proposed VGA topology in Fig. 1b uses a total of 6 bits for the control: 4 bits ($A_0A_1A_2A_3$) for the variable-gain stage and 2 bits (A_4A_5) for the switches $S_0S_1S_2$.

In Fig. 1b, for combinations of the variable-gain stage and FGA1,2,3, the overall gain of the VGA can vary from -32 to 52 dB as shown in Fig. 2a. For example, to obtain a gain range from -32 to -11 dB, the switches S_0 and S_{12} in Fig. 1b are opened and closed, respectively, so that FGA1 is turned ON while FGA2,3 are powered OFF. Similarly, the gain variation from 31 to 52 dB is achieved by turning ON FGA2,3 while FGA1 is OFF. Assuming each of the amplifier blocks in Fig. 1 uses the same op-amp block, which consumes a power of P_0 , then the power dissipations of the conventional topology is always $4P_0$ while the average power dissipation of the proposed topology is $2P_0$, as shown in Fig. 2b. Consequently, the proposed VGA topology offers 50% of power saving compared with the conventional one. Moreover, as shown in Fig. 1b, the proposed topology uses fewer switches and resistors, resulting in smaller chip size or lower cost.

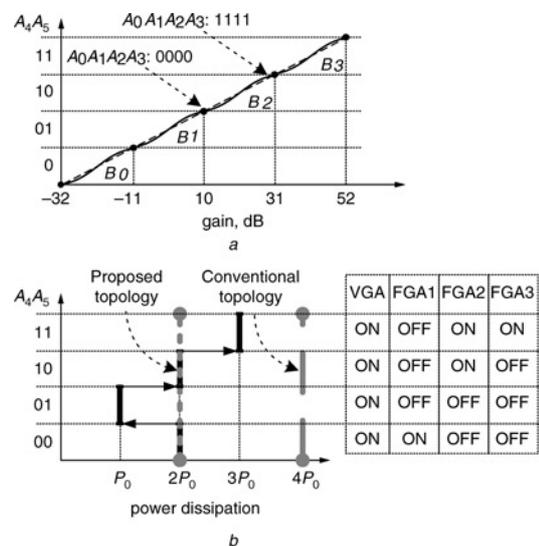


Fig. 2 Power dissipation comparison of proposed and conventional VGA topologies
 a Overall VGA gain against control bits
 b Power dissipation against control bits

Proposed schematic of VGA and FGA: The schematics of the proposed variable-gain stage and FGAs are shown in Fig. 3. In Fig. 3, the variable-gain stage is a differential amplifier with diode-connected loads. The common-mode feedback circuit (CMFB) stabilises the output DC voltages of the variable-gain stage. The gain of the variable-gain stage is given as

$$A_V = \sqrt{\frac{(W/L)_{input-pairs}}{(W/L)_{load-pairs}} \times \frac{I_{input-pairs}}{I_{load-pairs}}} \quad (1)$$

where $(W/L)_{input-pairs}$, $(W/L)_{load-pairs}$, $I_{input-pairs}$ and $I_{load-pairs}$ are the aspect ratios and bias currents of the input and load transistors as shown in Fig. 3, respectively. In a conventional VGA [2], the ratio $(W/L)_{input-pairs}/(W/L)_{load-pairs}$ is fixed and the gain is controlled by varying the bias current ratio $I_{input-pairs}/I_{load-pairs}$ such that the gain follows a pseudo-exponential function expressed as $e^x \approx [(1+x)/(1-x)]^{1/2}$ [2]. In this work, the gain of the amplifier in Fig. 3 is controlled by simultaneously varying the bias current ratio ($I_{input-pairs}/I_{load-pairs}$) and the transistor size ratio $(W/L)_{input-pairs}/(W/L)_{load-pairs}$. The ratios, $(W/L)_{input-pairs}/(W/L)_{load-pairs}$ and $I_{input-pairs}/I_{load-pairs}$, are controlled by 4 bits binary weighted transistor arrays A_0 , A_1 , A_2 and A_3 as shown in Fig. 3. The aspect ratios and bias currents as a function of the control

bits can be given as

$$(W/L)_{input-pairs} = (W/L)_1(2^0 A_0 + 2^1 A_1 + 2^2 A_2 + 2^3 A_3 + k) \quad (2)$$

$$(W/L)_{load-pairs} = (W/L)_2(2^0 \bar{A}_0 + 2^1 \bar{A}_1 + 2^2 \bar{A}_2 + 2^3 \bar{A}_3 + k) \quad (3)$$

$$I_{input-pairs} = I_{01}(2^0 A_0 + 2^1 A_1 + 2^2 A_2 + 2^3 A_3 + k) \quad (4)$$

$$I_{load-pairs} = I_{02}(2^0 \bar{A}_0 + 2^1 \bar{A}_1 + 2^2 \bar{A}_2 + 2^3 \bar{A}_3 + k) \quad (5)$$

where A_i is the digital control bit and k the constant for adjusting the gain range of the variable-gain stage. Therefore, the gain follows a squaring pseudo-exponential function given as $e^{2x} \simeq (1+x)/(1-x)$. Consequently, the proposed circuit can provide twice the gain-variation range compared to conventional one [2]. Moreover, in the conventional gain varying scheme that is applied to the conventional VGA cell [2], the gain is reduced by decreasing the bias current of the input pair. Hence, at low gains, the gate-source voltages (V_{GS}) of these input transistors decline and so does the amplifier linearity [3]. In Fig. 3, the sizes of the input/diode-connected transistors and their bias currents are controlled simultaneously in the same ratio. Therefore, the current densities of the input/diode-connected transistors stay constant with gain variation, which leads to significant improvement in linearity at low gains.

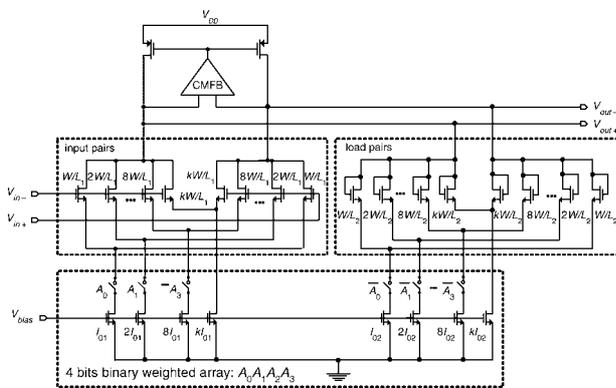


Fig. 3 Schematic of proposed variable-gain stage and FGAs

The FGA also uses the same differential amplifier with diode-connected loads, as shown in Fig. 3; however, since the gain of FGA is fixed, the transistor size and bias currents for FGAs are constant. The transistor size and bias currents are adjusted to offer the required fixed gains of 21 or -21 dB, respectively. The proposed VGA adopts highpass filters (HPF) in between FGAs and variable-gain stage to cancel the DC offset problems.

Measurement results: In the $0.13 \mu\text{m}$ CMOS process, the proposed VGA occupies an active area of 0.46 mm^2 and dissipates an average current of 5.2 mA at 1.5 V . Fig. 4 shows the measured gains and gain

errors against control words. In Fig. 4, the proposed VGA offers 84 dB of dynamic gain range (-32 to 52 dB) and the maximum gain error is less than $\pm 1 \text{ dB}$. The measured IIP3, P1dB, NF at 52 dB of gain, and 3 dB bandwidth are -37 to $+13 \text{ dBm}$, -42 to -2 dBm , 6.2 dB and 200 MHz , respectively.

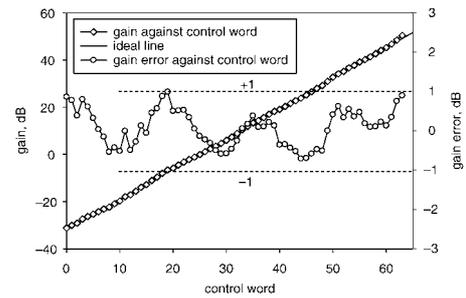


Fig. 4 Measured gains and gain error against control word

Conclusions: In this letter we have proposed a digitally-controlled VGA topology that reduces power dissipation to half that of the conventional one while occupying smaller die area and maintaining wide gain variation range as well as good linearity performance. The proposed VGA can be used in many low-power applications, such as medical equipment, telecommunication systems, hearing aids, disk drives etc.

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