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A 2.45 GHz CMOS up-conversion mixer design utilizing the current-reuse bleeding technique

J.-Y. CHOI†* and S.-G. LEE‡

A 2.45 GHz double-balanced modified Gilbert-type complementary metal-oxide-semiconductor (CMOS) up-conversion mixer design utilizing the current-reuse bleeding p-channel mos (PMOS) transistors is examined thoroughly based on simulations to demonstrate many advantages achievable when adopting the current-reuse bleeding technique in the mixer design. It is shown that the current-reuse bleeding technique certainly provides benefits in terms of gain, linearity and noise characteristics. In the mixer incorporating the current-reuse bleeding technique, the conversion gain improves monotonically with more bleeding. The linearity also improves with bleeding by a noticeable amount when the voltage headroom is not adequate. However, with excessive bleeding, linearity degrades by the current-limiting phenomena which defines the optimal bleeding ratio. Noise performance also improves monotonically with more bleeding. Of all the benefits provided, the improvement in noise performance seems most valuable. The measurement of the fabricated chip based on the standard 0.35 μm CMOS process supports the validity of the analysis. The measured mixer performance is quite excellent, and the measured characteristics are in close agreement with the simulations, which demonstrates the adequacy of the modelling approach based on the macro models for all the active and passive devices used in the design.

1. Introduction

The double-balanced Gilbert-type mixer topology is preferred in up-conversion mixer design since it suppresses the local oscillator (LO) signal at the output. Even though there have been many efforts to explain the operational mechanism involved and to improve the characteristics (Karanicolas 1996, MacEachern and Manku 1998, Lee and Choi 2000, Liu and Westerwick 2000), the operation of this important function block does not seem to be fully examined. Only a few successful CMOS design examples based on this topology have been reported at the frequency range above 2 GHz (Runge *et al*. 1999, Liu and Westerwick 2000), where more challenges are solicited for CMOS technology to prove its potential in higher frequency applications.

The double-balanced Gilbert-type CMOS mixer is basically composed of the input transconductance stage, the switching transistors, which operate in switching mode by differential LO signals to perform frequency conversion, and the mixer loads. In mixer design, the higher gain, higher linearity, lower noise and low power consumption are required, but it is not be easy to achieve them simultaneously.

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Higher gain and better linearity can be achieved by increasing the bias current through the transconductance stage (Fong and Meyer 1998, MacEachern and Manku 1998), but power consumption can be excessive. Furthermore, the larger current through the switching transistors can cause voltage headroom problems especially if resistive loads are used. Larger amount of current through the switching transistors also mandates a large LO drive, which is desirable for more ideal switching but troublesome in the CMOS technology, since it is not easy to get a large enough voltage swing at high LO frequency.

Better techniques to improve conversion gain have been introduced, where some sort of current bleeding techniques are utilized (MacEachern and Manku 1998, Lee and Choi 2000, Liu and Westerwick 2000). With the current bleeding technique, the bias current through the transconductance stage can be increased without increasing the current through the switching transistors. While not affecting the transconductance of the transconductance stage, the bleeding relaxes the voltage headroom problem, and allows smaller LO drive voltage applied to the switching transistors because of improved switching efficiency, which helps to improve the conversion gain.

The gain can be improved further by the current-reuse bleeding technique (Lee and Choi 2000), where the gates of the PMOS bleeding transistors are connected to the input together with the n-channel mos (NMOS) gates of the transconductance stage to enhance the transconductance of the transconductance stage. The PMOS transistors act not only as bleeding transistors but also as a part of input transconductance stage, and hence the bleeding current is effectively reused (see figure 1 in § 2).

In this paper, a 2.45 GHz double-balanced modified Gilbert-type CMOS up-conversion mixer design utilizing the current-reuse bleeding PMOS transistors is thoroughly examined based on simulation and measurement results, which may

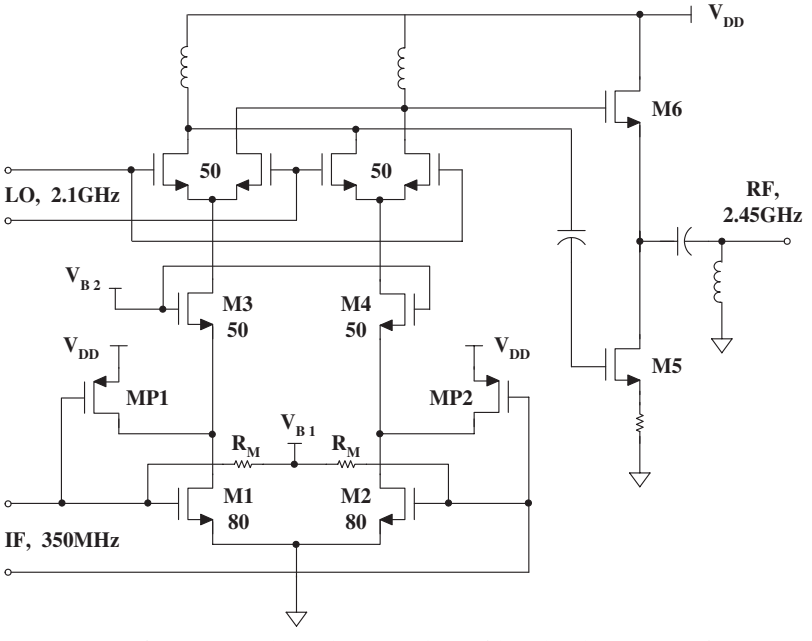

Figure 1. Proposed up-conversion mixer topology (bias circuits are not shown). Numbers shown beside the transistors indicate the number of 5 μm-width gate fingers.

provide design guidelines in applying this type of mixer both in up and down conversion.

In § 2, the idea behind the chosen mixer topology is explained in terms of characteristic improvements. In § 3, the characteristic changes in gain, linearity and other important behaviours as a function of the current-bleeding ratio are discussed. Modelling efforts to increase the accuracy of simulations are also introduced. In § 4, the measurement results of the chip fabricated utilizing 0.35 μm standard CMOS process are given to confirm the validity of the analysis. In § 5, the results are summarized briefly.

2. Mixer topology

Figure 1 shows the proposed double-balanced modified Gilbert-type CMOS up-conversion mixer. The cascode configuration of the transconductance stage is adopted to suppress the 2nd-order harmonic of the LO (2LO) signal at the mixer output since the higher output impedance of the transconductance stage tends to suppress the 2LO signal, as is explained in the following paragraph.

Figure 2 shows half of the double-balanced mixer schematic. In figure 2, Z_L is the load impedance of the mixer, M_2 and M_3 the switching transistors, and M_1 the transconductance amplifier. Assuming the amplitude of the LO signal is large enough, only one of the switching transistors are on for each half-cycle of the LO signal. The switching operation of the transistors generates 2LO frequency at the source and drain node of the switching transistors. During the 1st half-cycle, the transistor M_2 operates as a common-source amplifier with source degeneration. Therefore, the amplitude of the 2LO at the drain of M_2 is proportional to Z_L/Z_{SS}. With double-balanced mixer, the 2LO signal at the drain node of the switching transistor looks like the sum of the solid and dotted lines.

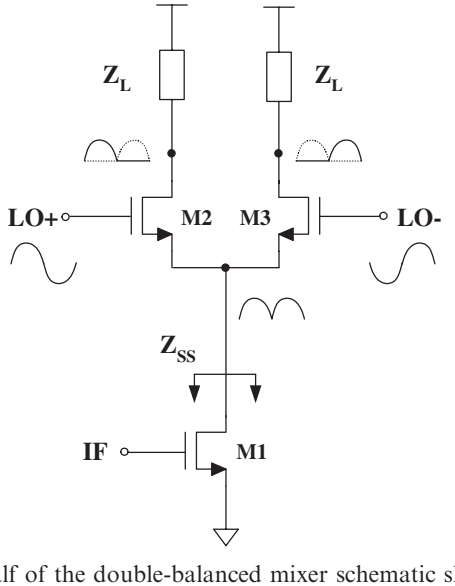

Figure 2. Half of the double-balanced mixer schematic shown with the LO signal distribution.

In mixers, especially the up-conversion mixer, the large amplitude of 2LO signals at the output node can be a problem as it can drive the switching transistors into the linear region of operation leading to the performance degradation. An effective way to reduce the 2LO at the output terminal of the mixer is to increase the output impedance (Z_{SS}) of the transconductance stage, for example, by adopting a cascode configuration. The amplitude of 2LO at the source of M_2 is about the same as that of the applied LO signal as it forms a source follower.

In figure 1, the IF input is resistively matched to the 200 Ω differential input at 350 MHz, which was chosen in accordance with the IF filter characteristic. Resistive matching was chosen since the reactive matching requires too large L or C for on-chip matching and also the noise performance is not critical in the up-conversion mixer specification. The mixer was assumed to be driven by differential LO signals of 2.1 GHz externally.

The source terminals of the transconductance stage are connected directly to the ground. The differential intermediate frequency (IF) drive allows class AB operation of the transconductance stage, which helps to achieve higher conversion gain and linearity (Fong *et al*. 1997). The on-chip inductors are used as loads to reduce headroom problems and to utilize the frequency tuning behaviour at the mixer output.

In figure 1, the PMOS transistors (M_{P1} and M_{P2}) are incorporated for the current-reuse bleeding (Lee and Choi 2000) to improve the conversion gain. In figure 1, the PMOS transistors can be biased separately and coupled capacitively with the NMOS transistors (M_1 and M_2). However, to simplify the biasing as well as to minimize the PMOS transistor size, the gates of the PMOS transistors are directly connected to the gates of the NMOS transistors. The current-reuse bleeding is also expected to improve the linearity since the effective dc current of the transconductance stage increases (Fong and Meyer 1998) because PMOS and NMOS transistor effectively form a single transistor.

In figure 1, the common-drain-common-source (CDCS) buffer balun stage, composed of M_5 and M_6, is adopted at the output stage to get the single-ended output, which is matched to the 50 Ω RF load at 2.45 GHz by the on-chip capacitor and bond wire.

The N-well accumulation-type MOS capacitors and the poly2–poly1 capacitors were used for on-chip coupling, bypass, and matching purpose, and the poly2 resistors were used for biasing.

3. Performance analysis

As mentioned in the introduction, several papers concerning the mixer topologies incorporating the current bleeding and/or current reusing technique have been reported (Karanicolas 1996, MacEachern and Manku 1998, Lee and Choi 2000, Liu and Westerwick 2000), but the results have not been analysed thoroughly. In this section, the proposed mixer performances are analysed thoroughly with the help of circuit simulations to characterize the benefits and drawbacks in adopting the current-reuse bleeding technique in mixer design.

Simulations on this work are based on the bsim3v3 model parameters of the standard 0.35 μm CMOS process. The width of transistor fingers was chosen as 5 μm to minimize the gate resistance. The measured cutoff frequency and maximum frequency of oscillation of the NMOS transistors were all about 25 GHz. All the components including transistors, inductors, capacitors, resistors and pads have

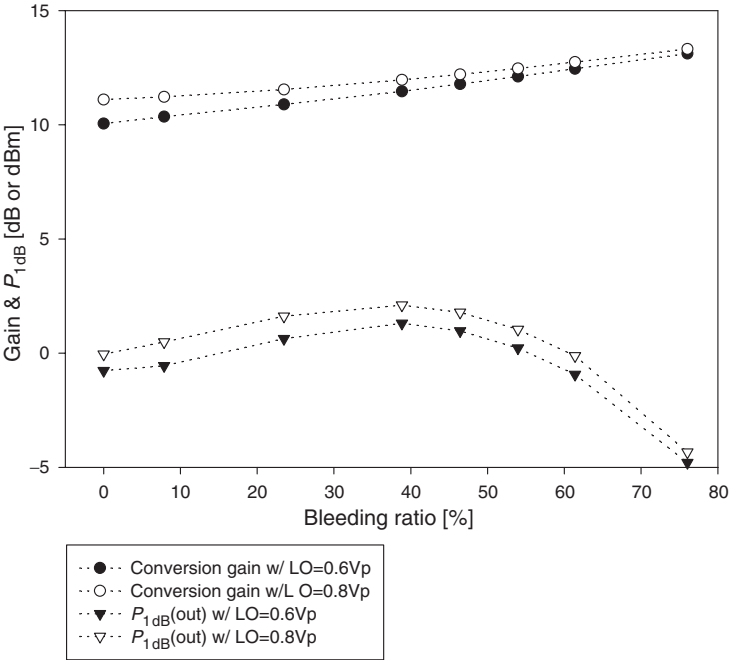

Figure 3. Simulated conversion gain and output $P_{1\,dB}$ variation with bleeding. IF = −30 dBm at 350 MHz, LO = 2.1 GHz.

been previously fabricated using the same technology and carefully modeled as macro cells to fit the measured *s*-parameters up to 10 GHz. The three in/out ports, V_{DD} and ground pads are assumed to be connected to the outside through the minimal bond wire, which was simply modelled by the series inductance and the resistance of 0.8 nH/mm and 200 mΩ/mm, respectively.

Figure 3 shows the variation of the mixer conversion gain and the output $P_{1\,dB}$ as a function of the bleeding ratio. The currents through the transconductance stage transistors M_1 and M_2 are about 5.7 mA, and the CDCS output balun consumes 4.7 mA of current. The bleeding ratio is defined as the ratio of the current through the bleeding PMOS transistors (M_{P1} and M_{P2}) to the current through M_1 and M_2, and is varied by changing the PMOS size. The case where no bleeding PMOS transistor is used is represented by 0%. The simulation results with two different LO amplitudes ($0.6V_p$ and $0.8V_p$ differential) are presented.

In figure 3, the values of the conversion gain and the output $P_{1\,dB}$ depend on LO amplitude. In general, the conversion gain and the output $P_{1\,dB}$ improves at higher LO drive. This is due to the more ideal switching of the switching transistors.

As can be seen in figure 3, the conversion gain improves as the bleeding ratio increases, more efficiently with lower LO drive. As will be clarified in the discussion concerning the results in figure 4, the gain improvement is caused by the enhanced switching efficiency of the switching transistors due to the reduced current by the bleeding, as well as by the enhancement of transconductance with the increased reuse current.

In figure 3, linearity improves by noticeable amounts with current-reuse bleeding and it seems there exists some optimal condition for the bleeding ratio. When the bleeding current is about 40% of the drive current, which corresponds to 5 to 6

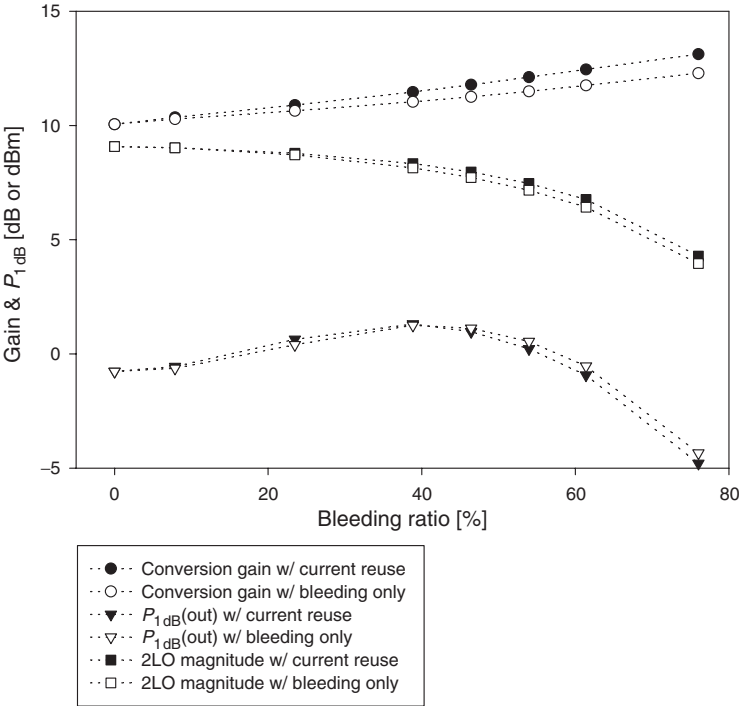

Figure 4. Simulated conversion gain, output $P_{1\,dB}$, and 2LO characteristics with and without current reusing. IF $= -30$ dBm, LO $= 0.6V_p$ (differential).

PMOS fingers, the output $P_{1\,dB}$ shows its maximum. Simple bleeding mixer without current reusing also showed similar behaviour.

In figure 4 we compare the characteristics of the bleeding mixer with and without current reusing when the differential LO amplitude is $0.6V_p$. For the bleeding-only case in figure 4, the gates of the PMOS transistors in figure 1 were disconnected from the IF input and directly connected to the same dc bias level. The improvement in conversion gain with bleeding-only is also effective, which must be caused by the enhanced switching efficiency of the switching transistors by the reduced current. The improvement in conversion gain with current reusing is not so effective in figure 4. This is because small-size PMOS transistors are used for the bleeding. For example, the width of PMOS transistor is 30 μm for 46% of the bleeding ratio in figure 4. If larger PMOS bleeding transistors are used with separate gate bias, the gain improvement by the current reusing can be more effective. However it requires additional bias circuits to assign proper dc current through PMOS transistors and the on-chip dc blocking capacitor between the gates of the PMOS transistors and the NMOS transistors introduces signal loss as well.

In figures 3 and 4, the linearity of the mixer degrades as the bleeding ratio increases above a certain value. The linearity degradation had been monitored in the down-conversion mixer incorporating the current bleeding technique (Liu and Westerwick 2000). However, detailed explanation for the mechanism has not been given. To figure out the mechanism involved in the linearity variation in figure 4, internal voltage and current variations have been monitored.

The linearity characteristics in figure 4 involve two mechanisms. Firstly, the linearity improves with more bleeding as the current through the switching transistors via the common-gate transistor (M_3 and M_4) decreases. In this regime, the linearity is determined by the voltage limiting, where the transistors in the common-gate stage and the switching transistors go out of the saturation region of operation as the amplitude of IF signal increases. Since the gate-source voltage required to sustain the reduced dc current decreases with more bleeding, the required drain-source voltage to maintain the saturation region of operation diminishes. Therefore the output $P_{1\,\mathrm{dB}}$ improves as the bleeding ratio increases. When smaller transistors are used for the switching transistors to enhance the switching efficiency and hence to increase the conversion gain, the required gate-source voltage at the switching transistors increases and so does the drain-source voltage. Therefore the linearity at 0% bleeding ratio degrades. In this case, the linearity improvement with bleeding is more prominent, since the linearity is poor with 0% bleeding.

Secondly, the linearity degrades by the current limiting as the bleeding ratio exceeds certain amount, as can be seen in figure 4. Since the bias current through the common-gate stage decreases monotonically with more bleeding, the lower bound of current swing reaches zero faster with excessive bleeding. The drain current of the common-gate transistor experiences more severe distortion as the amplitude of IF signal increases. Therefore, in this aspect, the dc current through the common-gate transistor should be maintained large enough to extend the linearity above some specific level.

These two mechanisms counteract with each other, and result in best linearity when the bleeding current through PMOS transistor is about 40% of the driving current in figure 4. When current reusing is incorporated, the transconductance increases by the added transconductance of the PMOS transistor, leading to higher current swing. And hence the current limiting occurs at lower IF input power. The resulting output $P_{1\,\mathrm{dB}}$ with current reusing is getting somewhat worse at higher bleeding ratio, compared to the bleeding-only case, as can be seen in figure 4.

In figure 4, the 2LO frequency component in the radio frequency (RF) output spectrum is also plotted as a function of the bleeding ratio. It is simply normalized to the IF power without any physical meaning to show the relative magnitude of 2LO compared to that of RF. The magnitude of 2LO decreases with more bleeding. This is because the impedance seen at the output of cascode stage increases as the average current decreases with more bleeding, which is the well-known ac characteristic of MOS transistors in saturation. The mechanism that determines the amplitude of 2LO at the mixer output is explained with the help of figure 2. Since the 2LO signal comes out as a common-mode signal at the output of the Gilbert cell, the 2LO signal should be negligible at the final output (the RF port) for the symmetric output buffer. However due to the asymmetries in the CDCS buffer balun used, the 2LO signal appears at the output.

Figure 5 compares the mixer characteristics with and without cascoding the transconductance stage when the LO amplitude is $0.6V_{\mathrm{p}}$. For both cases presented in figure 5, bleeding was adopted without the current reusing. For the case without cascode, the simple common-source stage replaces the cascode stage.

Figure 5 shows that the peak output $P_{1\,\mathrm{dB}}$ level can be improved by adopting cascode structure. In the case of the non-cascoded structure, the initial improvement in linearity as appeared in the cascoded structure is not much shown since only two transistors are stacked between supply voltage and ground, and hence the voltage

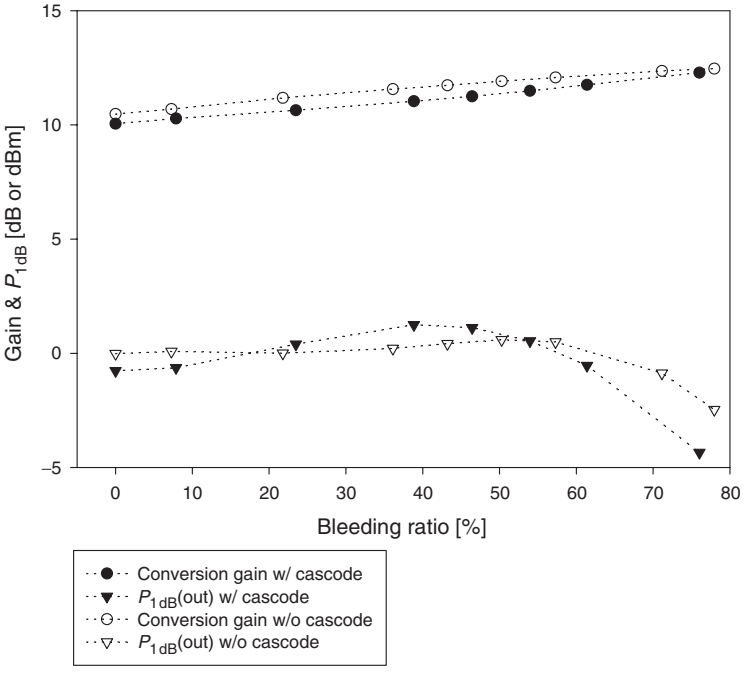

Figure 5. Simulated conversion gain and output $P_{1\,\mathrm{dB}}$ characteristics with and without cascoding the transconductance stage. IF $= -30$ dBm, LO (differential) $= 0.6V_{\mathrm{p}}$.

headroom for each transistor is adequate. Note that even in the design with a non-cascoded structure, there can be a voltage-headroom problem if the design stacks more devices for any purpose, and then the improvement in the linearity with bleeding can be effective. In the non-cascoded case in figure 5, the output $P_{1\,\mathrm{dB}}$ worsens noticeably when the bleeding ratio exceeds 70%. The output $P_{1\,\mathrm{dB}}$ worsens at larger bleeding ratio in the simple common-source structure since the bias current of the transconductance stage is larger by about 5% in this design.

Figure 6 shows the simulated conversion gain and the single-side-band (SSB) noise figure (NF) variation as a function of bleeding ratio when the amplitude of LO is $0.6V_{\mathrm{p}}$. In figure 6, the characteristics with and without current reusing are compared. Improvement in noise characteristic with current bleeding is clearly shown even though the NF value itself is somewhat lower than expected, which is the result of utilizing the inaccurate noise model defined in the simulator. The noise model includes thermal noise, drain channel noise, and flicker noise. The induced-gate noise model (van der Ziel 1986) is missing, but it was effectively incorporated through the gate resistance included in the transistor macro model, which matches well with the measured *s*-parameters of the transistor used. However we believe that the drain channel noise model in the simulator somewhat underestimates the noise generated in the short channel transistors we are using, since the noise coefficient used is only good for long channel transistors (Layman and Chamberlain 1989).

The improvement in noise figure with current reusing has been explained with the enhanced transconductance (Karanicolas 1996). In figure 6, however, noise figure improves even with bleeding only, which has never been explained before.

To figure out the reasons concerning the improvement in noise figure with bleeding only, we have examined the output noise contribution of each component in the

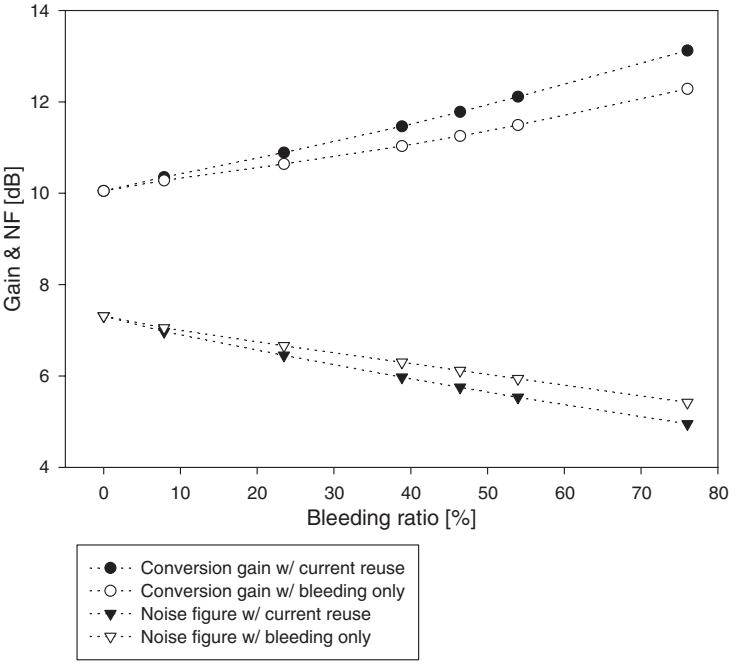

Figure 6. Simulated conversion gain and noise figure characteristics with and without current reuse. IF $= -30$ dBm, LO (differential) $= 0.6V_{\mathrm{p}}$.

circuit. Note that noise figure can be defined by the ratio of the total output noise power to the output noise due to input source resistor. The improvement in noise characteristics with current bleeding can be explained by two mechanisms that occur, one of which is the increased conversion gain and the other is more ideal switching of the switching transistors, both of which are available with smaller current flowing through switching transistors. The ideal switching tends to reduce noise generated in the switching transistors by reducing the amount of time that both transistors are on. This characteristic is confirmed by the fact that the drain-channel noise contribution of the switching transistors and the thermal noise contribution from the LO-signal source resistor is reduced with increase in the current bleeding ratio. As the conversion gain increases with more bleeding, the total output noise power increases since the noise components prior to the gain stage are multiplied by the increased gain, but the noise generated in the switching transistors decreases due to more ideal switching, and therefore the percentage output noise contribution of the input source resistor increases to result in the reduced noise figure.

The additional improvement in the noise figure when adopting the current-reuse technique is simply due to gain improvement provided by the additional transconductance of the PMOS bleeding transistor. The percentage output noise contribution of the input source increases to result in the reduced noise figure again. However it is minimal in figure 6 since the chosen PMOS transistor size is small.

If the size of PMOS transistor is increased with separate bias circuits, the amount of noise generated by the PMOS bleeding transistor itself increases and the noise figure may degrade since the noise contribution of the current source connected in parallel with the signal path becomes larger as the transconductance of the current source increases (Razavi 2000). Therefore the noise figure with bleeding only is

expected to be larger than that shown in figure 6. However, in this case, the improvement in noise figure with current reusing can be more prominent than that shown in figure 6 due to the improved gain. This was confirmed in the additional simulations where we chose the PMOS transistor size as 200 μm with separate bias circuits to set the bleeding ratio of 35%, which is somewhat lower but was chosen to get the best linearity. The conversion gain and the output $P_{1\,\mathrm{dB}}$ were comparable to those of the design with 30 μm-wide PMOS transistor, which corresponds to the case with 46% of the bleeding ratio in figure 4. The noise figure in this case with the LO amplitude of $0.6\,V_{\mathrm{p}}$ is about 7.3 dB with bleeding only, but it reduces to 5.6 dB with current-reuse bleeding, which is slightly lower than that with 46% of the bleeding ratio in figure 6.

To reduce the noise contribution of the bleeding current source, a design that incorporates common-mode current injection through the LC resonance tank has been suggested (MacEachern and Manku 1998). However the LC resonator may not be effective as it blocks the noise component only at one frequency. The image and high frequency noise contributions still exist. However with the current-reuse bleeding technique suggested in this work, the noise contribution of the PMOS bleeding transistor can be minimized as it becomes a part of the transconductance stage.

4. Measurement results

The mixer circuit shown in figure 1 was fabricated using a standard 0.35 μm 4-metel and 2-poly CMOS process to verify the analysis. The PMOS transistor size was chosen as 30 μm to set the bleeding ratio of 46%, which seems to provide good performances in terms of conversion gain, linearity, and noise. The photograph of the chip is given in figure 7. The chip size is about $1.15 \times 0.99\,\mathrm{mm}^2$.

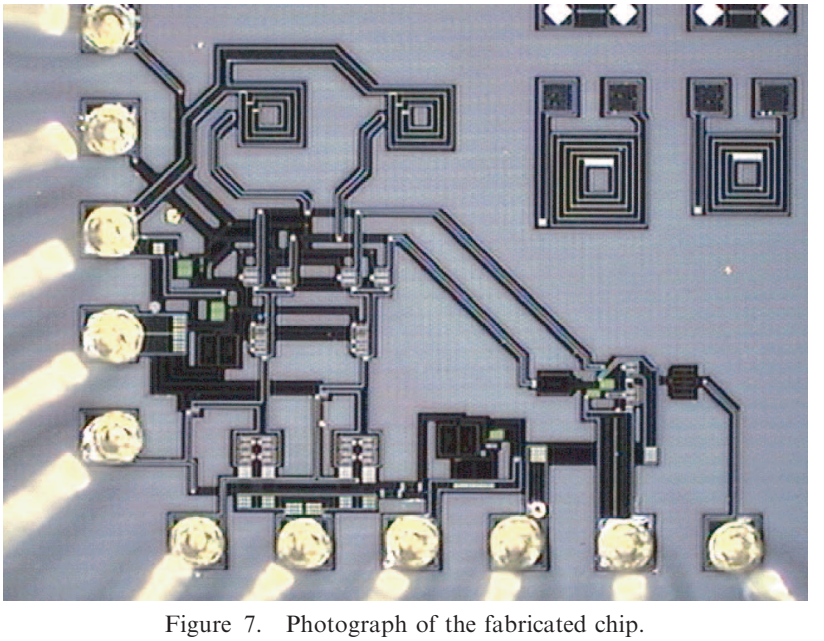

Figure 7. Photograph of the fabricated chip.

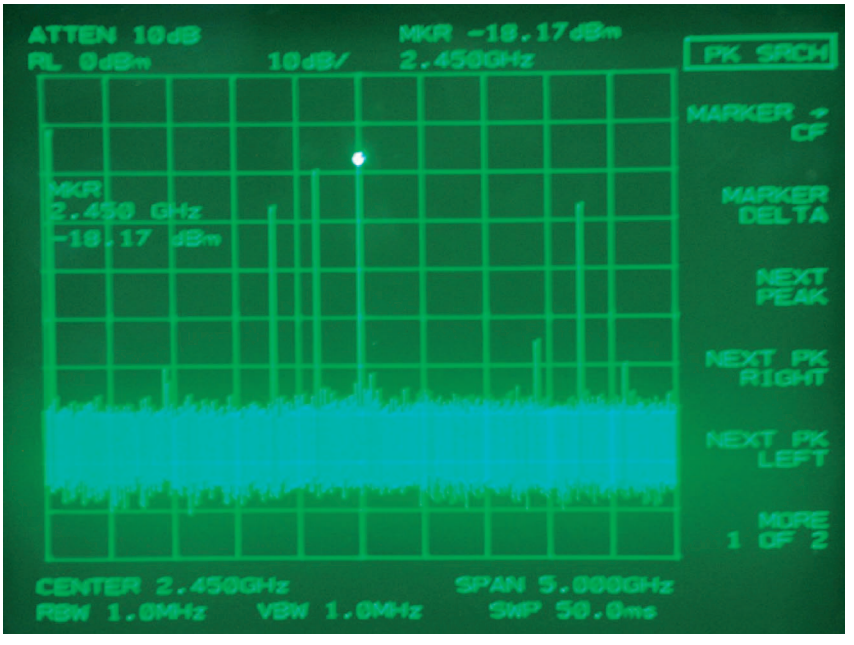

Figure 8. Measured output frequency spectrum of the up-conversion mixer. IF = −30 dBm at 350 MHz, LO = 0 dBm at 2.1 GHz.

Figure 8 shows the measured output frequency spectrum of the fabricated up-conversion mixer with IF = −30 dBm at 350 MHz, LO = 0 dBm at 2.1 GHz. The measurement includes external transformer balun and cable losses. The bias current through each of the transconductance stage was 5.5 mA, and the output balun consumed 4.8 mA of current at V_{DD}=3 V. In figure 8, considering the power loss through the external IF balun and the cables, the conversion gain is about 14 dB. The simulated and measured characteristics are compared in table 1.

In table 1, the measured characteristics are in good agreement with the simulated results, and the overall performance of the fabricated up-conversion mixer is respectable. Compared to the simulated results, the LO component at the output is quite large. The simulations assume ideal situations. However, the LO suppression at the output can be degraded for many different reasons such as imperfect match in the mixer core transistors, mismatch in interconnect parasitics, capacitive and inductive coupling, and substrate coupling, etc. For example, the mismatch in core transistors can be serious by the process variations. The transistor mismatch can be reduced by adopting careful layout practices such as quad-transistor structure for differential pair (Bastos *et al.* 1996), which has not been executed in this design. Also in the layout, the metal-3 LO signal lines cross the metal-4 mixer output lines by mistake.

Figure 9 shows the measured gain compression characteristics of the mixer. The external transformer balun and cable losses are not calibrated out in the plotted data. With 5.5 mA of the bias current through the transconductance stage, the conversion gain is about 14 dB and the output $P_{1\,dB}$ is about 1.5 dBm when considering the external losses. When the bias current is reduced to 3.9 mA by decreasing the supply voltage for the input bias circuit, the conversion gain increases by 1 dB, but the output P_{1dB} degrades by 12 dB. This is predicted from the discussions relating to

Specifications		Simulation	Measurement
Conditions		$f_{IF} = 350$ MHz, $f_{LO} = 2.1$ GHz, $f_{RF} = 2.45$ GHz, $V_{DD} = 3$ V, LO $= 0.8 V_p$ (differential)	LO $= 0$ dBm (single-ended)
DC current	Mixer core	11.4 mA	11.1 mA
	Output balun	4.7 mA	4.8 mA
Conversion gain		12.2 dB	14 dB
$P_{1\,dB}$(out)		1.7 dBm	1.5 dBm
OIP3		9 dBm	9.5 dBm
SSB noise figure		5.6 dB	8 dB (LO $= 0$ dBm) 7.4 dB (LO $= 3$ dBm)
LO power at the output		−91 dBm	−21.5 dBm
2LO power at the output		−18.5 dBm	−27.3 dBm

Table 1. Comparison between simulated and measured data.

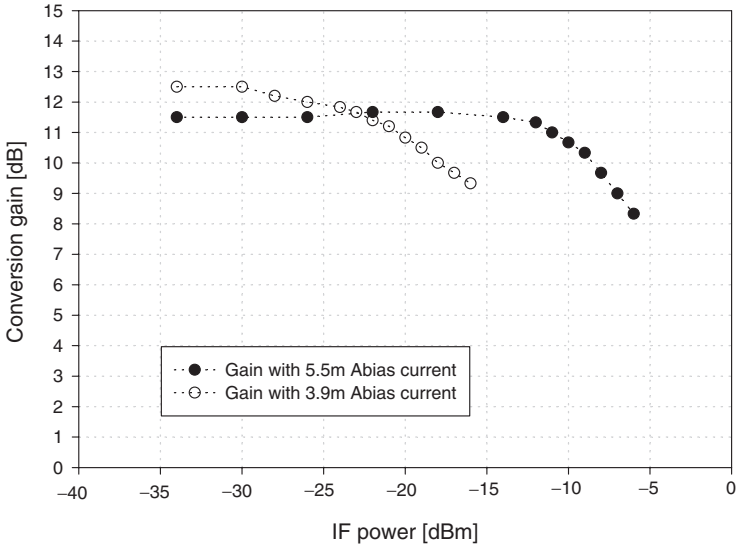

Figure 9. Measured gain compression characteristics. IF $= 350$ MHz, LO $= 0$ dBm at 2.1 GHz, $V_{DD} = 3$ V.

figures 3 and 4. When the bias voltage of the input NMOS and PMOS transistors is decreased to reduce the bias current, the NMOS current is decreasing sensitively, but the PMOS current does not change significantly since the gate-source voltage of the PMOS is large. Therefore the bleeding ratio must be increased greatly with this reduced bias current. More bleeding improves the conversion gain, but excessive bleeding degrades the linearity by the current limiting as discussed before. It is also confirmed that the 2LO signal power is reduced from −27.3 dBm to −33.3 dBm when the bias current is reduced from 5.5 mA to 3.9 mA. This is also predicted from the simulation results in figure 4.

Figure 10 compares the measured IP3 to the simulation. Simulation extrapolates to 9 dBm of OIP3, while the measured OIP3 is about 9.5 dBm considering the 0.5 dB

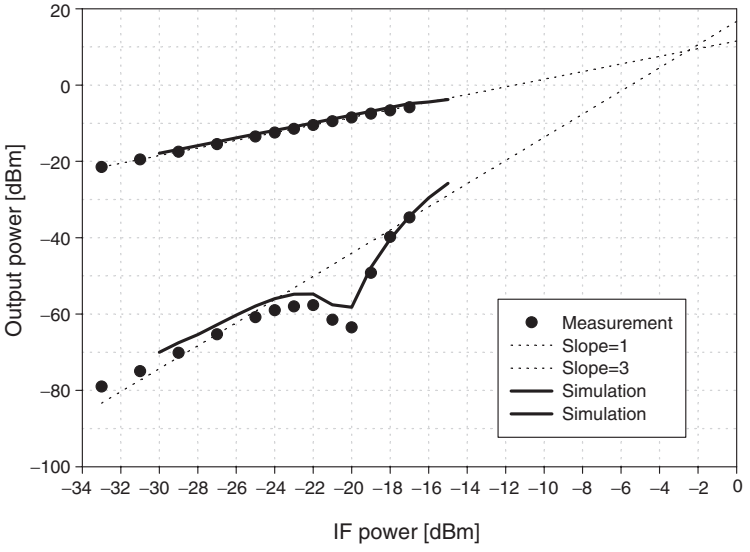

Figure 10. Measured and simulated IP3 characteristics. IF = 350 MHz, and LO = 2.1 GHz. LO = 0 dBm for measurement, and LO = $0.8V_p$ for simulation.

of RF cable loss. The notch in the 3rd-order product, which is the characteristic appearing in some of Class AB-type mixers (Orsatti *et al.* 1999), is well predicted by simulation. The notch seems to be the result of harmonic cancellation, which is uncertain, but is beyond the scope of this work.

As can be seen in table 1, the measured noise figure is 8 dB and 7.4 dB at 2.45 GHz when LO power is 0 dBm and 3 dBm, respectively. The measured noise figure of 7.4 dB is a respectable value especially when considering that the mixer incorporates the resistive matching at the IF input. This is truly the most important benefit we can get by adopting the current-reuse bleeding technique, as explained relating the result in figure 6. The disagreement between the measurement and the simulation is expected due to the inaccuracy in the MOS transistor noise model inside the simulator.

5. Summary

A 2.45 GHz double-balanced modified Gilbert-type CMOS up-conversion mixer design utilizing the current-reuse bleeding PMOS transistors has been thoroughly examined based on simulations to demonstrate many advantages achievable when adopting the current-reuse bleeding technique in the mixer design. The measurement of the fabricated chip based on the standard 0.35 μm CMOS process confirmed the validity of the simulation results. The measured mixer performance is quite excellent in terms of conversion gain, linearity, and noise, and the measured characteristics are in close agreement with the simulations, which demonstrates the adequacy of the modelling approach based on the macro models for all the active and passive devices used in the design. The current-reuse bleeding technique certainly seems to provide benefits in terms of gain, linearity and noise characteristics. In the mixer incorporating the current-reuse bleeding technique, the conversion gain improves monotonically with more bleeding, which is the benefit provided both by the current bleeding

and the current reusing. The current bleeding improves linearity by a noticeable amount when the voltage headroom is not enough. However with excessive bleeding, linearity degrades by the current-limiting phenomena, which defines the optimal bleeding ratio. Noise performance improves monotonically with more bleeding, which is also the benefit provided both by the current bleeding and the current reusing. The 2LO signal amplitude at the mixer output reduces with more bleeding, which is also beneficial. Above all the benefits provided, the improvement in noise performance seems most valuable. There is trade-offs in determining the current-reuse bleeding ratio, which implies that the benefits can be optimized to get most out of it.

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