Low-power 42 dB-linear single-stage digitally-controlled variable gain amplifier

H.-H. Nguyen, Q.-H. Duong, H.-B. Le, J.-S. Lee and S.-G. Lee

A compact digitally-controlled single-stage variable gain amplifier (VGA) is introduced, which doubles the dB-linear range through the reconfiguration, saves power by 50% while maintaining the same linearity performance compared to those of the previous design. Implemented in 0.18 μm CMOS technology, the 5-bit digitally-controlled VGA achieves dB-linear gain range of 42 dB (−21 to 21 dB) with gain error less than ±0.55 dB, bandwidth of 84 MHz at maximum gain of 21 dB and maximum IIP3 of 14 dBm while consuming only 760 μA from a 1.8 V supply.

Introduction: Variable gain amplifiers (VGAs) are important blocks that can be employed in many communication systems, hearing aids, disc drivers, etc. in order to maximise the dynamic range of the overall system. Obtaining wider dB-linear gain range for each stage is an efficient solution for reducing the amount of power dissipation and the chip size of a VGA, these being the key technical challenges. In the VGA designs reported lately, many pseudo-exponential and Taylor series approximation functions have been proposed to extend the dB-linear range with gain varied in continuous-type [1]. However, these functions are difficult to apply for the VGAs with discrete-type gain variation. Therefore, the pseudo-exponential approximation function, $e^{2x} \simeq (1+x)/(1-x)$, is typically used for discrete-type VGAs [2, 3]. Nguyen *et al.* [3] reported a digitally-controlled VGA cell following the pseudo-exponential approximation function, $e^{2x} \simeq (1+x)/(1-x)$, that can achieve dB-linear gain range of 20 dB with less than ±0.5 dB gain error by simultaneously changing the transistor size and bias currents of the input and diode-connected load transistors of the differential amplifier. Moreover, the discrete changes of input and load transistors [3] lead to better linearity compared to that of the current density controlled VGAs [1]. This Letter presents the design of a digitally-controlled VGA that can double the dB-linear gain range while dissipating only half the amount of power and yet maintains thesame linearity performance compared to that of the VGA cell reported in [3].

Proposed VGA architecture: Fig. 1 shows the VGA cell proposed in [3], which consists of a differential input pair (M_1 and M_2) and diode-connected loads (M_3 and M_4). By varying the transistor size and bias current simultaneously by the same ratio, the dB-linear voltage gain of the VGA cell can be varied by more than 20 dB with gain error less than ±0.5 dB [3].

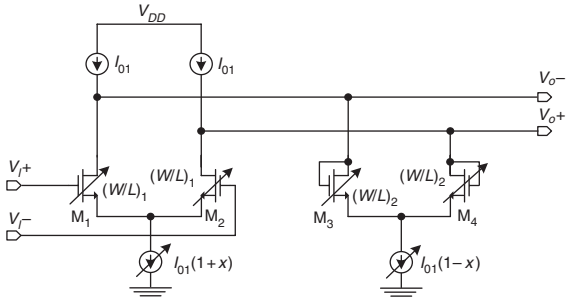

Fig. 1 *Schematic of VGA cells reported in [3]*

An amplifier architecture, which is equivalent to the VGA cell shown in Fig. 1, but can double the dB-linear range, is shown in Fig. 2*a*. In Fig. 2*a*, the input and diode-connected transistor pairs are implemented as a complementary combination of NMOS and PMOS transistors. Depending on the logic level of the control signal S, the PMOS or the NMOS transistor pairs switch the role of input or diode-connected transistors, respectively, such that, the PMOS and NMOS input transistor configurations provide the lower- and upper-half of the gain range, respectively, doubling the gain range compare to that of [3]. In Fig. 1, since the input and diode-connected transistors of the VGA cell are biased with current $I_{01}(1+x)$ and $I_{01}(1-x)$, respectively, the total current is $2I_{01}$. In the VGA shown in Fig. 2*a*, the NMOS and PMOS transistor pairs are biased at $I_{01}(1+x)$ and $I_{02}(1-x)$, respectively, where the condition $I_{01}(1+x) > I_{02}(1-x)$ is secured, and the difference of the two currents $I_{01}(1+x) - I_{02}(1-x)$ is compensated for by the common-mode feedback circuit. In Fig. 2*a*, since the value of x is varied over the range of $(-1, 1)$, the total current varies from 0 to $2I_{01}$ with an average of I_{01}. Thus, on average, the proposed VGA cell consumes 50% less power than that of the VGA cell reported in [3]. As in [3], the current density of the NMOS and PMOS differential pairs of the proposed VGA cell are kept constant over the gain variation. Hence, the linearity performance is the same as that of the VGA cell reported in [3]. Furthermore, the chip area of the proposed VGA cell is approximately equal to that of the one reported in [3] since the number of transistors in the two VGA cells are nearly identical.

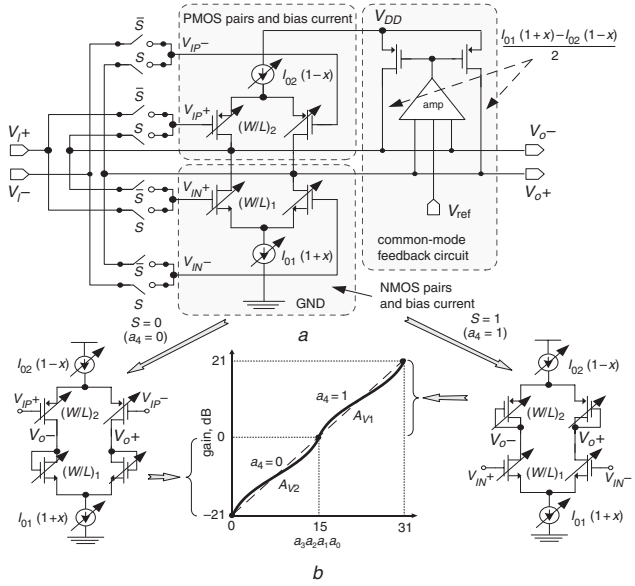

Fig. 2 *Proposed VGA cell*

a Circuit schematic including reconfiguration switches
b Two VGA configurations and gain against control bits

Circuit design: The detailed schematic of the proposed 5-bit digitally-controlled VGA cell is shown in Fig. 3. In Fig. 3, four least significant bits (LSBs) $a_3a_2a_1a_0$ are used for the size control of differential input/diode-connected pairs and their bias currents and the one most significant bit (MSB) a_4 (control signal S in Fig. 2*a*) is used for altering the roles of PMOS and NMOS transistor pairs. The aspect ratios and bias currents of the differential NMOS and PMOS transistor pairs against control bits can be given by

$$(W/L)_N = (W/L)_1(2^0a_0 + 2^1a_1 + 2^2a_2 + 2^3a_3 + k) \quad (1)$$

$$(W/L)_P = (W/L)_2(2^0\overline{a_0} + 2^1\overline{a_1} + 2^2\overline{a_2} + 2^3\overline{a_3} + k) \quad (2)$$

$$I_1 = I_{01}(2^0a_0 + 2^1a_1 + 2^2a_2 + 2^3a_3 + k) \quad (3)$$

$$I_2 = I_{02}(2^0\overline{a_0} + 2^1\overline{a_1} + 2^2\overline{a_2} + 2^3\overline{a_3} + k) \quad (4)$$

where a_i is the digital control bit, and k is a constant for adjusting the gain range of the VGA. Using (1)–(4), the differential voltage gains of the proposed VGA can be given by

$$A_{V1} = \sqrt{\frac{\mu_n(W/L)_N I_1}{\mu_p(W/L)_P I_2}} = \beta\frac{2^0a_0 + 2^1a_1 + 2^2a_2 + 2^3a_3 + k}{2^0\overline{a_0} + 2^1\overline{a_1} + 2^2\overline{a_2} + 2^3\overline{a_3} + k}$$

$$= \beta\frac{x+k}{2^4 - 1 - x + k} \quad (5)$$

$$A_{V2} = \sqrt{\frac{\mu_p(W/L)_P I_2}{\mu_b(W/L)_N I_1}}$$

$$= \left(\frac{1}{\beta}\right)\frac{2^0\overline{a_0} + 2^1\overline{a_1} + 2^2\overline{a_2} + 2^3\overline{a_3} + k}{2^0a_0 + 2^1a_1 + 2^2a_2 + 2^3a_3 + k}$$

$$= \left(\frac{1}{\beta}\right)\frac{2^4 - 1 - x + k}{x + k} \quad (6)$$

where A_{V1} and A_{V2} are the gains for the case of NMOS ($a_4 = 1$) and PMOS ($a_4 = 0$) input transistor configurations, respectively, $x = 2^0a_0 + 2^1a_1 + 2^2a_2 + 2^3a_3$ the digital control word and

$$\beta = \sqrt{\frac{\mu_n(W/L)_1 I_{01}}{\mu_p(W/L)_2 I_{02}}}$$

a constant. The constant $k = 5$ is chosen so that A_{V1} and A_{V2} cover each 21 dB of gain range, respectively, and β is chosen so that there is overlap between the gain variation range of A_{V1} and A_{V2} (see Fig. 2*b*). As x (the decimal value of four LSBs) varies from 0 to 15, A_{V1} and A_{V2} vary in the ranges −21 to 0 dB and 0 to 21 dB, respectively, with an overall range of 42 dB (−21 to 21 dB) in 1.31 dB steps. The proposed VGA topology can be implemented with larger number of control bits for smaller gain step.

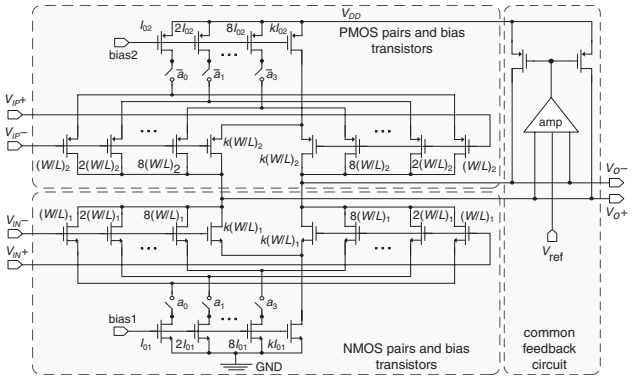

Fig. 3 *Detailed circuit schematic of proposed 5-bit digitally-controlled VGA*

Measurement results: The proposed VGA is fabricated in 0.18 μm CMOS technology and the chip occupies 0.05 mm^2, excluding bonding pads, and dissipates average current of 760 μA from a 1.8 V supply. Fig. 4 shows the measured gain against the digital control word at 30 MHz. As can be seen in Fig. 4, the proposed VGA shows a dB-linear gain range of 42 dB from −21 to 21 dB with gain error less than ±0.55 dB. The measured IIP3, P1 dB, and 3 dB bandwidth are −9 to 14 dBm, −21.5 to −9 dBm, and 84 MHz, respectively. From the simulation, the VGA shows a noise figure (NF) of less than 13 dB at the maximum gain of 21 dB.

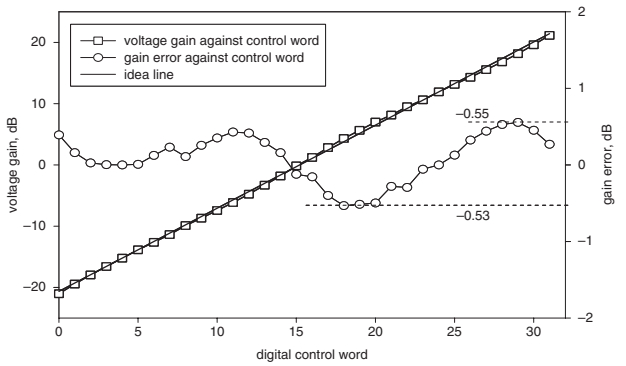

Fig. 4 *Measured gain and gain-error against control word*

Conclusions: A digitally-controlled VGA cell architecture with a new gain control scheme, which includes reconfiguration by the PMOS/NMOS input and load pair switching, and simultaneous switching of the transistor sizes and their bias currents, is presented. The compact 5 bit digitally-controlled VGA implemented in 0.18 μm CMOS shows dB-linear gain range of 42 dB (−21 to 21 dB) with gain error less than ±0.55 dB, bandwidth of 84 MHz at the maximum gain of 21 dB, IIP3 of −9 to 14 dBm, and P1 dB of −21.5 to −9 dBm, respectively, while dissipating an average current of only 760 μA from a 1.8 V supply. The proposed VGA extends the dB-linear gain range by two times, saves power dissipation by 50%, provides the same linearity, and occupies the same chip area compared to those of previous work.

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