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A 1-V low power gain boosted self-cascoding current mirror operational transconductance amplifier

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A low-voltage, micro-power, low-noise, high-gain, high-output swing current mirror-based operational transconductance amplifier (OTA) is presented. The proposed OTA achieves high DC gain and output swing by the adoption of gain boosted current mirroring and self-cascoding techniques. From the simulation, the proposed OTA implemented on a 0.18 μm CMOS shows the DC gain up to 90 dB with a gain bandwidth of 700 KHz for a load capacitor of 1 pF and an output voltage swing of 600 mV. The OTA dissipates only 750 nW from 1.0 V supply.

Keywords: current mirror OTA; low voltage; low power; OTA; self-cascode

1. Introduction

Operational transconductance amplifiers (OTAs) are the main building blocks of many circuits where the OTA tends to dominate the power consumption. The key performance parameters of OTAs are output swing, DC gain, and gain bandwidth (GBW). The output swing is of great importance in low-voltage (LV) and low-power (LP) designs. Single-stage OTAs tend to be more power efficient than two-stage OTAs, because no power is wasted in driving the compensation capacitance in single-stage OTAs (Chandrawat and Mishra 2007). The single-stage OTA that can provide rail-to-rail output swing is the current mirror-based OTA (CMOTA) which is shown in Figure 1. The typical voltage gain of the CMOTA is about 20–40 dB in submicron technologies. With many applications, the required DC of OTAs is much higher than 40 dB. There are many techniques to increase the gain of the CMOTA. Figure 2 shows the CMOTA with the gain boosted current mirroring technique which can enhance the gain by 10–20 dB without additional power consumption (Yao, Steyaert and Sansen 2004). In Figure 2, a portion of input transistor (M_1/M_2) currents are diverted by the current sources (M_5/M_6) from the current mirror transistors (M_3/M_4). As a result, the DC gain of the OTA is boosted by $1/(1-k)$ times, where $k = I_{D5,6}/I_{D1,2}$. By increasing k close to 1, the OTA gain can be increased significantly. However, the higher the k factor, the higher the impedance at node C, and the lower the corresponding non-dominant pole frequency. This non-dominant pole degrades the phase margin of the OTA and may cause stability

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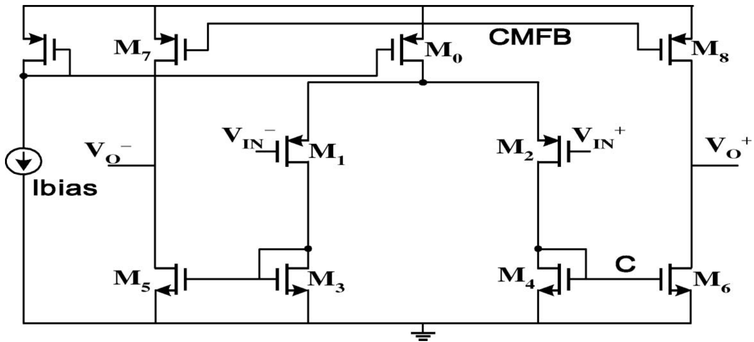

Figure 1. The conventional current mirror OTA.

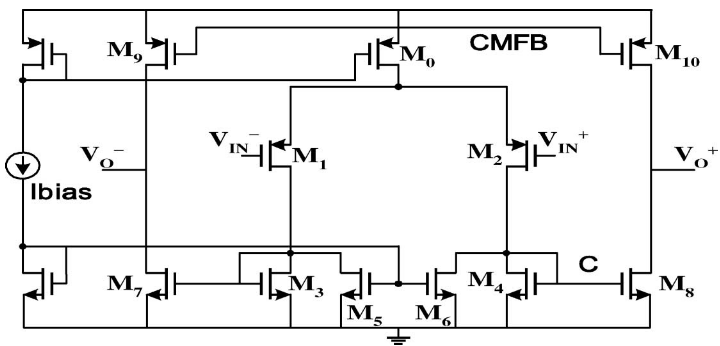

Figure 2. The current mirror OTA with gain enhancement.

problems. Therefore, the increase in k factor is limited, and the actual gain enhancement is not higher than 20 dB. The self-cascoding is another technique that can increase the DC gain of CMOTAs while still providing enough output voltage swing (Castello, Grassi and Donati 1990; Gerosa and Neviani 2003) as shown in Figure 3. In Figure 3, for high output voltage swing, $M_5/M_6/M_{11}/M_{12}$ and $M_7/M_8/M_9/M_{10}$ are biased to operate in strong and weak inversion regions, respectively. Using the OTA topology shown in Figure 3, Gerosa and Neviani (2003) report a DC gain of 65 dB with an output voltage swing of 620 mV out of 1.2 V supply.

2. Circuit design

Figure 4 shows the schematic of the OTA proposed in this work. The proposed OTA combines the two previous techniques, gain boosted current mirroring and self-cascoding. The combination of the two techniques allows a very high DC gain, low supply voltage, sub-micro power, and high output swing OTA implementation. The proposed OTA is designed based on a 0.18 μm CMOS with 1.0 V supply. From Figure 4,

$$V_{g8} = V_{gs8} = V_{th} + V_{dsat8} \tag{1}$$

where V_{g8}, V_{gs8}, V_{th}, and V_{dsat8} are gate, gate-source, threshold, and saturation voltages of M_8, respectively. In order to secure the strong inversion region operation of M_8, the drain voltage of M_8 should be larger than the saturation voltage V_{dsat8}.

$$V_{d8} = V_{gs8} - V_{gs10} = V_{th} + V_{dsat8} - V_{gs10} > V_{dsat8} \qquad (2)$$

The inequation (2) holds if $V_{th} > V_{gs10}$, i.e. the transistor M_{10} has to be biased in weak inversion region. In order to force M_4/M_8 to operate under strong inversion, their channel lengths are chosen relatively long. The proposed OTA is designed to work with micro-power; therefore, it is easy to bias M_{10} to operate under a weak inversion region by increasing its size. In this design, the sizes of M_4, M_8, and M_{10} are chosen to be 3/20 μm, 5/20 μm, and 40/1 μm, respectively. The transistors $M_0/M_4/M_6/M_8$ are biased at 500 nA/80 nA/170 nA/125 nA, respectively. The proposed OTA is intended to be used for switched-capacitor (SC) applications, so the SC common-mode feedback circuit shown in the lower part of Figure 4 is adapted because it does not consume extra static power. Figure 5 shows the frequency response and the step response of the proposed OTA. The proposed OTA

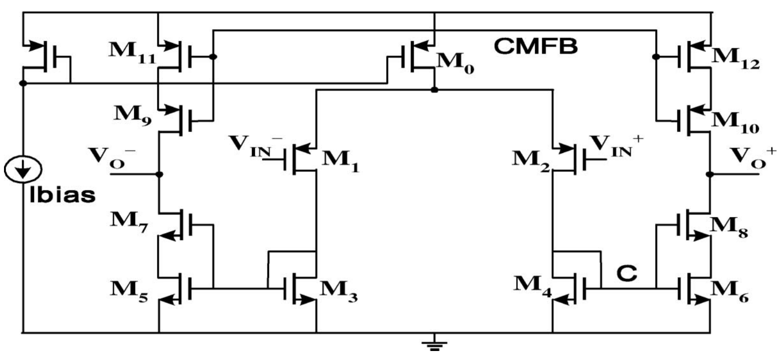

Figure 3. The current mirror OTA with self-cascoding output stage.

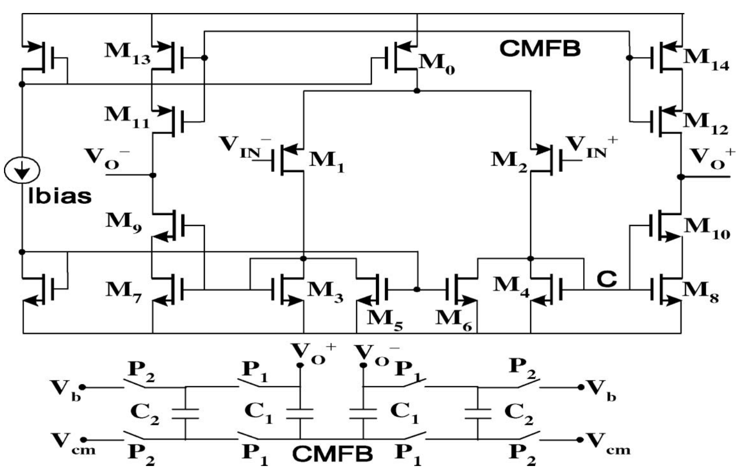

Figure 4. The proposed gain boosted self-cascoding current mirror OTA.

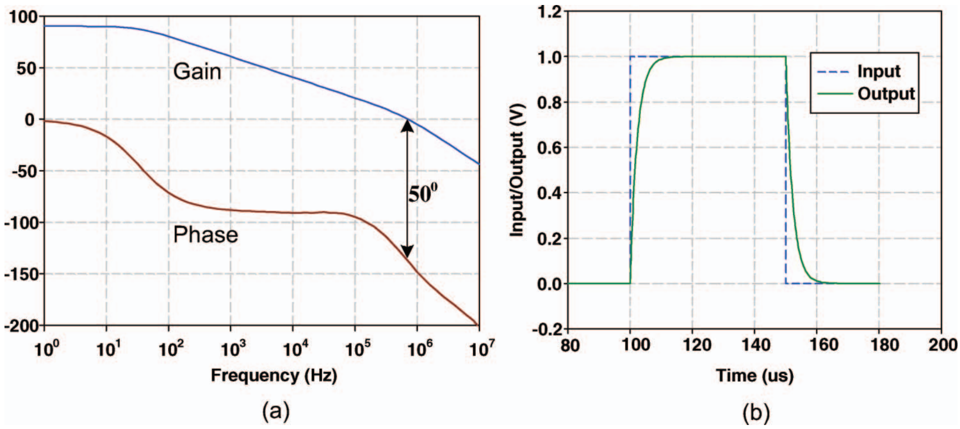

Figure 5. Frequency response of the proposed OTA.

Table 1. Performance summary and comparison.

Specifications	Chandrawat and Mishra 2007	Yao et al. 2004	Gerosa and Neviani 2003	This work
Technology (CMOS)	0.5 μm	90 nm	0.35 μm	0.18 μm
Supply/power	1.0 V/2.56 mW	1.0 V/80 μW	1.2 V/120 nW	1.0 V/750 nW
Output swing (mV)	NA	NA	620	600
DC gain (dB)	86.2	50	65	90
GBW	136.6 MHz	57 MHz	60.4 kHz	700 KHz
Phase margin (°)	NA	57	43	50
Load capacitor (pF)	1	6	NA	1
Slew rate (V/μs)	211	NA	NA	0.3
Settling time	25 ns	NA	NA	5.1 μs

shows a DC gain of 90 dB with GWB product of 700 kHz for a load capacitor value of 1 pF while achieving the phase margin of 50°. The settling time is 5.1 μs, and the slew rate is 0.3 V/μs. The input referred noise of the OTA at 10 kHz is 79 nVrms/sqrt (Hz), and output voltage swing is 600 mV while dissipating 750 nW from 1.0 V supply. Table 1 summarizes the OTA performance in comparison with prior works.

3. Conclusions

A low-voltage, micro-power, low-noise, high-gain, high-output swing OTA by combing the gain boosted current mirroring and self-cascoding techniques is presented. The design detail and simulated performance is described. The proposed OTA, implemented in 0.18 μm CMOS, shows a DC gain of 90 dB, GWB product of 700 kHz, an output voltage swing of 600 mV while dissipating 750 nW from 1.0 V supply.

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