Single-chip A/D converter for digital microphones with on-chip preamplifier and time-domain noise isolation

H.B. Le, J.W. Nam, S.T. Ryu and S.G. Lee

A 1-bit sigma-delta modulator (ΣΔM) with an on-chip preamplifier for digital electret microphones has been implemented. A differential gm-opamp-RC preamplifier eliminates the traditional single-ended JFET interface and is integrated with an on-chip ΣΔM by removing all external components. The proposed time-domain noise isolation technique preserves circuit performance under a single power supply condition. The prototype implemented in a 0.18 μm CMOS technology achieves a 78 dB dynamic range and 62 dB peak signal-to-noise + distortion ratio (both A-weighted) with a current consumption of 450 μA under a 1.8 V supply.

Introduction: Electret capacitor microphones (ECMs) have been popular for sound inlet devices in many applications. To take out the signal from the electret capacitor (EC), which is modelled as a capacitive voltage source, a JFET amplifier has been attached to the EC as a buffer in a traditional ECM. These days, however, the performance of a JFET-based analogue ECM is not good enough for many high-end mobile multimedia applications. As the physical size of the EC shrinks for compactness, the large input capacitance of the JFET limits the ECM sensitivity. Another drawback is that the analogue signal from the JFET is easily corrupted by external noise. To solve these problems, JFET amplifiers have recently been replaced by CMOS preamplifiers, and the traditional analogue ECM structures are being replaced by digital ECMs, which generate a digital output by embedding an ADC in its cartridge. In this Letter we present a single-chip ADC for digital ECM applications by deriving a well-suited preamplifier architecture and by suggesting a regulator-free switching noise isolation technique.

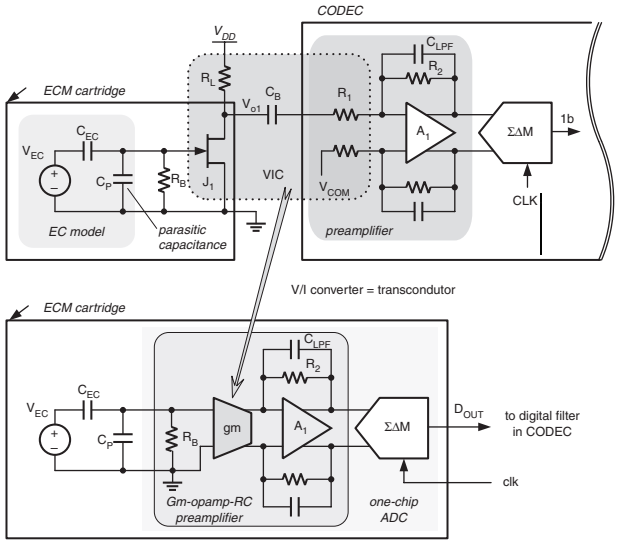

Fig. 1 *Traditional ECM + CODEC configuration (upper) and proposed digital ECM architecture (lower)*

High-impedance preamplifier and ECM architecture: To replace the traditional JFET interface, several CMOS preamplifiers have been suggested [1, 2]. Differently from prior arts, this work has found a proper preamplifier structure from the traditional ECM configuration. The upper part of Fig. 1 shows a traditional ECM and an ADC configuration. The single-ended output of the JFET amplifier, V_{o1}, is connected to the preamplifier in the CODEC via an external DC blocking capacitor, C_B. The preamplifier is composed of R_1, R_2, C_{LPF} and A_1, where C_{LPF} is used for high frequency noise filtering. By following the signal flow from the EC to the preamplifier, one can recognise that the functions of J_1, R_L and R_1 are V/I, I/V and V/I converters, respectively. Thus, each of them can be merged and replaced by a single V/I converter, a gm-cell. This modification combines the JFET-based high impedance interface and preamplifier into a single gm-opamp-RC amplifier, which is similar to the integrator structure in [3] even though the motivations behind them are different. Then, the ECM + ADC configuration becomes simplified, as shown in the lower part of Fig. 1. With no external devices, the preamplifier and ADC can be integrated together on-chip, and the one-chip ADC can then be embedded in an ECM cartridge in order to build up the digital ECM. The designed gm-cell is a PMOS-input folded-cascode OTA. The PMOS input pair has source degeneration resistors to linearise and stabilise the gm value. Since the typical signal level from an EC is about several tens of mV, this open-loop gm-cell can be appropriate in terms of linearity. The output common level of the gm-cell is defined by the common-mode feedback network, which uses triode region transistors in the OTA's cascode branch, specifically in between the power supply and the current source, for no additional power consumption. The input bias resistor, R_B, has been implemented with a weak inversion NMOS transistor in order to obtain a Giga-ohm order resistance. A_1 is a two-stage opamp with its own common-mode feedback.

ΣΔM and time-domain noise isolation: The 1-bit ΣΔ modulator (ΣΔM) in Fig. 1 has been designed with a second-order switched-capacitor configuration. Low power telescopic amplifiers have been used for the integrators, and the loop-filter coefficients have been chosen to reduce the integrators' output swing. All the reference voltages and currents have been defined using the on-chip bandgap reference voltage. An on-chip RC damping filter attached to the reference driver removes the large external capacitor. One special constraint in this design is that only a single pad has been assigned to the power supply for the device compactness. Therefore, the preamplifier and ΣΔM should share the same power supply, which is usually avoided in a general mixed-signal IC design because of the switching noise coupling. One popular way of combating this poor condition is separating the analogue and digital power supplies internally by inserting regulator(s). However, the regulator-based solution cannot be perfect because the switching noise through the common ground and substrate cannot be decoupled. In addition, since the regulator lowers the internal supply voltage by at least 0.2 to 0.3V, this solution can make circuit design difficult. Therefore, we suggest a regulator-free noise isolation technique based on the time-domain noise separation. The proposed method is based on two known facts: 1. the performance of a ΣΔM is especially sensitive to the noise occurring in the neighbourhood of the sampling clock edge [4], and 2. most switching noise in ΣΔM comes from I/O transitions [5]. Thus, in this design, the output data transition is intentionally delayed by 2 ns from the input sampling edge by the D flip-flop inserted in between the ADC and the output driver. Then, the switching noise occurring after sampling decays as time goes on and becomes minimum near the next sampling instant, as described in Fig. 2. In addition to this time-domain noise isolation, noise coupling is minimised by applying star-configured power/ground connections. One drawback with this regulator-free solution can be a poor PSRR, and therefore the entire signal path has been designed in a fully-differential structure, and the layout has been done as symmetrically as possible.

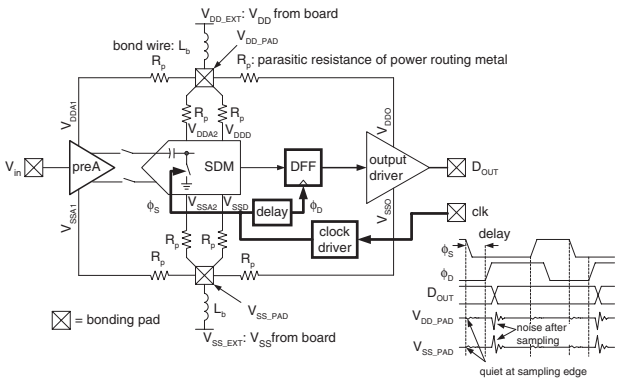

Fig. 2 *Block diagram of prototype with power/ground routing and concept of time-domain noise isolation*

Experimental results: A prototype has been fabricated in a 0.18 μm CMOS process. It operates at a 2.56 MHz sampling frequency with a signal bandwidth of 10 kHz. Fig. 3 shows the measured ADC output spectrum with a 1 kHz 30 mV_{pp} (−20 dBFS) sinusoidal input signal and a measured SNDR of 58 dB. Fig. 4 shows the measured signal-to-noise ratio (SNR) and signal-to-noise + distortion ratio

(SNDR) against input level. The achieved maximum SNDR is 62 dB at a 50 mV_{pp} input signal, and the dynamic range (DR) is 78 dB with a maximum input (0 dBFS) of 300 mV_{pp} (both are A-weighted). The measured SNR is much worse than expected. The reason we have found for this is that the in-band flicker noise had mistakenly been divided by the oversampling ratio in the design phase. Thus, the flicker noise effect is clearly seen in Fig. 3. Harmonic distortion at a large input signal is mainly from the nonlinearity of the open-loop gm-cell. However, the result is acceptable for ECM since typically it requires a THD of less than 10% at 0dBFS. The measured PSRR with 100 mV 217 Hz sine wave is 85 dB. The total current consumption is 450 μA at a 1.8 V supply. The core size excluding pads is 400 × 600 μm.

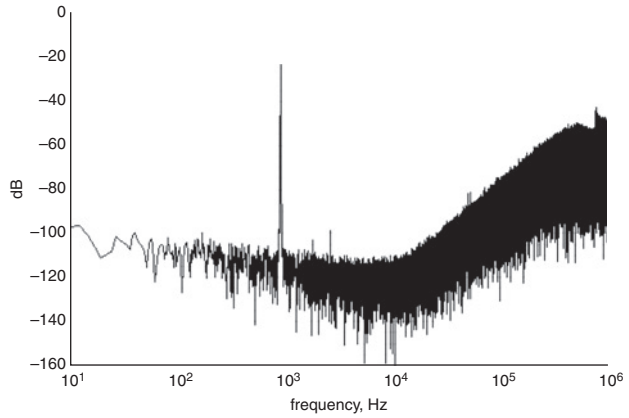

Fig. 3 *Measured ADC output spectrum with 1 kHz 30 mV_{pp} (−20 dBFS) sinusoidal input signal*

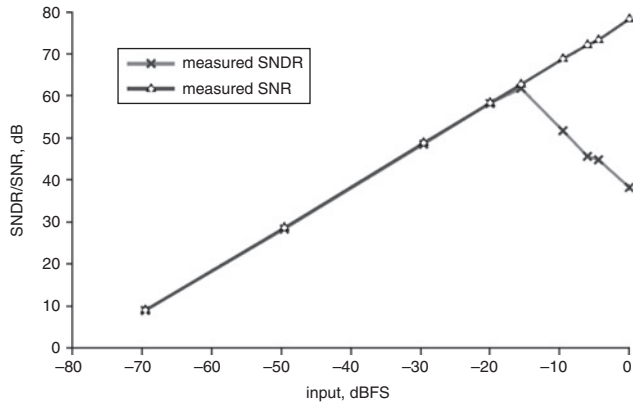

Fig. 4 *Measured SNR and SNDR against input level*
0 dBFS = 300 mV_{pp}

Conclusion: A single-chip A/D converter for digital ECMs is presented. The gm-opamp-RC configured preamplifier enables a compact one-chip ADC with no need for external devices. The noise-coupling problem under a single power supply condition is alleviated by ensuring undisturbed signal sampling using the time-domain noise isolation technique and the fully differential circuits.

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