A Low-Parasitic and Common-Centroid Cross-Coupled CMOS Transistor Structure for High-Frequency VCO Design

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***Abstract*—This letter reports a cross-coupled transistor structure that allows simple routing, induces no gate–drain overlap interconnect capacitances, minimizes the parasitic resistances of interconnects, allows smaller drain-junction parasitic capacitances, and provides inherent common-centroid characteristic, all of which help to improve the high-frequency and wideband performances of CMOS voltage-controlled oscillators (VCOs). The proposed cross-coupled transistor structure is applied for a 26.2-GHz differential VCO design which dissipates 7.3 mA from 1.8-V supply using 0.18-μm CMOS. Measurements show 2.1-GHz, 29%, and 4-dB improvements in operating frequency, tuning range, and phase noise compared to those of the VCO using a conventional cross-coupled transistor layout, respectively. The VCO with the proposed transistor structure shows the phase noise of -113.7 dBc/Hz at 1 MHz, which corresponds to FOM and FOM_T of -190.4 and -194 dBc/Hz, respectively.**

***Index Terms*—CMOS, common-centroid, cross-coupled transistor layout, gain cell layout, low parasitic, voltage-controlled oscillator (VCO).**

I. Introduction

With technology scaling, CMOS technology extends its application into millimeter-wave frequencies. For the micro- and millimeter-wave differential voltage-controlled oscillator (VCO) design, the parasitic in the gain cell (the cross-coupled transistor pair) significantly limits the oscillation frequency, tuning range, and phase noise performances.

De Ranter and Steyaert [1] and Cao and O [2] reported a low-parasitic cross-coupled transistor structure (layout) where the parasitic capacitances are reduced through the proper adjustment in finger width and finger-to-contact space. However, the requirement of two additional drain junctions and the routing parasitic for the interconnection to the output can still significantly limit the VCO performance. Furthermore, the asymmetry in routing and the mismatch in transistor size are the remaining problems that need to be resolved. This letter reports a novel cross-coupled transistor structure (layout), which minimizes parasitic with inherent common-centroid characteristic.

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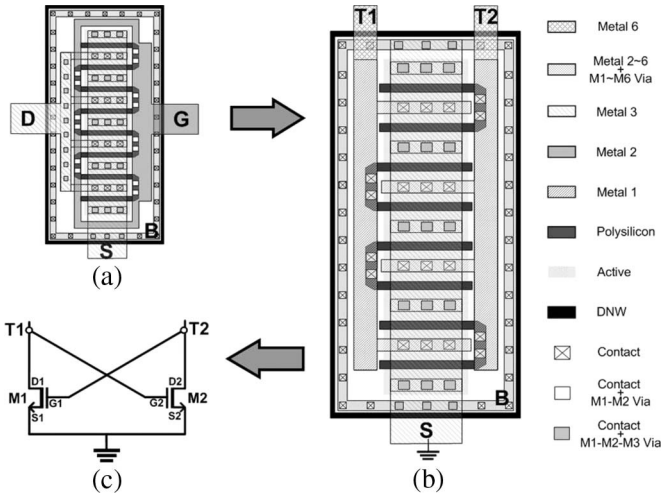

Fig. 1. Conversion of an RF transistor structure. (a) Conventional RF transistor layout, (b) proposed cross-coupled transistor layout, and (c) the corresponding cross-coupled transistor circuit schematic.

II. Common-Centroid Cross-Coupled Transistor

Fig. 1 shows the conversion of a radio-frequency (RF) transistor structure (layout) into the proposed cross-coupled transistor structure and the corresponding circuit schematic. As can be seen from Fig. 1(a) and (b), the RF transistor with eight gate fingers is converted into the cross-coupled transistors M_1 and M_2, with each of them having four gate fingers. In Fig. 1(b), the drain and the four gate fingers of opposite transistors are tied directly through contact and metal-1 layer, and then, the interconnects leave the transistor cell via metal-6 (T1 and T2). As can be seen in Fig. 1(b), the gate–drain cross-connection involves no additional routing and/or overlapping of interconnects. Note that, even in the standard RF transistor cell shown in Fig. 1(a), there is overlap of interconnects between gates and drain fingers. It is confirmed from the PDK file of the given technology that the gate–drain capacitance C_{gd} of the transistor shown in Fig. 1(a) is dominated by the overlap capacitance of the interconnect lines. Although the gate resistance of the proposed transistor increases, C_{gd} reduction is more significant in VCO design since the effective C_{gd} doubles due to the Miller effect degrading transistor f_T and $f_{\max}$, oscillation frequency, and even tuning range. In addition, parasitic resistance reduction from simple routing somewhat compensates for the gate resistance degradation. In Fig. 1(b), since the two cross-coupled transistors (M_1 and M_2) are built on a single standard RF transistor

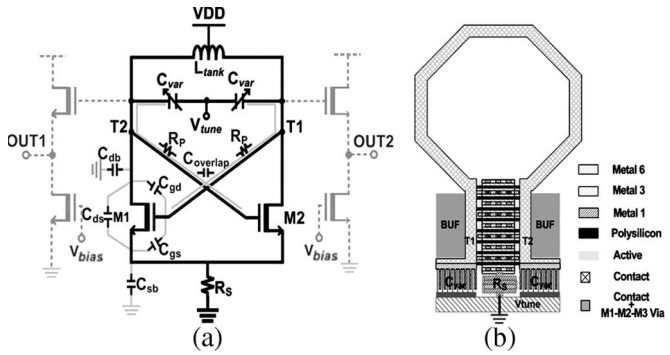

Fig. 2. (a) Circuit schematic of a differential LC-VCO with two buffers. (b) LC-VCO layout with the proposed cross-coupled transistor structure.

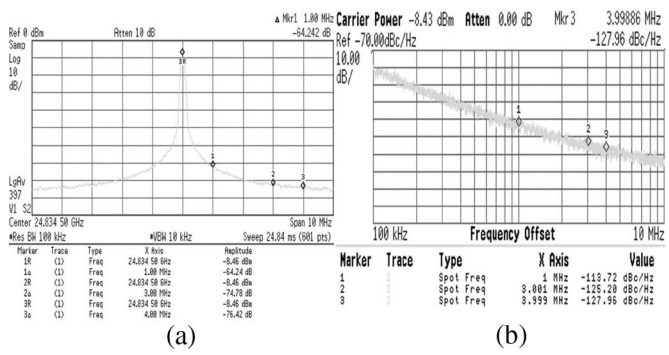

Fig. 3. (a) Measured frequency spectrum. (b) Phase noise of the proposed-transistor-structure-based VCO operating at 24.8 GHz.

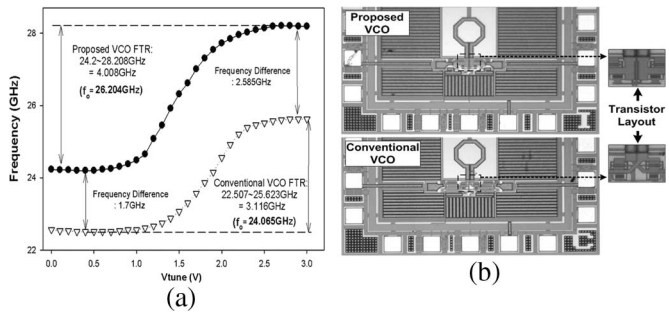

Fig. 4. (a) Measured oscillation frequency versus the control voltage $V_{\rm tune}$ of the two VCOs using the conventional and proposed transistor structures. (b) Microphotograph of the two VCO chips with the proposed and conventional cross-coupled transistor structures.

cell, the overall transistor area becomes smaller, which implies smaller parasitic by itself, by sharing the source, the substrate, the circulating body, and the deep N-well (or P-well for PMOSFETs). Furthermore, the proposed unified transistor structure reduces the number of sources by one compared to the conventional two-unit-transistor-based structure and the drain fingers by two compared to the cross-coupled structure reported in [1] and [2], thus reducing the source- and drain-to-body parasitic capacitances. Moreover, in Fig. 1(b), the gate fingers of transistors $\rm M_1$ and $\rm M_2$ are configured as a common-centroid transistor pair. This symmetry annuls any mismatch arising from the process-induced gradients on the silicon wafer. The proposed cross-coupled transistor pair can be regarded as a three-terminal transistor cell.

III. 26-GHz VCO Design

Fig. 2(a) shows the circuit schematic of a differential LC-VCO. The buffers in Fig. 2(a) (dashed line) are added for measurement purposes only. In Fig. 2(a), the transistor and the routing interconnect parasitic in the VCO core are represented in shaded color, $C_{\rm gs}$, $C_{\rm gd}$, $C_{\rm ds}$, $C_{\rm db}$, $C_{\rm sb}$, $C_{\rm overlap}$, and R_p, respectively.

Two VCOs of given topology are implemented in 0.18-μm CMOS technology, which adopt the conventional and the proposed cross-coupled transistor structure, respectively. As described in the previous section, the LC-VCO using the proposed transistor structure reduces the values for most of the parasitic capacitances that contribute to the reduction of oscillation frequency and tuning range. In Fig. 2(a), the parasitic resistance R_p of the interconnect lines is minimized with the proposed transistor structure, which degrades the quality factor of the LC-tank, leading to phase noise degradation. The common-centroid scheme of the proposed transistor structure is expected to improve the phase noise by the improved symmetry [3].

From the simulation, the two VCOs are designed for 26-GHz operation with $L_{\rm tank} = 625.09$ pH, $C_{\rm var} = 48.68-145.4$ fF, and the transistor size of $20 \times 2 \times 0.18$ μm, respectively. Calculations, based on the transistors' geometry, indicate that the proposed configuration reduces $C_{\rm gd}$ at nodes T1 and T2 by 4.0426 fF. Including the Miller effect, this leads to net capacitance reductions of 16.17 and 8.085 fF for single-ended and differential modes, respectively. Furthermore, $C_{\rm db}$ is reduced by 2.34 fF compared to the transistors reported in [1] and [2]. Considering the relative size of parasitic versus varactor capacitance, the proposed transistor structure is expected to provide considerable increase in oscillation frequency and tuning range. Fig. 2(b) shows the LC-VCO layout with the proposed cross-coupled transistor structure. Note the compactness and symmetry of the VCO layout. The two VCOs are designed to dissipate 7.3 mA from 1.8-V supply.

IV. Measurement Results

Fig. 3 shows the measured frequency spectrum and the phase noise at 24.6 GHz of the VCO with the proposed transistor structure. As can be seen in Fig. 3(a) and (b), a -8.46-dBm output power is measured at each side of the buffer output, and the phase noise of the VCO with the proposed transistor structure at 24.8 GHz shows -113.7 dBc/Hz at 1-MHz offset, which is 4 dB better than that of the VCO with a conventional transistor structure. Fig. 4 shows the measured oscillation frequency versus the control voltage $V_{\rm tune}$, and the microphotograph of the two VCO chips with the proposed and conventional cross-coupled transistor structures. In Fig. 4(a), the operating frequencies of two VCOs are measured over the full varactor tuning range. As can be seen in Fig. 4(a), the VCO with the proposed transistor structure shows more than 2-GHz and 900-MHz (29%) increases in center frequency and tuning range, respectively, compared to those of the VCO with a conventional transistor structure. The FOM and FOM_T of the VCO with the proposed transistor structure are -190.4 and -194 dBc/Hz, respectively [4]. Table I summarizes the measurement results of the VCO with the proposed cross-coupled transistor structure in

TABLE I
SUMMARY OF THE MEASUREMENT RESULTS OF THE VCO WITH THE PROPOSED CROSS-COUPLED TRANSISTOR STRUCTURE IN COMPARISON WITH PRIOR HIGH-FREQUENCY VCOS

Ref.	Technology	f_O [GHz]	V_{DD} [V]	FTR [%]	P_{DC} [mW]	Phase Noise [dBc/Hz]	FOM [dBc/Hz]	FOM_T [dBc/Hz]
This Work	0.18 μm CMOS	**26.2**	**1.8**	**15.3**	**13.1**	**-113.7@1MHz (24.83GHz)**	**-190.4**	**-194**
[1]	0.25μm CMOS	17.4	1.4	8.6	10.5	-108@1MHz	-182.6	-181.3
[2]	0.13 μm CMOS	59	1.5	9.8	9.8	-89@1MHz	-174.5	-174.3
[5]	0.13μm CMOS	26	1.2	23.6	36.5	-96.2@3MHz	-159.3	-166.8
[6]	GaInP/GaAs HBT	17.9	3.0	2.4	4.4	-110.4@1MHz	-189.0	-176.5
[7]	0.15 μm GaAs pHEMT	21.6	5.5	-	30.8	-99.6@1MHz	-170	-
[8]	0.13μm CMOS	5.2	1.5	3.2	7.5	-97@100KHz	-182.6	-172.7

$$FOM = L(f_0) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \qquad FOM_T = L(f_0) - 20\log\left(\frac{f_0}{\Delta f} \times \frac{FTR[\%]}{10}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right)$$

comparison with prior works. Fig. 4(b) shows the microphotograph of the two VCO chips with the proposed and conventional cross-coupled transistor structures. The chip size of both VCOs is 1000×567 μm^2 (290×290 μm^2 for the VCO core).

V. CONCLUSION

In this letter, a low-parasitic and common-centroid cross-coupled transistor structure for high-frequency VCO design is proposed. The design details and featured characteristics are described in comparison with conventional and prior works. A 26-GHz LC-VCO that draws 7.3 mA from 1.8-V supply is designed and implemented in 0.18-μm CMOS technology to exploit the performance advantage of the proposed cross-coupled transistor structure in comparison with the conventional structure. Measurements show improvements in operating frequency, tuning range, and phase noise by 2.1 GHz, 29%, and 4 dB, respectively. The VCO with the proposed transistor structure shows the phase noise of -113.7 dBc/Hz at 1 MHz, which corresponds to FOM and FOM_T of -190.4 and -194 dBc/Hz, respectively.

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