Complex DC-offset cancellation circuit

Y.S. Jang, J.S. Lee, S.G. Lee and J.H. Ko

A novel DC-offset cancellation circuit that is applicable to complex filters is presented. The proposed circuit allows for a high-gain complex filter, which leads to a small chip size and low current consumption. Adopting the proposed scheme, a 10 to 73 dB gain complex filter that cancels an input referred DC-offset by more than ±100 mV is designed based on 0.18 μm CMOS technology, which dissipates 2.4 mA from a 1.8 V supply.

Introduction: Low-IF receiver architectures have been frequently adopted for the increased requirements of high-level integration and lower power consumption in today's wireless communication systems. One of the largest power consuming parts in low-IF receivers is the analogue block, which consists of a variable gain amplifier (VGA) and channel selection filter. Channel selection filters tend to be implemented in image rejection schemes, and complex filters in low-IF architectures. For a smaller chip size and lower power consumption, a complex filter with variable gain control is a preferred technological direction. Furthermore, the current consumption of a complex filter can be reduced by lowering the centre frequency of the filter. However, combining high gain with low centre frequency in a complex filter is limited by the DC-offset problem owing to insufficient gain reduction near DC. The frequency response is represented in Fig. 1, which shows the conditions of high-gain complex integrator frequency responses with and without DC-offset cancellation. R3, R4, C1 and C2 are represented in Fig. 2. As the gain of the integrator gain increases, the gain reduction near DC becomes insufficient, and thus a system can be spoiled by a DC-offset. In order to remove this undesirable situation, the proposed complex DC-offset cancellation circuit (complex-DCOC) is used. Fig. 1 shows that the complex-DCOC sharpens the frequency characteristics near DC. To the best of the authors' knowledge, a DC-offset cancellation circuit for complex filters has not yet been reported. This Letter details a novel DC-offset cancellation circuit for a complex filter, and complex filter design.

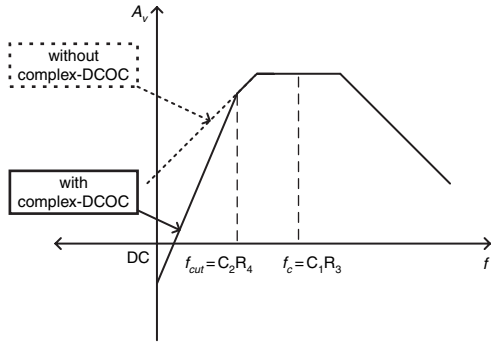

Fig. 1 *Complex filter frequency characteristic with and without complex DCOC*

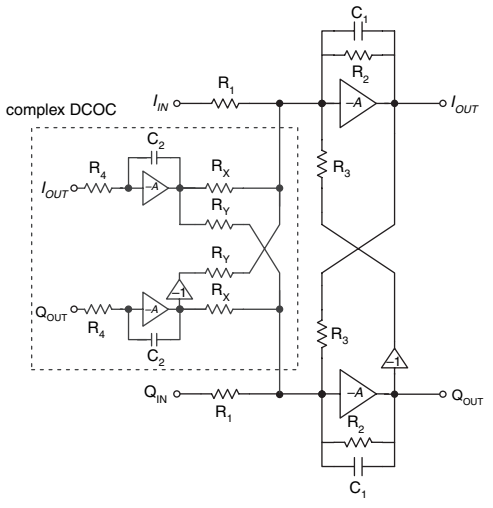

Fig. 2 *Complex integrator with complex DCOC*

Complex DC-offset cancellation circuit: Fig. 3*a* shows a half-circuit of a differential integrator with a conventional DC-offset cancellation circuit (DCOC). In Fig. 3*a*, the DC-offset cancellation is obtained using a negative feedback path with lowpass filtering, which leads to a highpass characteristic of the overall integrator.

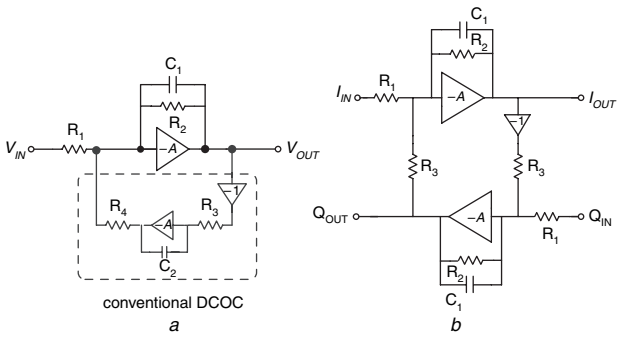

Fig. 3 *Integrator with conventional DCOC and complex integrator*
a Integrator with conventional DCOC
b Complex integrator

The conventional complex integrator without DCOC in Fig. 3*b*, which is drawn in a similar format as in Fig. 3*a*, has two input/output pairs called I and Q, respectively, and cross connections between the input and output of the I/Q nodes. It is well known that a complex integrator's poles are moved through a complex axis in the S-domain and that a band-pass characteristic is obtained based on mathematical analysis. For conceptual analysis, if Q_{in} and Q_{out} paths in Fig. 3*b* are removed, the circuit configuration will be the same as in Fig. 3*a*, which means that Fig. 3*b* also has a DC-offset cancellation characteristic.

As the intermediate frequency is lower, the amount of DC-offset cancellation is insufficient. However, complete DC-offset cancellation in a complex integrator is not possible using a conventional DCOC because complex paths through R_3 make additional DC-offsets, and the added DC-offsets cannot be removed completely using a conventional DCOC. Assuming that the operational amplifier is an ideal one, the quantitative amount of DC-offset in the complex integrator shown in Fig. 3*b* is calculated as:

$$\begin{bmatrix} V_{I,IN}(0) \\ V_{Q,IN}(0) \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{R_2} & \frac{R_1}{R_3} \\ -\frac{R_1}{R3} & -\frac{R_1}{R_2} \end{bmatrix} \begin{bmatrix} V_{I,OUT}(0) \\ V_{Q,OUT}(0) \end{bmatrix} \quad (1)$$

where $V_{I,IN}$ (0) and $V_{Q,IN}$ (0) are the input referred offset voltages, and $V_{I,OUT}$ (0) and $V_{Q,OUT}$ (0) the output offset voltages, at DC. From (1), it is clear that a DC-offset in a complex integrator can be removed if I_{IN} (0) and Q_{IN} (0) are zero.

In Fig. 2, a complex integrator with the proposed complex DC-offset cancellation circuit (complex-DCOC) is presented. The complex-DCOC removes DC-offsets by adding components that can compensate the offset terms in (1). The DC-offset in the circuit in Fig. 1*b* can be represented as:

$$\begin{bmatrix} V_{I,IN}(0) \\ V_{Q,IN}(0) \end{bmatrix} = \left\{ \begin{bmatrix} -\frac{R_1}{R_2} & \frac{R_1}{R_3} \\ -\frac{R_1}{R3} & -\frac{R_1}{R_2} \end{bmatrix} + \begin{bmatrix} \frac{R_1}{R_X} & -\frac{R_1}{R_Y} \\ \frac{R_1}{R_Y} & \frac{R_1}{R_X} \end{bmatrix} \right\} \begin{bmatrix} V_{I,OUT}(0) \\ V_{Q,OUT}(0) \end{bmatrix} \quad (2)$$

From (2), the condition for zeroing the DC-offsets can be drawn as

$$R_X = R_2 \quad (3a)$$

$$R_Y = R_3 \quad (3b)$$

While the resistances of (3a) and (3b) also influence the frequency response of a complex integrator, they should be determined considering both the frequency response characteristics and system requirements of DC-offset cancellation. In other words, smaller R_X and R_Y values provide a larger DC-offset range, but they can distort an integrator's original frequency characteristics owing to its loading effect, and vice versa. The R_X and R_Y values are optimised for the frequency response and DC-offset as described in Fig. 2. Fig. 4 shows the output DC-offset of the designed integrator depending on the intentionally forced input DC-offset. As expected, the system is spoiled without a complex

DCOC when a DC offset exists. From the Figure, it is shown that the output DC-offset is cancelled in spite of a rather large input DC-offset of more than −100 to 100 mV, which is a sufficient range in the target system, ZigBee.

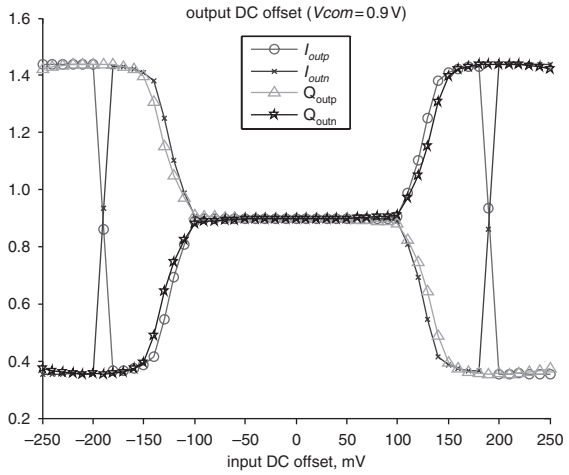

Fig. 4 *DC-offset cancellation results in complex filter*

Filter design: A fourth-order Butterworth-type complex filter with the proposed complex-DCOC is designed for a ZigBee system having a low-IF configuration. The key design issue in a ZigBee system is low power consumption, which can be achieved using a lower-IF and low-power operational amplifier. As a filter is a continuous system, even if second pole and negative zero is under the unit gain frequency, the system's accuracy and stability will not be affected. The feed forward compensation technique [1, 2], rather than the Miller compensation, is an attractive choice. In this design, the modified amplifier of [2] is used. Normally, a 10 to 73 dB controllable gain is obtained with a two-stage PGA or VGA in a complex system. However, along with a complex DCOC, this system uses only a one-stage PGA having a gain of 0 to 15 dB with 1 dB steps, and a complex filter having a gain of 10 to 58 dB with 12 dB steps.

Conclusion: A complex DC offset cancellation circuit (complex-DCOC) is proposed. The proposed complex-DCOC can remove the DC-offset in a complex integrator, which allows a complex filter to have a high gain, thereby making the analogue block of a low-IF receiver very efficient. The designed integrator, adopting the proposed complex-DCOC, cancels DC-offset when the input offset is around −100 to 100 mV. An image rejection filter with a complex-DCOC for application in a ZigBee system is designed based on 0.18 μm CMOS technology. The designed filter has a fourth-order Butterworth configuration and shows 10 to 73 dB controllable gain with DC-offset cancellation. Therefore, owing to the complex-DCOC, a system can be implemented with low power by removing the need for an additional PGA with a high-gain complex filter.

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