A Binary-Weighted Switching and Reconfiguration-Based Programmable Gain Amplifier

Huy-Hieu Nguyen, Hoai-Nam Nguyen, Jeong-Seon Lee, and Sang-Gug Lee, *Member, IEEE*

***Abstract*—In previous works, the authors reported on binary-weighted switching and reconfiguration techniques to design programmable gain amplifiers (PGAs) with a wide decibel (dB)-linear range, a small gain error, a wide 3-dB bandwidth, and high linearity. In this brief, two techniques are analyzed in more detail. Adopting the two techniques, a new low-voltage PGA version is proposed that offers a precise and process/temperature-insensitive gain and achieves a double dB-linear range with a small gain error while maintaining the same chip size, as compared with those of previous designs. Implemented in 0.18-μm CMOS, from the measurements, the proposed PGA shows a dB-linear gain range of 42 dB (-21 to 21 dB) with a gain error of less than ± 0.54 dB, a maximum input-referred third-order intercept point (IIP3) of 14 dBm, and a 3-dB bandwidth of 60 MHz at the maximum gain while consuming only 2.1 mA from a 1.5-V supply.**

***Index Terms*—Decibel (dB)-linear gain, digitally controlled variable-gain amplifier (VGA), programmable gain amplifier (PGA), reconfiguration.**

I. Introduction

THE automatic gain control (AGC) circuit is an important building block of many systems. A function of the AGC loop, particularly in wireless applications, is to automatically adjust the gain of the receiver path so that the signal at the input of the analog-to-digital converter appears constant, regardless of the signal level at the antenna. A variable-gain amplifier (VGA) is a key block of AGC loops that are based on both feedback [1] and feedforward [2] approaches. While many high-performance VGAs have successfully been implemented with a continuous-mode gain variation [3], [8], with most applications, the VGAs are controlled by various digital circuitries or digital signal processing units. Therefore, digitally controlled VGAs [i.e., programmable gain amplifiers (PGAs)] save the need for auxiliary digital-to-analog converters.

Fig. 1 shows the reported PGA architectures. In Fig. 1(a), the voltage gain of the inverting amplifier is digitally varied by the digital control of the input and feedback resistor values [4]. The variation of input and output impedances is a disadvantage of this method. Some people have tried to solve the impedance problem by adopting a current division network (CDN), as shown in Fig. 1(b) [5]. The voltage gain of VGAs in resistive feedback architectures, as shown in Fig. 1(a) and (b), depends on the ratio between the feedback and input resistors. Thus, it is accurate and insensitive to process and temperature variations. However, although resistive feedback amplifiers usually provide high linearity, they are not suitable for high-frequency applications due to the large current required by high-frequency operational amplifiers. For high-frequency applications, open-loop amplifiers using the variable input g_m [6] or output loads [7], as shown in Fig. 1(c) and (d), respectively, are popular. However, the voltage gain $g_m R_L$ of these amplifiers is sensitive to process and temperature variations. Moreover, they require a large number of switches for the small step size, leading to higher complexity.

VGAs with diode-connected loads and bias current variation [8], as shown in Fig. 1(e), provide a voltage gain that is insensitive to process/temperature variations. From Fig. 1(e), the voltage gain of the VGA cell can be expressed as

$$A_V = \frac{g_{m\text{-input}}}{g_{m\text{-load}}} = \sqrt{\frac{(W/L)_{\text{input}}}{(W/L)_{\text{load}}} \times \frac{I_{C1}}{I_{C2}}} \tag{1}$$

where $g_{m\text{-input}}$ is the transconductance of the input differential pair, and $g_{m\text{-load}}$ is the transconductance of the diode-connected load transistors. From (1), the voltage gain is not sensitive to process/temperature variations but only depends on the ratios of the transistor size and their bias currents. In [8], the ratio $(W/L)_{\text{input}}/(W/L)_{\text{load}}$ is fixed, and the gain is controlled by only varying the bias current ratio I_{C1}/I_{C2}, along with a new pseudoexponential function that extends the decibel (dB)-linear range. However, the proposed function is difficult to apply to VGAs with a discrete-type gain variation. In [8], the current density of the input and diode-connected load transistors is changed with the gain variation. Therefore, at low gains, the input transistors operate at a low current density, which leads to poor amplifier linearity [12].

In [9], the authors have introduced a PGA based on the architecture shown in Fig. 1(e), which adopts a binary-weighted transistor size switching that extends the gain range and maintains good linearity at low gains. In Section II of this brief, the binary-weighted switching technique is analyzed in more detail. In [10], by adopting the binary-weighted switching and reconfiguration techniques, the authors have reported on a PGA that extends the dB-linear range while saving on power consumption and chip size. In Section III, the reconfiguration technique is discussed. In Section IV, adopting the two techniques,

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The authors are with the u-Radio laboratory, Korea Advanced Institute of Science and Technology, Daejeon 305-714, Korea (e-mail: huyhieu@icu.ac.kr).

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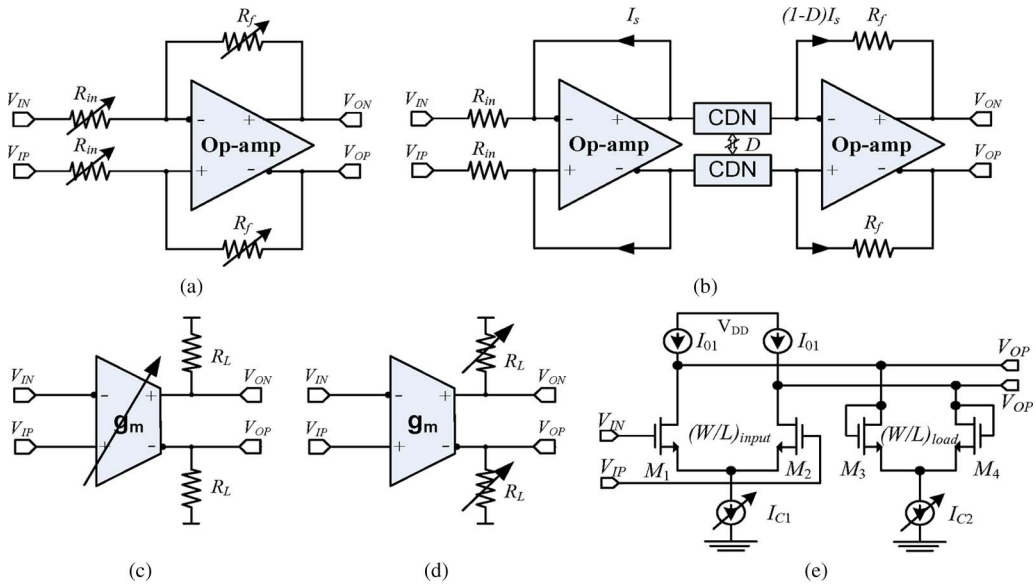

Fig. 1. PGA architectures with (a) resistive feedback, (b) resistive feedback with the CDN, (c) variable g_m, (d) variable load, and (e) diode-connected load and bias current variation.

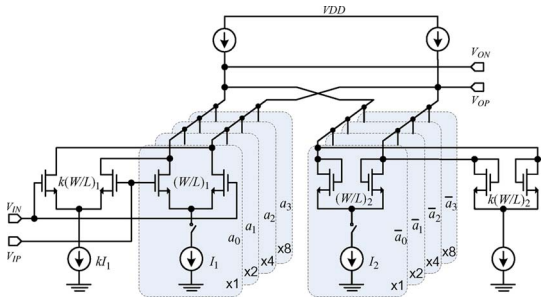

Fig. 2. Schematic of the binary-weighted switching technique-based PGA.

a new low-voltage PGA is proposed, which offers a precise process/temperature-insensitive gain characteristic and doubles the dB-linear range of [9], with a small gain error while maintaining the same chip size as in [9] and [10]. Section V presents the measurement results of the proposed PGA, and conclusions are given in Section VI.

II. Binary-Weighted Switching Technique

The key idea of the binary-weighted switching technique is to simultaneously vary the size and bias current of the input and load transistors of the amplifier using binary-weighted transistor arrays. With this method, the current densities of the input and load transistors are fixed while varying the voltage gain, therefore keeping a constant overdrive voltage ($V_{\rm GS} - V_{\rm TH}$). Thus, the amplifier provides better linearity compared with the case of varying the current densities of the input/load transistors, as reported in [8] and [12].

The schematic of a PGA cell adopting the binary-weighted switching technique is shown in Fig. 2. As shown in Fig. 2, the input g_m stage and the diode-connected load consists of an array of switchable transistor pairs in parallel. Each unit of the array is composed of a transistor pair, a current tail, and a switch for activation/deactivation. In Fig. 2, the units with THE multiplication factor k are not switched but stay ON. Note that, in Fig. 2, except for the units with the multiplication factor k, the units with the multiplication factor i $(i = 1, 2, 4, 8)$ in the two arrays do not turn ON or OFF at the same time. Thus, by changing the control bits $a_0, a_1, \ldots$, the transconductance values of the input g_m and the diode-connected load can conversely be varied and are expressed as

$$g_{m\text{-input}} = \sqrt{2\mu_n C_{ox}(W/L)_1 I_1} \times (2^0 a_0 + 2^1 a_1 + 2^2 a_2 + 2^3 a_3 + k) \quad (2)$$

$$g_{m\text{-load}} = \sqrt{2\mu_n C_{ox}(W/L)_2 I_2} \times (2^0 \overline{a}_0 + 2^1 \overline{a}_1 + 2^2 \overline{a}_2 + 2^3 \overline{a}_3 + k) \quad (3)$$

where a_i (0 or 1) is the digital control bit, and k is the constant for adjusting the gain range.

Using (2) and (3), the differential voltage gains of the PGA shown in Fig. 2 can be given by

$$A_V = \frac{g_{m\text{-input}}}{g_{m\text{-load}}} = \beta \frac{2^0 a_0 + 2^1 a_1 + 2^2 a_2 + 2^3 a_3 + k}{2^0 \overline{a_0} + 2^1 \overline{a_1} + 2^2 \overline{a_2} + 2^3 \overline{a_3} + k} = \beta \frac{x + k}{2^4 - 1 - x + k} \quad (4)$$

where $x = 2^0 a_0 + 2^1 a_1 + 2^2 a_2 + 2^3 a_3$ is the digital control word, and $\beta = \sqrt{(W/L)_1 I_1}/\sqrt{(W/L)_2 I_2}$ is a constant. Using four control bits, when x varies from 0 $(a_3 a_2 a_1 a_0 = 0000)$ to 15 $(a_3 a_2 a_1 a_0 = 1111)$, by defining $t = (x - 7.5)/(k + 7.5)$, the voltage gain in (4) varies following the squared pseudoexponential function $A_v = \beta(1 + t)/(1 - t) \approx \beta e^{2t}$, whereas the gain variation scheme reported in [8] follows the pseudoexponential function $e^t \approx [(1 + t)/(1 - t)]^{1/2}$ by only changing the ratio of bias currents I_{c1}/I_{c2} shown in Fig. 1(e). The squared pseudoexponential function can provide twice the dB-linear gain range compared with the conventional pseudoexponential function. The voltage gain versus the control word that follows (4) with $\beta = 1$ is shown in Fig. 3 for various k values. As shown in Fig. 3, the dB-linear range varies as a function of the value of k. The dB-linear range can be extended up to 31 dB with a gain error of less than ± 0.85 dB. Another advantage of the binary-weighted switching technique is a scaleable gain step. In other gain control techniques, to reduce the gain step by half, the number of switches is normally doubled [4], increasing the

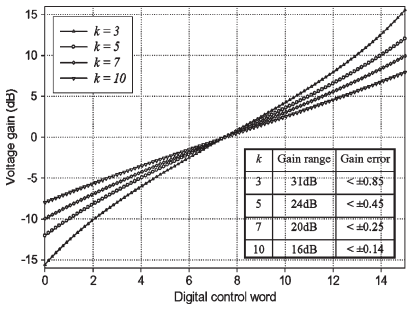

Fig. 3. Voltage gain versus control word of (4) with different k-factors.

complexity and degrading the performance due to the parasitic added from the switches. Whereas in the proposed switching technique, the size of the gain step can easily be reduced by inserting one or more units with the equivalent number of increasing control bits in the input/load array using the corresponding multiplication factor, which does not degrade performances of the PGA. Moreover, the gain variation range of the PGA can be shifted up or down by changing the constant β. With all the aforementioned advantages, the binary-weighted switching technique can be considered as a flexible and simple method to design a wide dB-linear range and a high-linearity PGA.

III. Reconfiguration Technique

VGAs typically use many gain stages to satisfy the required wide dynamic range [4], [5], [8]. However, the use of many gain stages with a large number of switches results in a big chip size or a high cost. The PGA topology reported in [9] combines one VGA cell with three fixed-gain amplifiers (FGAs) to achieve an 84-dB gain range. The adoption of FGAs allows a smaller chip size and lower power dissipation compared with those of a conventional topology. However, in principle, a wider dB-linear range in each gain stage allows for a smaller chip size, lower noise, and lower circuit complexity.

In [10], the authors introduced a reconfiguration technique in combination with the binary-weighted switching technique that doubles the gain range of the single-stage PGA while saving on power consumption by half and maintaining nearly the same chip size and gain error compared with those of the PGA cell reported in [9]. Fig. 4 shows the circuit schematic of the PGA reported in [10]. In Fig. 4, the input and load transistor pairs are implemented in a complementary combination. Depending on the logic level of the most significant bit (MSB), the PMOS or NMOS transistor pairs switch the roles of the input or diode-connected transistors, respectively. As shown in Fig. 4, the PMOS and NMOS input transistor configurations provide the lower and upper halves of the gain, respectively, doubling the gain range compared with that of [9]. In Fig. 4, compared with the PGA reported in [9], the current consumption is reduced by half since the bias currents for NMOS transistors are reused for the PMOS transistors. However, by stacking four transistors, the output swing is degraded, limiting the application for a low supply voltage. Moreover, the voltage gain depends on the NMOS and PMOS transistor mobility, i.e., μ_n and μ_p, respectively, leading to process and temperature dependence. The following section introduces a modified PGA that corrects the aforementioned deficiencies.

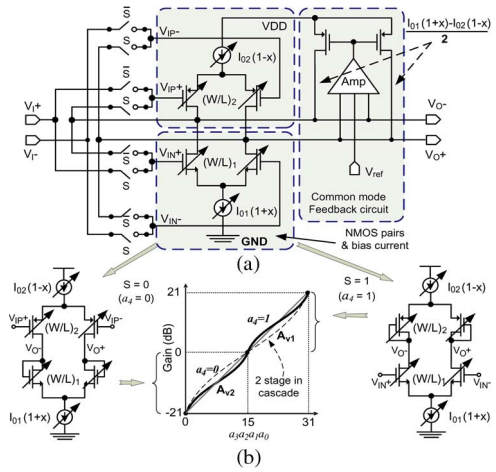

Fig. 4. Reconfiguration-technique-based PGA with a complementary transistor combination. (a) PGA schematic. (b) Each configured PGA schematic and its corresponding gain range.

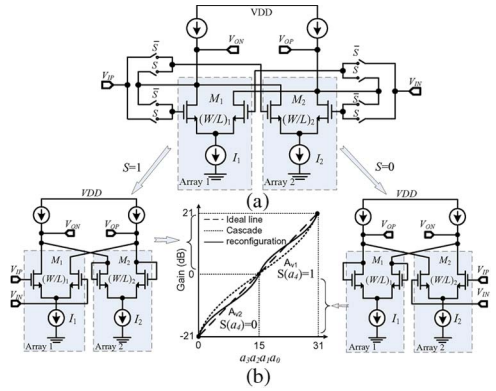

Fig. 5. Modified reconfiguration-technique-based PGA. (a) Overall PGA schematic. (b) Schematics of each configured PGA and the corresponding gain ranges.

IV. All-NMOS Reconfiguration-Based PGA

Fig. 5 shows a schematic of an all-NMOS reconfiguration-technique-based PGA. In Fig. 5, the reconfiguration involves NMOS transistors only, where the role of transistor arrays 1 and 2 are swapped between the input and load stages. Assuming $I_1 > I_2$ and $(W/L)_1 > (W/L)_2$, with $S = 1$, array 1 serves as the input g_m stage and array 2 as the diode-connected load, providing high gain levels, whereas with $S = 0$, the role of arrays 1 and 2 are swapped, providing low gain levels. Fig. 5(b) shows each configured circuit schematic and its corresponding gain variation range. Note that the reconfiguration doubles the gain range, whereas the gain error is not doubled, that is, compared with the case of doubling the gain range by the cascade of two gain stages (the dot-dot line). Compared with the complementary transistor reconfiguration, the all-NMOS reconfiguration is suitable for low supply voltage applications since only three transistors are stacked from the supply to the ground.

The temperature compensation circuit in conventional CMOS-based VGAs is usually realized using parasitic bipolar transistors or MOS transistors in the subthreshold region operation; however, the models for these transistors are not accurate [3], [11]. Using the binary-weighted switching and the modified reconfiguration technique (Fig. 5), the PGA gain becomes process and temperature independent. Compared with the binary-weighted transistor array-based PGA reported in

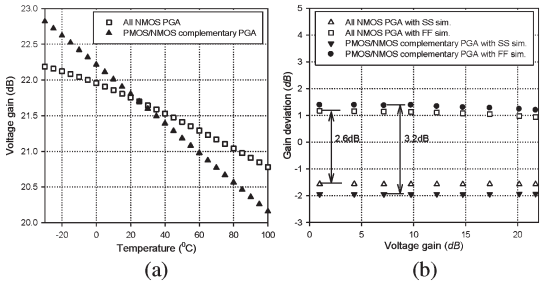

Fig. 6. (a) Simulated gain versus temperature at the highest gain setting. (b) Gain deviation with SS and FF corner simulation settings.

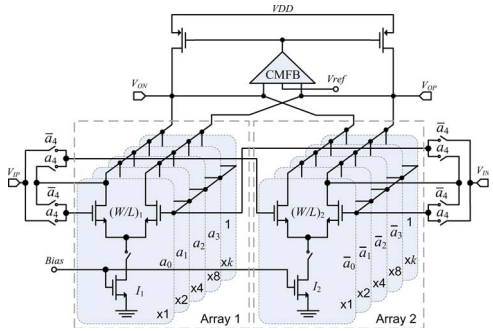

Fig. 7. Complete schematic of the proposed 5-bit PGA.

[9] or a PGA based on complementary transistor arrays using the reconfiguration technique [10], the newly proposed all-NMOS transistor array-based reconfigurable PGA offers performance advantages in terms of gain range, chip size, process/temperature independence, and low voltage operation. However, due to the additional parasitic capacitance of switches, which are used to change the roles of the arrays 1 and 2, at the output nodes, the proposed PGA shown in Fig. 5 offers the 3-dB bandwidth smaller than that of the PGA shown in Fig. 2. Thus, the sizes of the switches should be small to minimize their effect.

Fig. 6(a) shows the simulated gain versus temperature of the all-NMOS PGA shown in Fig. 5 and the PMOS/NMOS complementary PGA shown in Fig. 4. The all-NMOS PGA and the PMOS/NMOS complementary PGA show the gain deviations of 1.4 and 2.6 dB, respectively, over the temperature range of -30 °C to 100 °C. Fig. 6(b) shows the gain deviation with Slow Slow (SS) and Fast Fast (FF) corner simulations compared to typical conditions. The all-NMOS PGA shows a 0.6-dB less gain variation than that of the PMOS/NMOS complementary PGA.

Fig. 7 shows the complete circuit schematic of a 5-bit PGA with the modified reconfiguration technique. In Fig. 7, four least significant bits (LSBs), i.e., $a_3a_2a_1a_0$, are used for the size control of differential input/diode-connected load pairs and their bias currents, and one MSB, i.e., a_4, is used for swapping the role of the transistor arrays. Similar to (4), the differential voltage gains of the proposed VGA can be given by

$$\begin{aligned} A_{V1} &= \sqrt{\frac{(W/L)_1 I_1}{(W/L)_2 I_2}} \\ &= \beta \frac{2^0 a_0 + 2^1 a_1 + 2^2 a_2 + 2^3 a_3 + k}{2^0 \overline{a_0} + 2^1 \overline{a_1} + 2^2 \overline{a_2} + 2^3 \overline{a_3} + k} \\ &= \beta \frac{x + k}{2^4 - 1 - x + k} \end{aligned} \tag{5}$$

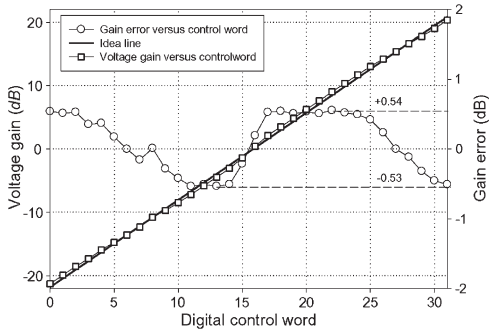

Fig. 8. Measured gain and gain error versus control word.

$$\begin{aligned} A_{V2} &= \sqrt{\frac{(W/L)_2 I_2}{(W/L)_1 I_1}} \\ &= \left(\frac{1}{\beta}\right) \frac{2^0 \overline{a_0} + 2^1 \overline{a_1} + 2^2 \overline{a_2} + 2^3 \overline{a_3} + k}{2^0 a_0 + 2^1 a_1 + 2^2 a_2 + 2^3 a_3 + k} \\ &= \left(\frac{1}{\beta}\right) \frac{2^4 - 1 - x + k}{x + k} \end{aligned} \tag{6}$$

where A_{V1} and A_{V2} are the two gains shown in Fig. 5(b), $a_4 = 1$ and $a_4 = 0$, respectively. The constant $k = 5$ is chosen so that A_{V1} and A_{V2} cover each 21 dB of gain range, respectively, and β is chosen so that no overlap occurs between the gain variation range of A_{V1} and A_{V2} [see Fig. 5(b)]. As x (the decimal value of four LSBs) varies from 0 to 15, A_{V1} and A_{V2} vary over a range of -21 to 0 dB and 0 to 21 dB, respectively, which is an overall range of 42 dB (-21 to 21 dB) with 1.31-dB steps. The proposed PGA topology can be implemented with a larger number of control bits for a smaller gain step. As in [9], the current density of the input and diode-connected load transistors of the proposed PGA cell is kept constant over the gain variation. Hence, a similar linearity performance as that of the PGA cell reported in [9] is expected. Furthermore, the chip area of the proposed PGA cell is approximately equal to that of [9] and [10] since the numbers of transistors in all three PGA cells are nearly the same.

In Fig. 7, the common-mode feedback circuit (CMFB) that is similar to the one reported in [8] is used for maintaining a constant output dc voltage. To exploit a low-voltage operation, the proposed PGA is designed using a 1.5-V supply.

V. Measurement Results

The single-stage PGA shown in Fig. 7 is fabricated in a 0.18-μm CMOS process and dissipates an average current of 2.1 mA from a 1.5-V supply. Fig. 8 shows the measured gain and gain error versus control words at 50 MHz. In Fig. 8, the proposed PGA shows a dynamic gain range of 42 dB (-21 to 21 dB) and a maximum gain error of less than ± 0.54 dB. The measured input-referred third-order intercept point (IIP3) and the 1-dB compression point (P1dB) are -11.5 to 14 dBm and -15 to -5 dBm, respectively, as shown in Fig. 9. Fig. 10 shows the measured gain for ten different prototypes. As shown in Fig. 10, the maximum gain deviation over ten prototypes is less than 1.7 dB. Fig. 10 shows the measured gain versus control words at operating temperatures of 0 °C, 25 °C, 50 °C, 75 °C, and 100 °C. In Fig. 11, the maximum gain deviation over 0 °C to 100 °C is less than 0.85 dB. The 3-dB bandwidths at

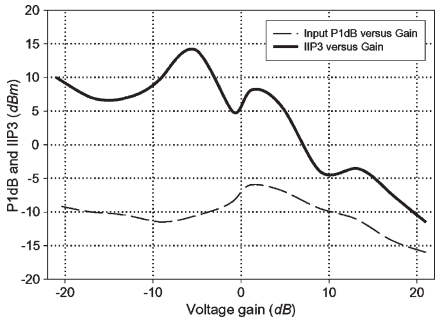

Fig. 9. Measured IIP3 and P1dB versus gain.

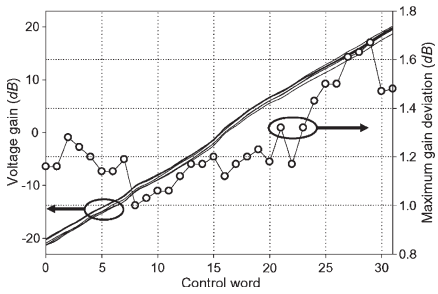

Fig. 10. Measured gain versus control word of ten prototypes and the gain deviation.

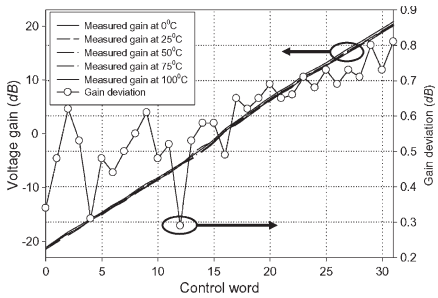

Fig. 11. Measured gain versus control word over the temperature variation and the gain deviation.

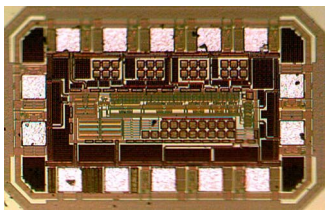

Fig. 12. Microphotograph of the proposed PGA chip.

voltage gains of 21, 0, and −21 dB are measured as 60, 160, and 950 MHz, respectively. From the measurement, the PGA shows a noise figure of less than 15 dB at the maximum gain of 21 dB. The microphotograph of the proposed PGA chip is shown in Fig. 12. The PGA, excluding bond pads, occupies less than 0.078 mm^2 of chip area. The performance is compared with [3], [10], and [11], which is shown in Table I.

VI. Conclusion

In this brief, two previously reported PGA gain control schemes have been reviewed in more detail, namely, binary-weighted and reconfiguration switching techniques. Adopting these same techniques, a new low-voltage and temperature/process-insensitive PGA has been proposed. The proposed compact 5-bit PGA implemented in 0.18-μm CMOS technology shows a dB-linear gain range of 42 dB (−21 to 21 dB) with a gain error of less than ±0.54 dB, a bandwidth of 60 MHz at the maximum gain of 21 dB, a noise figure of less than 15 dB at a 21-dB gain, an occupied chip area of 0.078 mm^2, and IIP3 and P1dB of −11.5 to 14 dBm and −15 to 5 dBm, respectively, while consuming an average current of 2.1 mA from a 1.5-V supply. Small gain deviations of 0.85 and 1.7 dB were measured over a temperature range of 0 °C to 100 °C and over ten prototypes, respectively.

TABLE I
PGA Performance Comparison

	This work	[3]	[10]	[11]	Units
Technology	*0.18μm CMOS*	0.13μm CMOS	0.18μm CMOS	0.8μm bipolar	-
Power consumption	*3.2 /1.5*	20.52 /1.8	1.4 /1.8	16.2 /2.7	mW /V
Gain range /gain step	*(-21~21) /1.31*	(38.8~55.3) /-	(-21~21) /1.31	(-70~7) /-	dB /dB
Gain error	*< ±0.54*	< ±3	< ±0.55	< ±1.5	dB
Bandwidth	*60*	900	84	400	MHz
IIP3	*-11.5~14*	-59.1~ -10.8	-9~14	-	dBm
P1dB	*-15~-5*	-	-21.5~-9	-6.8@7dB gain	dBm
Gain deviation over temp.	*< 0.85*	< ±3.0	<1.35	< ±1.5	dB
Gain deviation over 10 chips	*< 1.7*	-	-	-	dB
Die area	*0.078*	0.42	0.05	1.11	mm^2

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