Current-Reused Ultra Low Power, Low Noise LNA+Mixer

Viet Hoang Le, Seok-Kyun Han, Jeong-Seon Lee, and Sang-Gug Lee, *Member, IEEE*

***Abstract*—A current-reused ultra low power, low flicker noise direct-conversion low noise amplifier (LNA)+mixer architecture is proposed. Measurements of the proposed LNA+mixer applied for 2.4 GHz Zigbee system using 0.18 μm CMOS technology shows 21 dB voltage gain, 6 dB noise figure, and approximately 300 KHz flicker noise corner frequency while dissipating 0.9 mA from a 1.8 V supply.**

***Index Terms*—Current reused, low noise amplifier (LNA)+mixer, low flicker noise, low power receiver.**

I. Introduction

TODAY, the implementation of various wireless communication systems demand longer battery life, which motivates development of low power transceivers. The IEEE 802.15.4 is a good example of a standard that requires a very low power transceiver. The applications of the IEEE 802.15.4 are home automation, sensor networks, personnel health care, and games, which require minimized transceiver power dissipation.

In the last few years, several low-power receiver implementations have been reported [1]–[3]. However, their power dissipations are still too high. The low power receiver front-end reported in [4] and [5] adopts a passive mixer that consumes no dc current. However, due to the conversion loss and the low input impedance of the passive mixer [4], [5], a high Q-factor external inductor is adopted at the output of the LNA. Furthermore, the passive mixer requires large LO swing, which leads to higher power dissipation in the LO buffer.

This letter presents the design and implementation of a low power receiver front-end for 2.4 GHz IEEE 802.15.4, where the bleeding current of the mixer is reused for the LNA. The proposed architecture can easily adopt inductor 1/f noise suppression in the mixer.

II. Circuit Description

Fig. 1 shows the proposed LNA+mixer architecture. As shown in the figure, the LNA is implemented by re-using the bleeding current of the mixer. The bleeding helps to improve the conversion gain of the mixer [6]. In the LNA, the value for

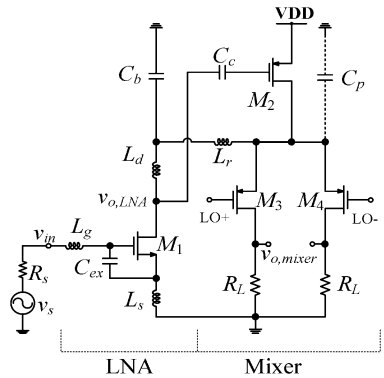

Fig. 1. Proposed LNA+Mixer architecture.

L_g, C_{ex} and L_s, as well as the size of M_1 and the gate-source voltage, are chosen following the design principle of the power-constrained simultaneous noise and input matching technique described in [7]. C_b and C_c are the bypass and coupling capacitors, respectively. In Fig. 1 the value of L_r is chosen to resonate at the LO frequency with the parasitic capacitance C_p at the common-source node of the mixer switching transistors M_3 and M_4. The $L_r - C_p$ resonance helps to suppress the 1/f noise at the mixer output [8], [9].

For the given power-constrained simultaneous noise and input matched LNA, it can be shown that the voltage gain of the LNA is independent of the transconductance g_{m1} of the input transistor M_1. Fig. 2 shows the simplified small-signal equivalent circuit of the LNA shown in Fig. 1. By applying the Kirchoff's voltage law at the input

$$v_{\rm in} = s^2 C_t (L_g + L_s)\frac{i_d}{g_{m1}} + \frac{i_d}{g_{m1}} + sL_s i_d \tag{1}$$

where $C_t = C_{gs} + C_{\rm ex}$, and $i_g, i_s, i_d, g_{m1}, L_g, L_s, C_{\rm gs}, C_{\rm ex}$ are described in Fig. 2. From the matched input condition [7]

$$s^2 C_t (L_g + L_s) = -1. \tag{2}$$

Therefore, from (1) and (2) the drain current of the LNA transistor M_1 can be given as

$$i_d = \frac{v_{\rm in}}{j\omega_0 L_s}. \tag{3}$$

Now, the value of L_d can be chosen to resonate with the parasitic capacitance at the LNA output. Assuming the Q-factor of the L_d in parallel with the LNA output parasitic capacitance is dominated by the Q-factor of L_d, the effective LNA load impedance at the frequency of resonance ω_o can be expressed as

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The authors are with the u-Radio Lab., Korea Advanced Institute of Science and Technology, Korea (e-mail: hoangle@icu.ac.kr).

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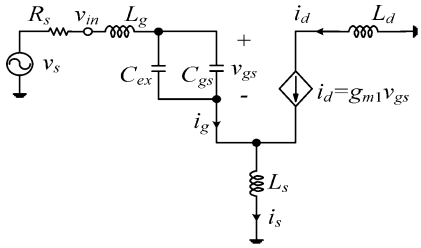

Fig. 2. Simplified small-signal equivalent circuit for the LNA part.

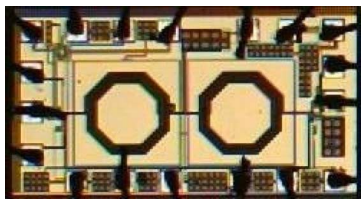

Fig. 3. Micophotograph of the fabricated LNA+mixer.

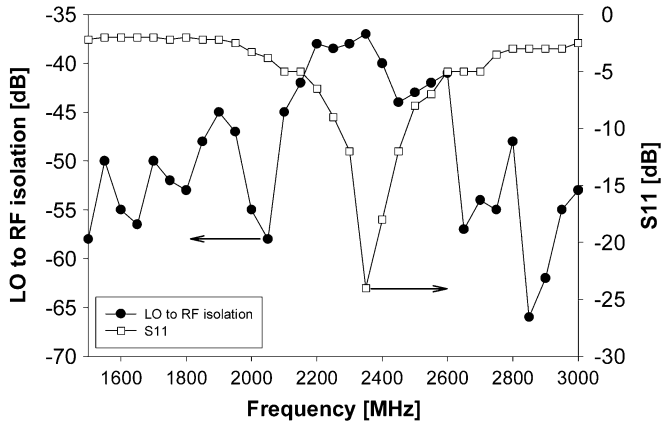

Fig. 4. S11 and LO to RF isolation of the measured LNA+mixer.

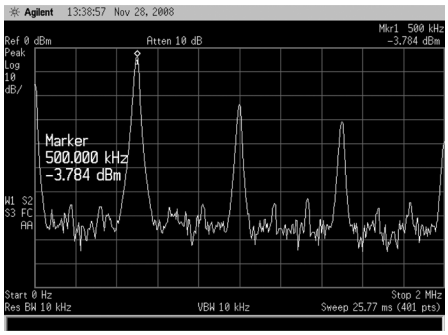

Fig. 5. Output baseband spectrum of the measured LNA+mixer.

$R_{o,\mathrm{LNA}} = \omega_o L_d Q_{Ld}$, where Q_{Ld} is the Q-factor of L_d. Therefore, with i_d from (3) the LNA output voltage can be given by

$$v_{o,\mathrm{LNA}} = i_d R_{o,\mathrm{LNA}} = \frac{v_{\mathrm{in}} L_d Q_{L_d}}{jL_s}. \tag{4}$$

Thus, from (1), (2), and (4), the voltage gain of the LNA is given as

$$A_{\mathrm{LNA}} = \left| \frac{v_{o,\mathrm{LNA}}}{v_{\mathrm{in}}} \right| = \frac{L_d Q_{L_d}}{L_s}. \tag{5}$$

The conversion voltage gain of the mixer can be given by [6]

$$A_{\mathrm{mixer}} = \frac{2}{\pi} g_{m2} R_L. \tag{6}$$

Therefore, the overall voltage conversion gain of the LNA+mixer is given by

$$A_c = A_{\mathrm{LNA}} A_{\mathrm{mixer}} = \frac{2}{\pi} g_{m2} R_L \frac{L_d Q_{L_d}}{L_s}. \tag{7}$$

From (7) and Fig. 1, it can be seen that the overall conversion gain of the LNA+mixer is independent of the transconductance g_{m1} of the LNA, g_{m2} is maximized by drawing the total supply current, and the bleeding through the LNA allows higher R_L for the mixer, all of which helps to increase the conversion gain of the LNA+mixer while dissipating least amount of current. However, the linearity requirement sets a constraint on the minimum value of g_{m1} which limits the minimum current consumption. When the matching condition holds, that is $R_s = (g_{m1}L_s)/(C_{\mathrm{gs}})$ or $g_{m1} = (R_s C_{\mathrm{gs}})/(L_s)$, the gain from the signal source to the gate of input transistor M_1 is equal to the quality factor of the input matching network, as

$$Q_{\mathrm{in}} = \frac{v_{\mathrm{gs}}}{v_s} = \frac{1}{R_s} \frac{1}{\omega C_{\mathrm{gs}}} = \frac{1}{\omega g_{m1} L_s}. \tag{8}$$

If g_{m1} is decreased, and L_s is kept the same so as to avoid changing the voltage gain of the LNA as described in (7), the gain provided by the matching network Q_{in} will increase. As a result, the gate-to-source ac voltage of M_1 increases, and thus the LNA linearity decreases. Reducing the dc bias current or W/L of the input transistor M_1 to reduce g_{m1} increases the gain by the matching network and degrades the linearity of the LNA. Reducing the gate-source bias voltage of the input transistor M_1 degrades the linearity further, as M_1 operates at a higher third order component value [10].

As suggested by [7], the additional capacitance C_{ex} and the degeneration inductance L_s are chosen to achieve simultaneous noise and input matching, satisfying the condition $(g_{m1}L_s)/(C_{\mathrm{ex}} + C_{\mathrm{gs}}) = R_s$. Large C_{ex} lowers Q_{in}. As a result, input matching can easily be achieved over a wide frequency range; however, the overall gain is reduced and the minimum noise increases since a larger L_s is needed [7]. If C_{ex} is small, Q_{in} increases, causing the matching to occur over a narrow frequency band. Moreover, the linearity of the LNA is degraded due to the higher gain provided by the matching network. The size of C_{ex} should be chosen considering the gain, noise figure, linearity and matching [7].

For the on-chip spiral inductors with quality factor Q_{Ld} of 7–10, L_d of about 10 nH, L_s of smaller than 2 nH, R_L of 500–1000 Ohm and with very small g_{m2} of several mS, the proposed LNA+mixer can provide 20–30 dB of voltage conversion gain. Therefore, the small g_{m2} allows the overall current dissipation to be lower than 1 mA. Furthermore, the proposed LNA+mixer provides low noise figure, through the power-constrained simultaneous noise and input matched LNA design as well as the 1/f noise suppression at the mixer output by the $L_r - C_p$ resonance.

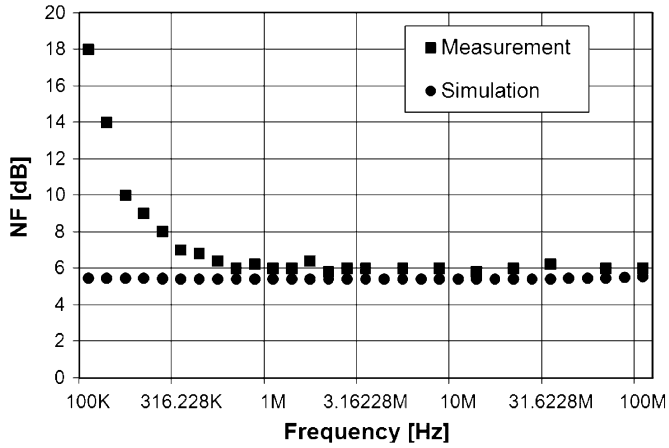

Fig. 6. Measured and simulated noise figure of the proposed LNA+mixer.

III. Measurement Results

The proposed LNA+mixer architecture is fabricated in 0.18 μm CMOS technology, and occupies an active area of 0.8 mm^2 including pads. The microphotograph of the LNA+mixer is shown in Fig. 3, all the components, indicated in Fig. 1, are implemented on-chip except the input matching inductor L_g. The measured LNA+mixer dissipates an average current of 0.9 mA at 1.8 V. The input return loss and forward transmission between the LO and RF ports are shown in Fig. 4. Fig. 5 shows the output baseband spectrum of the measured LNA+mixer; the baseband power at 500 KHz is -3.8 dBm while applying 2.4 GHz RF signal at the power of -25 dBm and an LO signal of 2.4005 GHz at the power of 0 dBm. The conversion gain is 21 dB. The measured noise figure is about 6 dB with 1/f noise corner of approximately 300 KHz, as shown in Fig. 6, together with simulated result. The measured result agrees quite well with the simulated result except at low frequency. The discrepancy between the measured and simulated noise figures can be explained by inaccurate estimation of the parasitic capacitance seen at the common source of the switching pairs M_3, M_4, leading to an offset in the L_r-C_p resonance [8], [9]. The measured overall input P1dB and IIP3 of the LNA+mixer are -24 dBm and -18 dBm, respectively. As specified in [2] and [5], the required gain, NF and IIP of the RX front-end are about 20 dB, 10 dB and -20 dBm, respectively. The proposed LNA+mixer's performances satisfy the Zigbee system requirements but dissipates significantly smaller current. Table I summarizes the performance of the proposed LNA+mixer in comparison with previous works. As can be seen in Table I, overall, (that is, considering operating frequency, conversion voltage gain, noise figure and dc power dissipation) the proposed LNA+ mixer shows the best performance as a low power solution.

TABLE I
Summary of the LNA+Mixer Performances in Comparison With Previous Works

RF front-end	[1]	[3]	[4]	This work
Operating Frequency [GHz]	2.44	0.9	0.9	2.4
Conversion Gain [dB]	21.4	15	10	21
Noise Figure [dB]	13.9	4	2.5	6
Power Consumption [mW]	6.4	4.32	3.6	1.62
Technology [μm]	CMOS 0.18	CMOS 0.18	CMOS 0.18	CMOS 0.18

IV. Conclusion

A current-reused ultra-low-power, low noise LNA+mixer architecture is proposed and the advantages and the design guidelines are discussed. The proposed LNA+mixer architecture is applied for 2.4 GHz Zigbee application based on 0.18 μm CMOS technology. Measurements show 21 dB of conversion gain, 6 dB of NF with approximately 300 KHz flicker noise corner frequency while consuming 1.6 mW.

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