Compact low-power high-slew-rate buffer for LCD driver applications

H.-B. Le, X.-D. Do and S.-G. Lee

A very compact, rail-to-rail, low-power, high-speed buffer amplifier for LCD driver applications is proposed. A slew-rate enhancement technique based on a dynamic current bias scheme is adopted, and a high slew-rate is obtained without increasing the quiescent current. The buffer amplifier uses a small number of transistors and enables very small active layout area. The proposed buffer amplifier is suitable for both low- and high-voltage LCD driver applications.

Introduction: As liquid-crystal displays (LCDs) approach high resolution, high quality, and physically large panel size, the design of output buffer amplifiers becomes more challenging. More specifically, the buffer amplifier needs to be faster in order to deal with larger load capacitance and resistance and thereby achieve smaller settling time. In addition, hundreds or thousands of output buffer amplifiers are integrated into one driver IC, and the buffer should occupy a small die area and consume small static power. It also should provide a rail-to-rail voltage driving capability so that higher grey levels can be accommodated.

To reduce settling time, the slew-rate of the buffer amplifier should be increased, because the slewing time normally dominates the settling time in LCD applications. Several techniques have thus far been used to increase slew-rate without additional static power. Lu [1, 2] used additional comparators to sense the rising/falling edges of the input and then turn on push/pull transistors in the output stage to charge/discharge the output load. Yu and Wu [3] proposed a class B buffer in which a comparator is used in the negative feedback path to eliminate the static current in the output stage. Kim and Cho [4] adopted positive feedback loops to speed up the slew-rate of the proposed buffer when there is a voltage difference in the differential input. Choi *et al.* [5] developed an adaptive dynamic current biasing scheme to increase slew-rate without increasing the quiescent current. In this Letter we propose a very compact low-power high-speed rail-to-rail buffer amplifier using a slew-rate enhancement technique (SRET) based on the adaptive current biasing scheme [5].

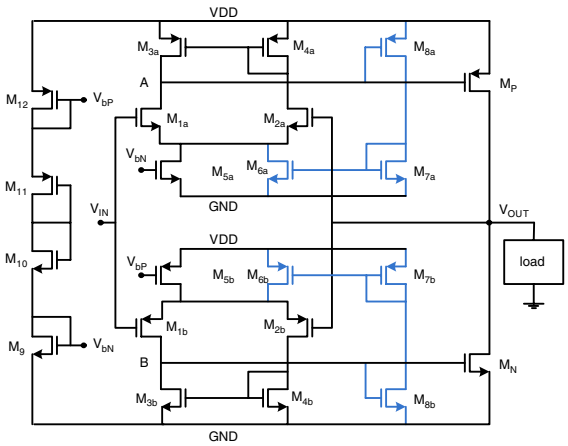

Fig. 1 *Proposed buffer amplifier*

Proposed buffer amplifier: Fig. 1 schematically illustrates the proposed buffer amplifier. To provide rail-to-rail driving capability, the buffer is composed of two complementary differential inputs with a common-source push-pull output stage, M_N/M_P. The upper part, M_{1a}-M_{5a}, with an NMOS input stage drives the output PMOS transistor, M_P, for sourcing current. The lower part, M_{1b}-M_{5b}, with an PMOS input stage drives the output NMOS transistor, M_N, for sinking current. Transistors $M_{6a/b}$-$M_{8a/b}$ form the slew-rate enhancement circuits. M_{6a}-M_{8a} in the upper part are responsible for rising slew enhancement while M_{6b}-M_{8b} in the lower part are responsible for falling slew enhancement. In the steady state, where the input and output voltage are the same, the slew enhancement circuits should consume very small static current in order to save power. Accordingly, $M_{8a/b}$ should be turned off during the steady state by biasing $M_{3a/b}$-$M_{4a/b}$ in the triode region so that the drain voltages of M_{3a}-M_{4a} are close to VDD and those of M_{3b}-M_{4b} are close to GND. The gate-source and drain-source voltages of these transistors should satisfy the following conditions:

$$|V_{GS\_8a}| = |V_{DS\_3a}| = |V_{DS\_4a}| = |V_{GS\_4a}| < |V_{thp}| \quad (1)$$

$$V_{GS\_8b} = V_{DS\_3b} = V_{DS\_4b} = V_{GS\_4b} < V_{thn} \quad (2)$$

In the slewing condition, when a large low-to-high step signal appears at the input, V_{IN}, all the tail current from M_{5a} flows through M_{3a}; accordingly, the drain voltage of M_{3a}, V_A, decreases. Subsequently, M_{8a} turns on and provides additional current to the upper part input pair through the current mirror circuit, M_{6a}-M_{7a}. Similarly, the falling slew detection circuit, M_{6b}-M_{8b}, operates when a large high-to-low step signal appears at the input, providing more current to the lower part input pair. In summary, whenever a large step signal is applied to the input (slewing condition), additional current will be supplied to the input pair, providing more dynamic current, which in turn helps to increase the slew-rate of the proposed buffer amplifier. Fig. 2 shows the simulated transient currents flowing through the lower and upper part, respectively, during slewing period. The maximum dynamic currents are more than 900 μA from the quiescent bias currents of less than 1 μA.

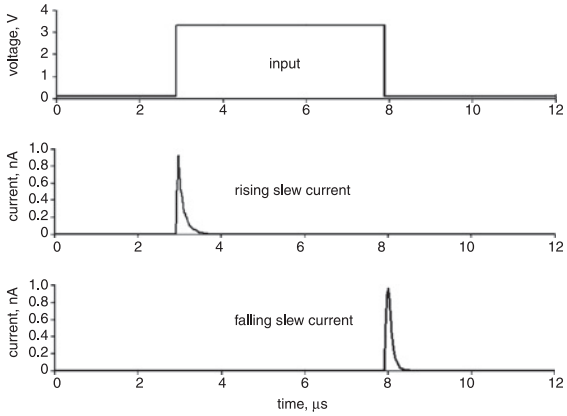

Fig. 2 *Simulated transient currents during slewing period*

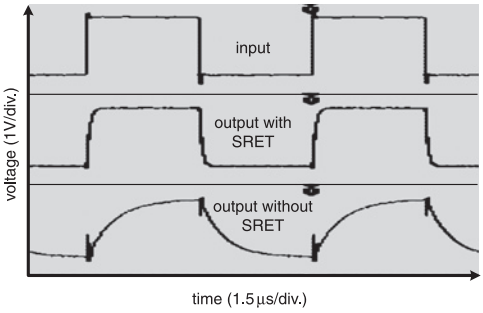

Fig. 3 *Measured step responses of version_01 chip with and without SRET*

Experimental results: To verify the proposed slew-rate enhancement technique, two versions of the proposed buffer were designed in different processes. Version_01 was designed and fabricated in a 0.18 μm CMOS process with a 3.3 V supply for low-voltage LCD driver applications, while version_02 was designed and simulated in a 0.35 μm CMOS process with a 12.0 V supply for high-voltage LCD driver applications. Fig. 3 shows the measured step responses of version_01 chip with and without the SRET for a step input of 0.1–3.2 V and 680 pF capacitive load. The SRET helps to increase the rising/falling slew-rates roughly seven-fold (from 2.6/2.5 to 18.0/18.5 V/μs). The rising/falling settling times within 0.2% of the final voltage are 0.45/0.40 μs when using the SRET and 2.40/2.70 μs without using the SRET. Fig. 4 shows the simulated transient responses of the version_02 chip with a step input of 0.1–11.9 V and 1.0 nF capacitive load. The rising/falling slew-rates are 25.0/23.0 and 4.1/4.0 V/μs for the proposed buffer with and without the SRET, respectively. The rising/falling settling times within 0.2% of the final voltage are 1.4/1.5 μs with the SRET and 4.5/5.0 μs without the SRET. The measured maximum offset voltage for the version_01 chip is 3.5 mV, and within 90% of the input range, 0.15–3.15 V, the offset voltage is less than

1.0 mV. Fig. 5 shows the layout of the version_01 chip. The chip occupies an active area of 30 × 60 μm. Table 1 presents a performance summary and comparisons with several published works. The proposed buffer shows the best performance.

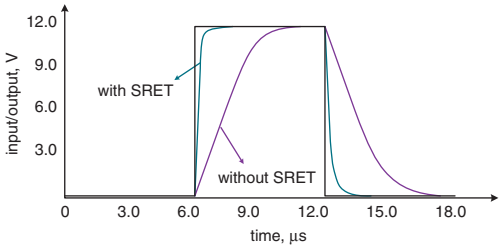

Fig. 4 *Simulated step responses of version_02 chip with and without SRET*

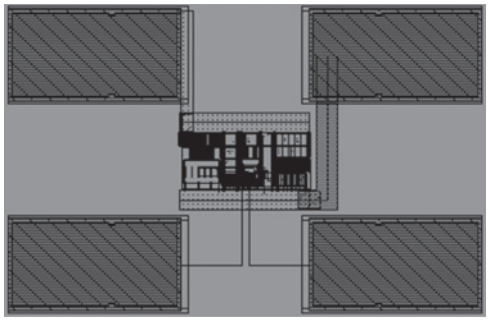

Fig. 5 *Version_01 chip layout*

Table 1: Performance summary and comparisons

Parameters	This work		[1]	[2]	[3]	[4]	[5]
	Version_01 (measured)	Version_02 (simulated)					
Process	0.18 μm	0.35 μm HV	0.60 μm	0.35 μm	0.80 μm	0.35 μm	0.35 μm
Supply voltage (V)	3.3	12	5	3.3	5	3.3	3.3
Load	680 pF	1.0 nF	680 pF	680 pF	600 pF	1.0 nF	20k/200 pF
Input/output range	0.1–3.2	0.1–11.9	0.15–4.0	0.14–3.09	1.0–5.0	NA	0–3.3
Slew-rate +/− (V/μs)	18.0/18.5	25.0/23.0	NA	NA	NA	>10	8
Max. offset (mV)	3.5	3.6	6	NA	7	10	NA
Settling time +/− (μs)	0.45/0.40	1.4/1.5	1.6/1.0	1.1/1.3	8.0/3.0	NA	7.2/6.4
Static current (μA)	0.3–1.3	1.0 – 4.0	30	4.5	24	1	5–6.5
Chip size (μm × μm)	30 × 60	NA	NA	NA	230 × 140	NA	NA

Settling time at 0.2% of final voltage; +/− : rising/falling edge; HV: high voltage

Conclusions: A very compact high-speed low-power buffer amplifier is presented. The proposed slew-rate enhancement technique helps to increase the speed of the buffer without additional static current. The number of transistors has been minimised thanks to the slew-rate enhancement technique, and the active area is very compact. The proposed buffer shows excellent performance in terms of speed, offset, power consumption, and chip size for both low and high voltage supplies, and thus has considerable potential for LCD drive applications.

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One or more of the Figures in this Letter are available in colour online.

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