An IF Bandpass Filter Based on a Low Distortion Transconductor

Ha Le-Thai, Huy-Hieu Nguyen, Hoai-Nam Nguyen, Hong-Soon Cho, Jeong-Seon Lee, and Sang-Gug Lee, *Member, IEEE*

***Abstract*—In this paper, a linearity improvement technique is proposed for a low-distortion G_m–C bandpass filter operating in high IF ranges. The proposed transconductor eliminates G_m'' value at the output by superposing the opposite non-linear behaviors of two differential structures in parallel. For the bandpass filter, instead of conventional biquad structure, a resonant-coupling structure is adopted for a flat frequency response which is insensitive to process and temperature variations. Fabricated in 65 nm CMOS process, the implemented 80 MHz bandpass filter shows a flat bandpass characteristic with 0.1 dB ripple, third-order harmonic rejection of 27 dB, IIP3 of −2 dBm, and NF of 21.5 dB, while consuming 11 mA from 1.2-V supply. The filter occupies the chip size of 0.5 × 0.5 mm^2.**

***Index Terms*—Low-distortion transconductor, linearization technique, Gm-C filter, flat band-pass.**

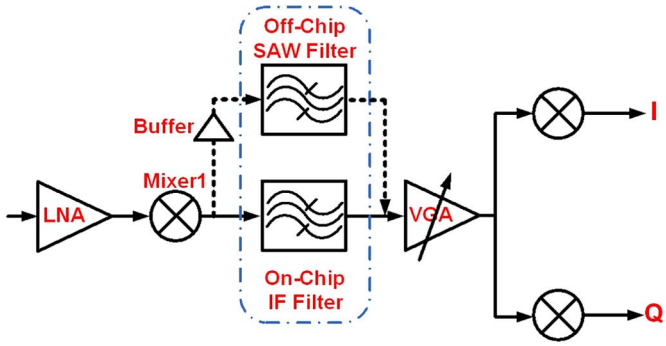

Fig. 1. Heterodyne receiver structure.

I. Introduction

In SOME wireless transceivers, especially heterodyne receivers shown in Fig. 1, the usages of off-chip SAW IF filters show disadvantages such as size and additional power consumption. In the heterodyne receiver structure shown in Fig. 1, the IF filter is placed after the first mixer stage in order to filter out unwanted IF signals. Because the input and output impedances of off-chip SAW filters are designed to be 50 Ohm, there must be a 50 Ohm buffer following the first mixer to drive the SAW filter. Thus, this structure with an off-chip SAW filter is likely to consume more power and chip area. Therefore, it would be nice to replace the off-chip SAW IF filter by an on-chip IF filter.

There are various filter types that are appropriate for the implementation of on-chip IF bandpass filters. Those are active-RC filters, switched-capacitor filters, and G_m–C filters. Though high linearity is an advantage of both active-RC and switched-capacitor filters, these filters have a disadvantage of operating at high frequency ranges due to the limitation of the unity bandwidth of the operational amplifier (OPAMP). Besides, it is not easy to implement tuning scheme for those two filter types. Meanwhile, G_m–C filters are popular for on-chip applications due to their advantages of high frequency performance and low power consumption, but have linearity problems. In order to overcome the disadvantage of linearity of G_m–C filters, many linearization techniques for transconductors have been reported. Fig. 2 shows some well-known linearization techniques. The resistive source degeneration technique shown in Fig. 2(a) may be the simplest and most well-known one, in which the linearization is achieved at the cost of power consumption. Fig. 2(b) shows the dynamic source degeneration technique [1], which is an improved version of the structure shown in Fig. 2(a). Though the range of input signal levels that the transconductor is linear is broadened, the ripple of the G_m response over the input amplitude is still high. The tunable feedback technique [2] shown in Fig. 2(c) and its combination with the dynamic source degeneration technique [3] shown in Fig. 2(d) are also reported to achieve high linearity at the cost of high power consumption due to the additional bias feedback part. Fig. 2(e) shows a transconductor with bias feedback technique [4], in which the four additional transistors M_3, M_4, M_5, and M_6 compose the adaptive biasing block besides the normal differential pair composed of two transistors M_1 and M_2. The additional block takes a role to keep the total current flowing through the main differential pair M_1 and M_2 balanced, increasing the linearity of the transconductor. Yet the obligated usage of a current tail in this bias feedback method limits its performance at low supply voltages. Besides, the technique is significantly affected by mismatching between the main differential pair and the adaptive biasing block.

In this paper, a linearization technique [5] is proposed to implement a low-distortion transcondutor by realizing a superposition method to diminish nonlinear components.

The next thing that needs to be considered here is the filter architecture for the high unwanted signal rejection ratio and flat

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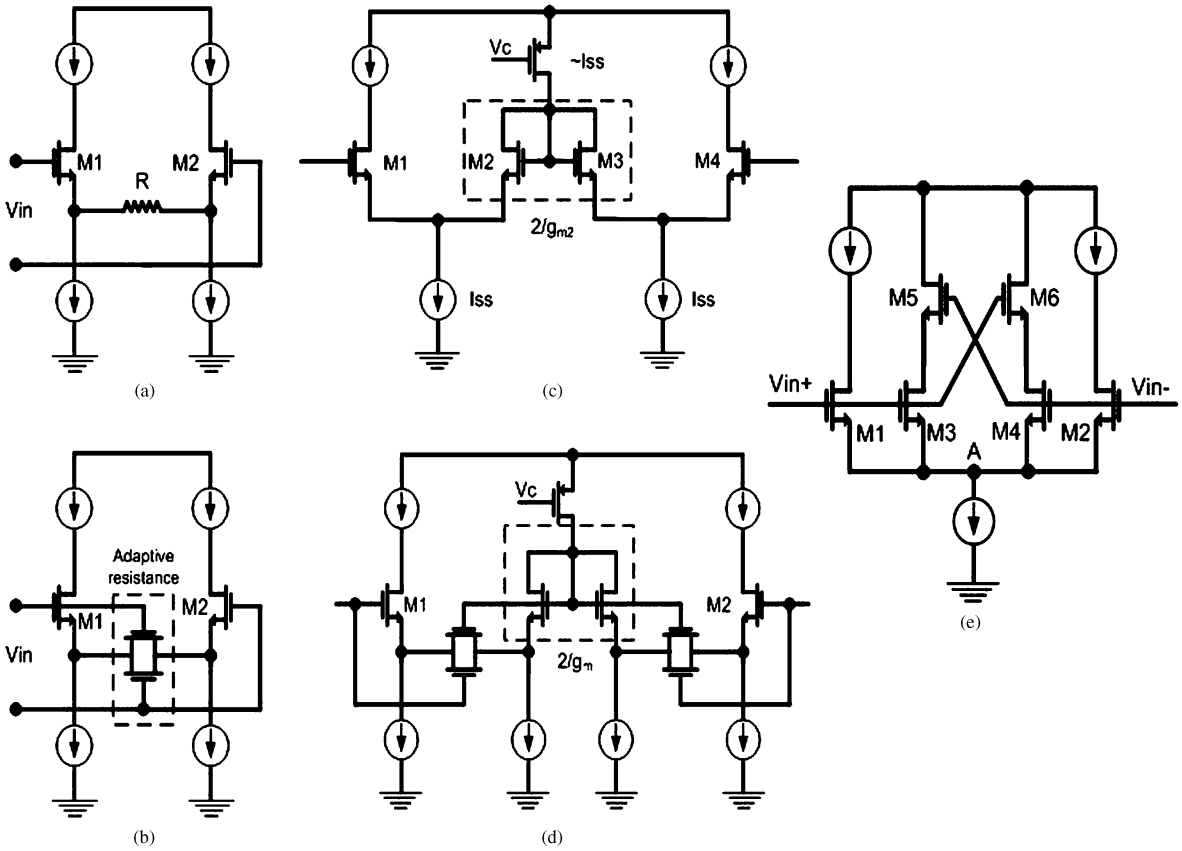

Fig. 2. Linearization techniques for Gm cells: (a) resistive source degeneration technique; (b) dynamic source degeneration technique; (c) tunable-feedback technique; (d) source-degeneration tunable-feedback combined technique; (e) bias feedback (or adaptive biasing) technique.

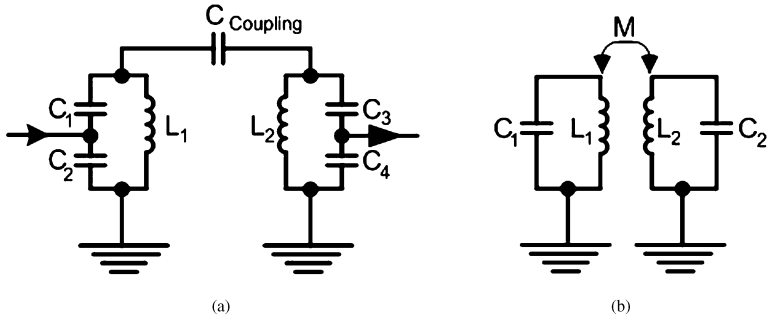

Fig. 3. Methods for making pass-band flat: (a) C-coupling method; (b) magnetic-coupling method.

pass-band characteristics. For high rejection ratio, negative resistance technique can be adopted as a simple method to increase the quality (Q) factor of the filter in this design.

Flat pass-band characteristic is another important issue of IF bandpass filter design because in-band signals after the filter are required to be equal in terms of strength. Fig. 3 shows C-coupling [6] and Magnetic-coupling [7] methods in order to achieve flat pass-band characteristics. However, each of them has its own disadvantages. Fig. 3(a) shows C-coupling technique, in which the two resonators are coupled together by a coupling capacitor C_{Coupling}. The value of the coupling capacitor is very important. Too high value of C_{Coupling} will lead to over-coupling problem which causes the bandwidth of the filter broadened too much. On the other hand, too small value of C_{Coupling}, though helps to narrow the bandwidth of the filter response, leads to a high insertion loss. It means that the high Q factor is achieved at the cost of higher loss. Besides, on-chip capacitor values usually show significant process variation, causing the bandwidth of the filter to vary. Fig. 3(b) shows another method to achieve flat bandpass filter called Magnetic-coupling, in which the two resonators are coupled together by the mutual inductance between the two inductors L_1 and L_2. There have been some reports [8], [9] trying to achieve equivalent active-circuit models for the Magnetic-coupling structure. In those papers, equivalent circuits based on voltage-controlled-voltage-source (VCVS) and current-controlled-current-source (CCCS) models have been adopted. Yet, the obligatory usage of inductors in this method limits the applications only for high frequency ranges. Thus, this technique is not proper for the IF frequency range.

In this paper, an on-chip IF bandpass filter working in 80 MHz band with low noise and high linearity as well as a flat bandpass characteristics has been introduced. The proposed linearization

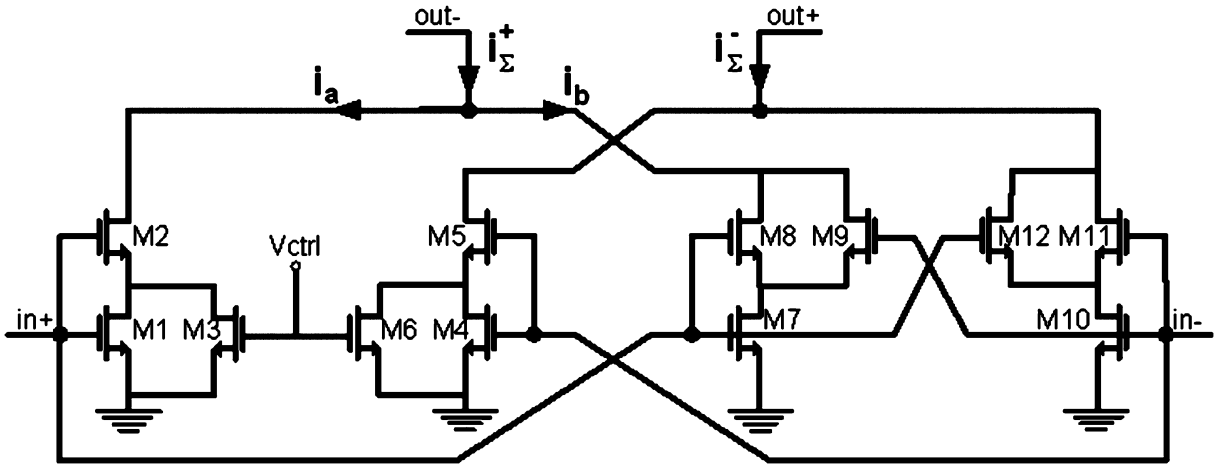

Fig. 4. The core structure of the proposed CMOS transconductor.

technique for the transconductors is described in Section II. Section III describes the filter architecture. The implementation result is given in Section IV. Section V concludes the paper.

II. Transconductor Description

A. The Proposed Highly Linear Transconductor

Fig. 4 shows the core structure schematic of a linearity improvement technique for the G_m-cell. In Fig. 4, there are 12 nMOS transistors M_1–M_{12}, of which two groups of 6 nMOS transistors are categorized for the two sides of the structure. The left wing of the structure is composed of nMOS transistors M_1–M_6 while the right wing is made of nMOS transistors M_7–M_{12}. In Fig. 4, both the right and the left wings are in differential structure. It means that there are pairs (M_1, M_4), (M_3, M_6), (M_2, M_5), (M_7, M_{10}), (M_8, M_{11}), and (M_9, M_{12}), in each of which, transistors are identical. From above descriptions, the proposed linearization method is analyzed based on the superposition of two paralleled differential structures with opposite behaviors of nonlinearity. These two opposite responses of the two parallel wings in Fig. 4 compensate one another to diminish non-linear elements. Therefore, the total distortion at the output of the G_m-cell can be reduced.

The structure of the two parallel sides, which are explained above is pseudo differential which is more suitable for low voltage design.

Fig. 5(a) and (b) show the halves of circuits in the left and the right wings described in Fig. 4, respectively. The both half circuits shown in Fig. 5(a) and (b) share the same self-cascode structure part, which is composed of transistors M_1 and M_2 in Fig. 5(a), and transistors M_7 and M_8 in Fig. 5(b). Based on the characteristics of self-cascode circuit, it can be realized that M_1 and M_7 operate in triode region while M_2 and M_8 are in saturation region. From Fig. 5(a)

$$i_2 = k_2(V_{\rm CM} + v - V_X - Vt)^2 \tag{1}$$

$$i_1 + i_3 = k_1\left[2(V_{\rm CM} + v - Vt)V_X - V_X^2\right] + k_3\left[2(V_C - Vt)V_X - V_X^2\right] \tag{2}$$

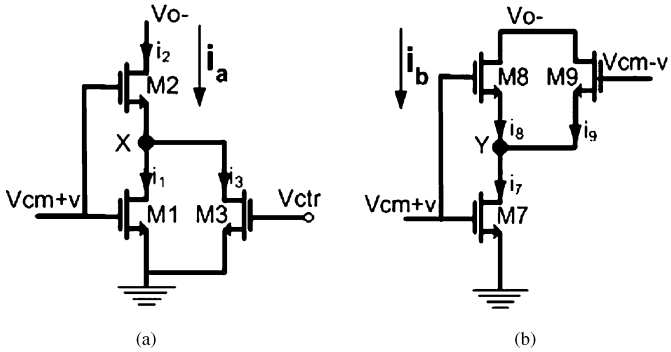

Fig. 5. The two half circuits of the two wings of Fig. 4, (a) the half of the left wing in Fig. 4, (b) the half of the right wing in Fig. 4.

where i_1, i_2, and i_3 are the drain currents of transistors M_1, M_2, and M_3, respectively, $V_{\rm CM}$ and $\pm v$ are the common mode and small AC voltages of the input node, respectively, Vt is the threshold voltage of nMOS transistors, V_X is the voltage value at node X of Fig. 5(a), $k_i = (1/2)(W/L)_i C_{\rm OX} (i = 1, 2, 3, 4, \ldots, 12)$, $k_{ij} = k_i + k_j (i \neq j)$, and $k_{ijl} = k_i + k_j + k_l (i \neq j \neq l)$. In Fig. 5, $V_{\rm CM} + v$ is applied at the inputs of transistors M_1, M_2, M_7, and M_8, while $V_{\rm CM} - v$ is at the input of M_9 in Fig. 5(b).

Since $i_2 = i_1 + i_3$, from (1) and (2), the voltage of node X can be expressed as

$$V_X = V_{\rm CM} - Vt + \frac{k_{12}v - \sqrt{\Delta'_X}}{k_{123}} \tag{3}$$

where

$$\Delta'_X = \left(k_{12}^2 - k_{123}k_2\right)v^2 + 2k_{123}k_1(V_{\rm CM} - Vt)v + k_{123}k_{13}(V_{\rm CM} - Vt)^2. \tag{4}$$

Therefore, from (1), and (3), the drain current i_a shown in Fig. 5(a) can be given by

$$i_a = i_2 = k_2\left(\frac{k_3 v + \sqrt{\Delta'_X}}{k_{123}}\right)^2. \tag{5}$$

Similarly, the drain current i_b shown in Fig. 5(b) can be given by

$$i_b = i_7 = k_8\left(\frac{2k_9 v + \sqrt{\Delta'_Y}}{k_{789}}\right)^2 + k_9\left(\frac{-2k_{78}v + \sqrt{\Delta'_Y}}{k_{789}}\right)^2 \tag{6}$$

where i_7, i_8, and i_9 are the drain currents of transistors M_7, M_8, and M_9, respectively; and

$$\Delta'_Y = [(k_{78}-k_9)^2 - k_{789}k_{89}]v^2 + 2k_{789}k_7(V_{\rm CM}-Vt)v + k_{789}k_7(V_{\rm CM}-Vt)^2. \tag{7}$$

Thus, from (5) and (6), the total drain current i_Σ in Fig. 4 can be given as

$$\begin{aligned} i_\Sigma &= i_a + i_b \\ &= k_2\left(\frac{k_3 v + \sqrt{\Delta'_X}}{k_{123}}\right)^2 + k_8\left(\frac{2k_9 v + \sqrt{\Delta'_Y}}{k_{789}}\right)^2 \\ &\quad + k_9\left(\frac{-2k_{78}v + \sqrt{\Delta'_Y}}{k_{789}}\right)^2 \\ &= \frac{k_2}{k_{123}^2}\Delta'_X + \frac{k_{89}}{k_{789}^2}\Delta'_Y \\ &\quad + \left[\frac{k_2 k_3^2}{k_{123}^2} + 4\frac{(k_8 k_9^2 + k_9 k_{78}^2)}{k_{789}^2}\right]v^2 \\ &\quad + \left[\frac{2k_2k_3}{k_{123}^2}\sqrt{\Delta'_X} - \frac{4k_{78}k_9}{k_{789}^2}\sqrt{\Delta'_Y}\right]v. \end{aligned} \tag{8}$$

Since the proposed transconductor is as differential structure as shown in Fig. 4, from (8), the differential output current $i_{\rm out}$ of the transconductor is

$$\begin{aligned} i_{\rm out} = i_\Sigma^+ - i_\Sigma^- &= \frac{k_2}{k_{123}^2}[\Delta'_X(v) - \Delta'_X(-v)] \\ &\quad + \frac{k_{89}}{k_{789}^2}[\Delta'_Y(v) - \Delta'_Y(-v)] \\ &\quad + \left[\frac{2k_2k_3}{k_{123}^2}\left(\sqrt{\Delta'_X(v)} + \sqrt{\Delta'_X(-v)}\right)\right. \\ &\quad \left. - \frac{4k_9k_{78}}{k_{789}^2}\left(\sqrt{\Delta'_Y(v)} + \sqrt{\Delta'_Y(-v)}\right)\right]v \end{aligned} \tag{9}$$

where, from (4) and (7),

$$\Delta'_X(v) - \Delta'_X(-v) = 4k_{123}k_1(V_{\rm CM}-Vt)v \tag{10}$$

$$\Delta'_Y(v) - \Delta'_Y(-v) = 4k_{789}k_7(V_{\rm CM}-Vt)v. \tag{11}$$

Equations (10) and (11) show that $[\Delta'_X(v) - \Delta'_X(-v)]$ and $[\Delta'_Y(v) - \Delta'_Y(-v)]$ are linear components. Thus, in (9),

$$\left[\frac{2k_2k_3}{k_{123}^2}\left(\sqrt{\Delta'_X(v)} + \sqrt{\Delta'_X(-v)}\right) - \frac{4k_9k_{78}}{k_{789}^2}\left(\sqrt{\Delta'_Y(v)} + \sqrt{\Delta'_Y(-v)}\right)\right]v$$

is the distortion source of the differential output current $i_{\rm out}$. Because of the fact that (9) is the differential expression of (8), it is easy to recognize $[(2k_2k_3)/(k_{123}^2)\sqrt{\Delta'_X} - (4k_9k_{78})/(k_{789}^2)\sqrt{\Delta'_Y}]$ as the nonlinear part of the output current i_Σ in (8).

Since $[(2k_2k_3)/(k_{123}^2)\sqrt{\Delta'_X} - (4k_9k_{78})/(k_{789}^2)\sqrt{\Delta'_Y}]$ in (8) is the source of distortion of the proposed transconductor, the component $(2k_2k_3)/(k_{123}^2)\sqrt{\Delta'_X}$ is the nonlinear contributor of the left wing shown in Fig. 5(a), while $-(4k_9k_{78})/(k_{789}^2)\sqrt{\Delta'_Y}$ is the nonlinear contributor of the right wing shown in Fig. 5(b). These two nonlinear components are opposite in sign and tend to cancel each other. And the highest linearity of the transconductor is achieved as these two distortion components of the left and the right wings cancel completely one another. Because of the fact that tuning the values of $(2k_2k_3)/(k_{123}^2)\sqrt{\Delta'_X}$ and $-(4k_9k_{78})/(k_{789}^2)\sqrt{\Delta'_Y}$ is implemented by controlling the sizes of transistors, the optimum condition for linearity can be achieved by changing the size of transistors in the G_m-cell. As a result, the 2nd derivative value (G''_m) of the overall transconductance value (G_m) can be kept nearly zero over a large range of input signal amplitude.

Fig. 6 shows the simulation results of transconductance values (G_m) and their second derivatives (G''_m). Fig. 6(a) shows the simulated transconductance values (g_m) of the left and the right wings as well as the overall transconductor shown in Fig. 4. Fig. 6(b) shows the simulation results of the second derivative values (g''_m) of the left wing, the right wing and the proposed transconductor. G''_m value of the overall transconductor is the combination of g''_m values of the left and the right wings. In Fig. 6(b), it can be seen that the g''_m values of the left and the right wings are in opposite signs. The total G''_m value of the transconductor is kept nearly zero over a large range of input signal.

In order to compare the proposed transconductor with some other famous types, Fig. 7 shows the simulated total harmonic distortion (THD) characteristics of four different types of transconductors: the conventional differential pair (CDP), the dynamic source degeneration pair (DSD) shown in Fig. 2(b), the bias feedback pair (BFB) shown in Fig. 2(e), and the proposed one (PPT). In the simulations, the same conditions of voltage supply, current consumption, and channel lengths of the transistors are applied for all the four methods. Fig. 7 shows that the linearity of BFB is higher than that of DSD, and DSD method is more linear than CDP. Among these four techniques, PPT method shows the lowest total harmonic distortion values over the others. Besides a better linearity achieved, the PPT technique also provides a low THD characteristic in a larger range of input level compared to the others.

Fig. 8 shows the simulation results of the G_m and G''_m values of the proposed transconductor while G_m values are tuned by changing the control voltage (Vctr) shown in Fig. 4. Fig. 8(a) shows G_m values according to each of Vctr values applied. In Fig. 8(b), it can be seen that the second derivative value G''_m changes little over the G_m tuning range. The reason for the insensitivity to the control voltage (Vctr) in Fig. 4 is caused by the triode region operation of the two identical transistors M_3 and M_6. Therefore, the linear amount of current contributed by those transistors does not have much effect on the linearity of

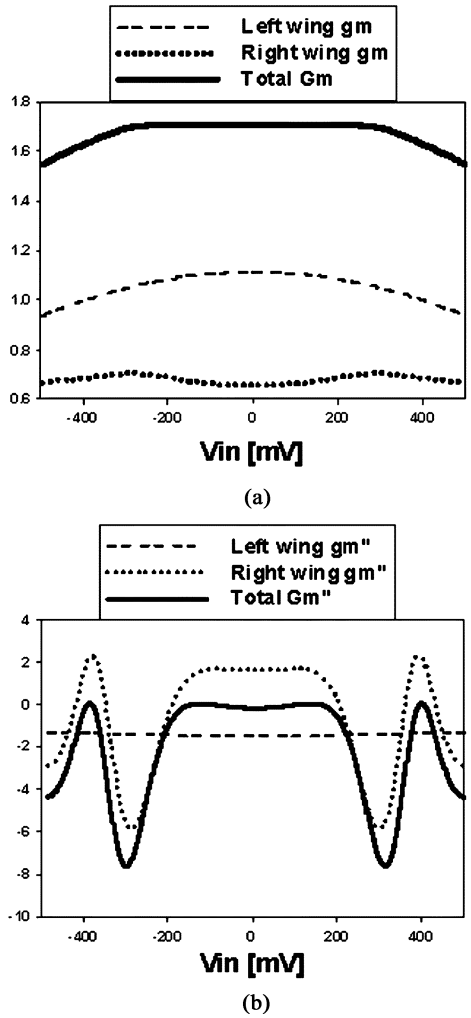

Fig. 6. Simulated characteristics of transconductances (g_m) and their derivatives (g''_m): (a) g_m value of the left and the right wings, and the combined total G_m value; (b) g''_m value of the left and the right wings, and the combined total G''_m value.

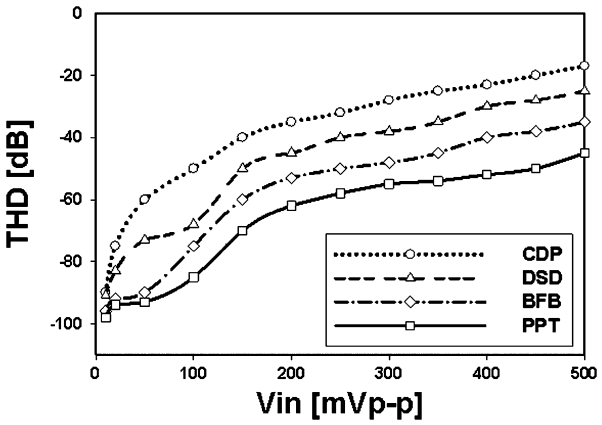

Fig. 7. Simulated total harmonic distortion (THD) versus the input voltage amplitudes for four cases of CDP, DSD, BFB, and PPT in the same voltage, current supplies and transistor channel length conditions.

the transconductor. As the result, the continuous-time tuning of the center frequency does not degrade the linearity of the filter.

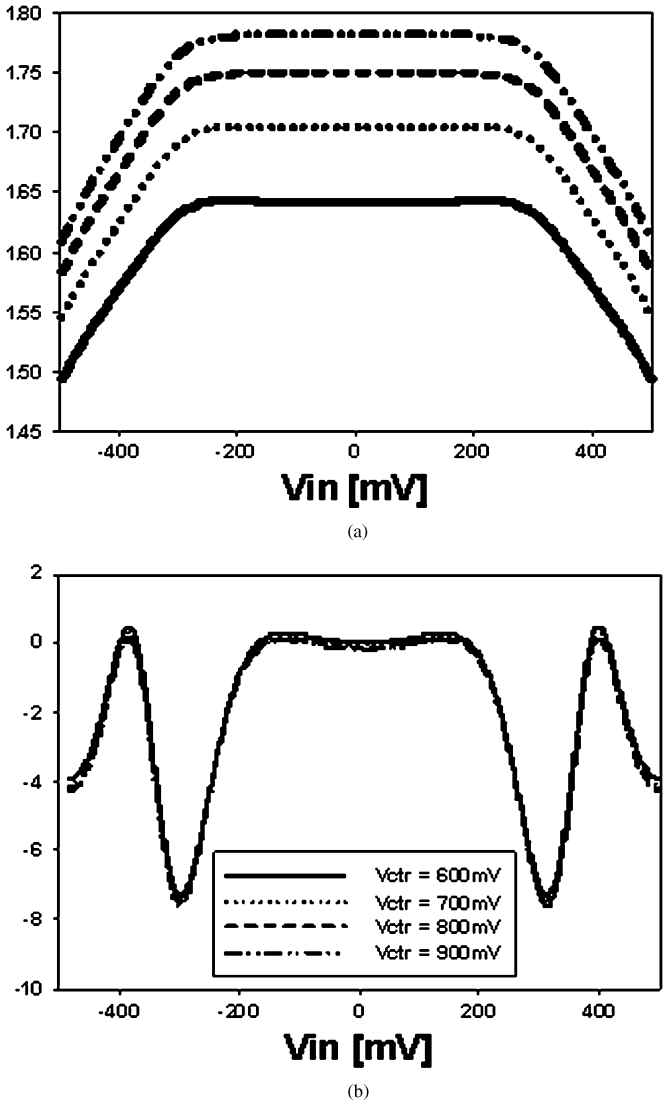

Fig. 8. The simulated variation of G''_m value versus G_m tuning: (a) G_m tuning with control voltage from 600 mV to 900 mV; (b) the change of G''_m versus G_m tuning.

Fig. 9 shows the simulations of the G_m and G''_m values of the proposed G_m-cell at different temperatures. In Fig. 9(a), though G_m varies, the flatness of the G_m behaviors over the input signal range stays the same. In Fig. 9(b), there is no significant change in G''_m values over the temperature variation. Thus, the linearity of the proposed transconductor is not significantly dependent on temperature variations. Besides, the variation of G_m values versus temperatures in Fig. 9(a) is due to the change in the threshold voltages of transistors, so causing the change of the bias current. Therefore, it can be explained that the variation of the width of the G''_m curves in Fig. 9(b) is because of the change in bias current of the G_m-cell.

B. The Complete Design of the Proposed Transconductor

Fig. 10 shows the overall design of the proposed transconductor which consists of the transconductance stage, the negative resistance circuits, and the common-mode feedback (CMFB) as well as common-mode feedforward (CMFF) circuits. In Fig. 10, all transistors of the same size are labeled with

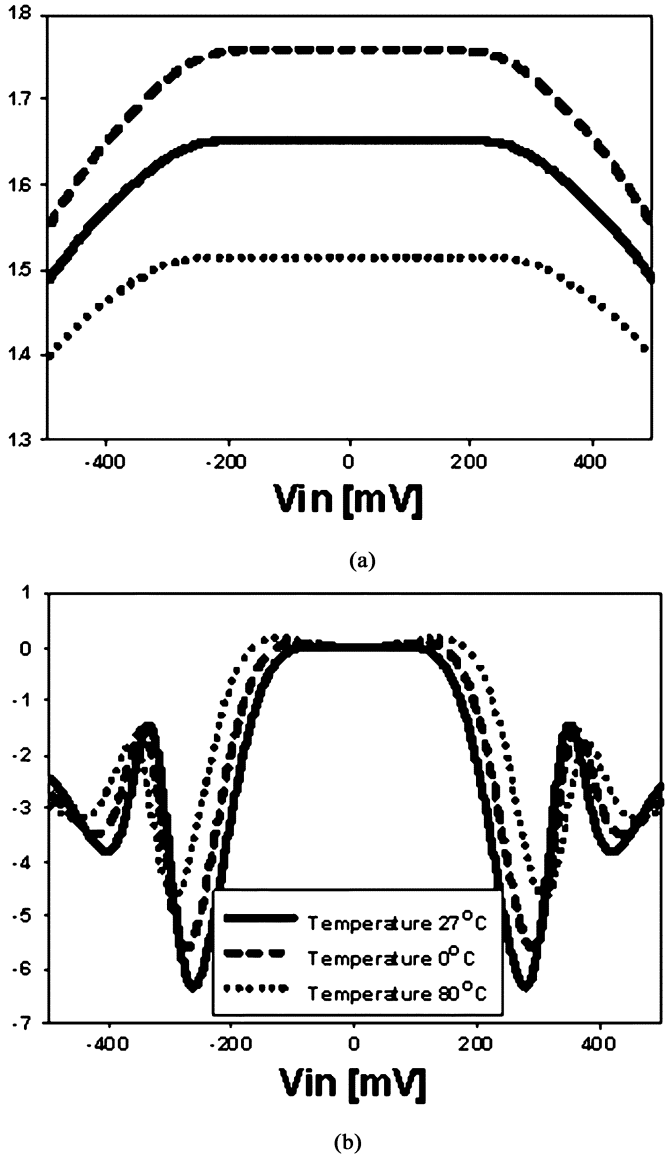

Fig. 9. The simulated variations of G_m and G''_m versus temperature conditions: (a) G_m variation; (b) G''_m variation.

same symbol. Fig. 10(a) shows the transconductance stage, in which identical pMOS transistors M_5–M_6 are adopted as active current sources of the transconductor. Fig. 10(b) shows the CMFB circuit which is composed of transistors M_7–M_{10}. The resistive common-mode detector is adopted for high linearity. The value of resistor Ro is around 100 kΩ. Additional small capacitors Co (20 fF) are adopted to prevent the phase margin degradation caused by the distributed capacitances of the common-mode resistors Ro [10]. In Fig. 10(b), in order to make sure that the phase margin of the CMFB loop is larger than 60°, one of the two pMOS active current sources of M_7 nMOS transistors is separated into two pMOS transistors M_9 and M_{10} [11]. And the transistor M_{10} is configured in diode structure to decrease the gain of the CMFB loop, by which the phase margin of the loop is increased. And the condition that $(W/L)_8 = (W/L)_9 + (W/L)_{10}$ is satisfied in order to keep the current flowing through the two transistors M_7 of the amplifier balanced.

Because the architecture adopted for the proposed transconductor is pseudo differential which is inherently sensitive to common-mode variations, there comes a need for a CMFF circuit [12]. Thus, transistors M_{11}–M_{13} in Fig. 10(b) are designed as the CMFF circuit to increase the common-mode rejection ratio (CMRR). The common-mode gain of the transconductor shown in Fig. 10(a) is $-G_m R_{\text{out}}$, in which G_m and R_{out} represents the transconductance and the output impedance of the transconductance stage shown in Fig. 10(a), respectively. The common-mode gain resulting from the CMFF circuit (M_{11}–M_{13}) shown in Fig. 10(b) and M_6 in Fig. 10(a) is $(2g_{m11})/(g_{m13})g_{m6}R_{\text{out}}$. Therefore, the overall common-mode gain of the transconductor shown in Fig. 10 is $-(G_m - (2g_{m11})/(g_{m13})g_{m6})R_{\text{out}}$. Thus, the common-mode gain can become zero by keeping $G_m = (2g_{m11})/(g_{m13})g_{m6}$, which can be satisfied by controlling the sizes of transistors.

Fig. 10(c) shows the complementary negative resistance circuit based on the positive feedback crossing structure [13], which is used to increase the output impedance of the transconductors in order to achieve higher Q factor for the filter. The transistor sizes of the negative resistance circuit are tuned to ensure that the DC operation point of the output is the same to the desired common-mode output level.

III. Filter Architechture

In order to achieve a flat pass-band characteristic, a resonant-coupling filter is employed by adopting the proposed linear transconductor. Fig. 11 shows the principle to achieve the flat pass-band characteristic that two poles at two different frequencies are created [14]. In conventional flat bandpass filter design, two poles are independently generated by the two resonators operating at two different frequencies. This approach has a disadvantage that the two generated poles are created by two independent resonators which is sensitive to process and temperature variations. In this paper, these two resonators are designed to operate at the same frequency. And an additional negative transconductance feedback coupling between the two resonators generates two poles at two different frequencies. Two frequencies of the two poles are correlated with each other and with the resonant frequency of the resonators. Therefore, the frequency response becomes less dependent on process and temperature variations.

Fig. 12 shows two equivalent filter structures for the two approaches to make the bandpass flat. Fig. 12(a) describes a filter composed of two cascaded resonators which operate at two different frequencies, which can be realized as the biquad structure.

For simpler calculation, the resonator is represented in an $L-C$ form whose impedance is expressed as

$$Z_{LC} = \frac{sL}{1 + s^2 LC}. \tag{12}$$

Thus, the voltages at node X and the output in Fig. 12(a) can be derived as

$$V_X = gm_1 \frac{sL_1}{1 + s^2 L_1 C_1} V_{\text{in}} \tag{13}$$

$$V_{\text{out}} = gm_2 \frac{sL_2}{1 + s^2 L_2 C_2} V_X \tag{14}$$

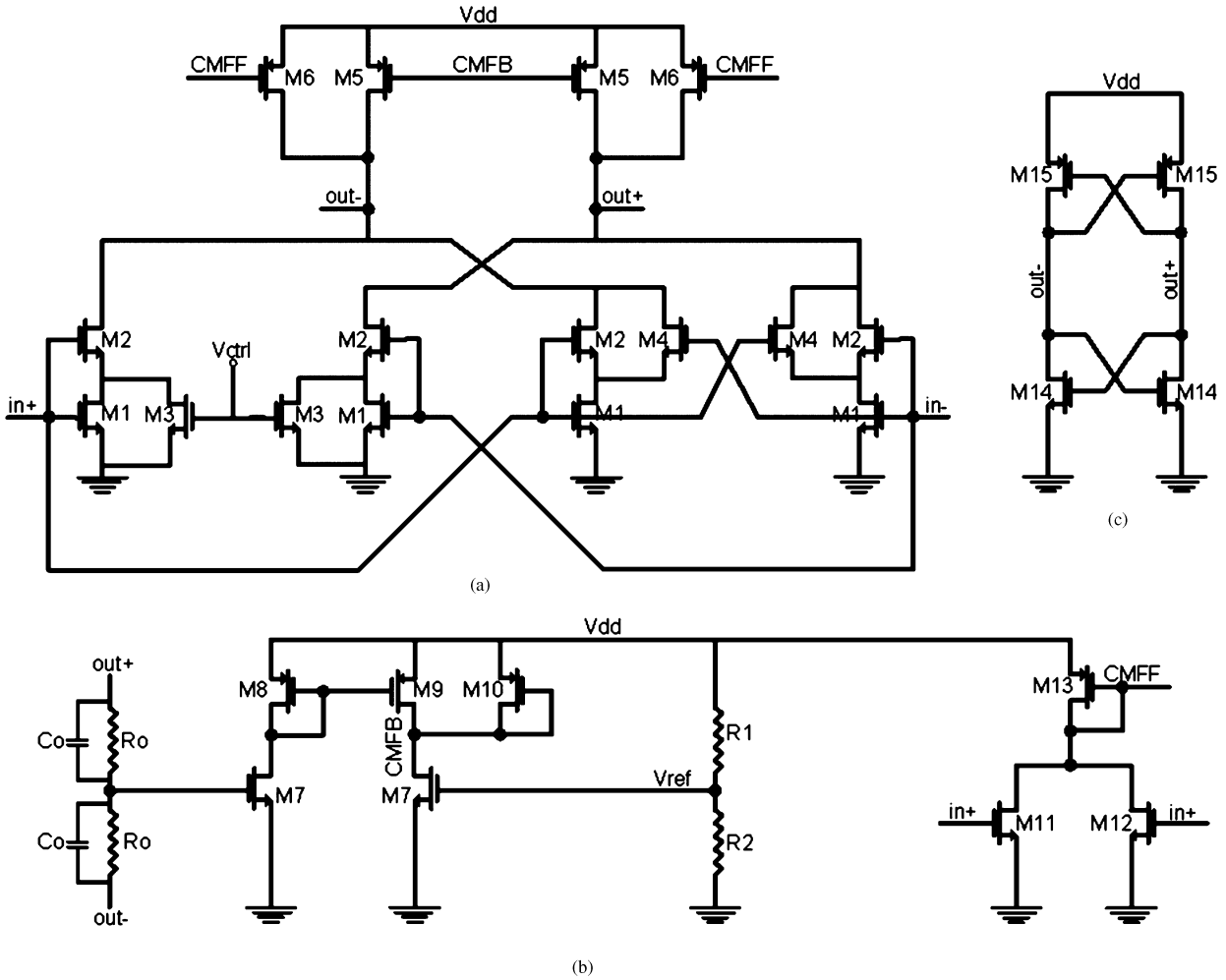

Fig. 10. The overall design of the proposed transconductor. (a) The proposed transconductor including pMOS dynamic-current-source transistors. (b) The CMFB and CMFF circuits. (c) The negative resistance.

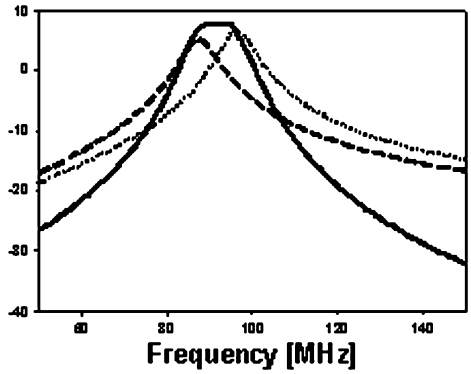

Fig. 11. Making the pass-band flat principle by combining two resonant frequencies.

where g_{m1} and g_{m2} are the transconductance values shown in Fig. 12(a).

From (13) and (14), the ac response of the filter structure in Fig. 12(a) can be expressed as

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}s^2}{(s^2+\omega_1^2)(s^2+\omega_2^2)} \tag{15}$$

where

$$\omega_1^2 = \frac{1}{L_1C_1} \quad \text{and} \quad \omega_2^2 = \frac{1}{L_2C_2}.$$

Since the two center frequencies in (15) are determined by the two separate *LC* resonators, the bandwidth and the pass-band flatness are sensitive to process and temperature variations. Fig. 12(b) shows the filter structure in which two identical resonators are coupled by a negative feedback path $(-g_{m3})$.

Similarly, $V_{\text{out}}/V_{\text{in}}$ can be derived as

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{\frac{g_{m1}g_{m2}}{C^2}s^2}{s^4 + 2s^2\left(\frac{1}{LC} + \frac{g_{m2}g_{m3}}{2C^2}\right) + \left(\frac{1}{LC}\right)^2} \tag{16}$$

where g_{m1}, g_{m2}, g_{m3} are the transconductance values shown in Fig. 12(b).

Equation (16) can be expressed as

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{\frac{g_{m1}g_{m2}}{C^2}s^2}{s^4 + 2s^2(\omega_0^2+\omega_\Delta^2) + \omega_0^4} = \frac{\frac{g_{m1}g_{m2}}{C^2}s^2}{(s^2+\omega_1^2)(s^2+\omega_2^2)} \tag{17}$$

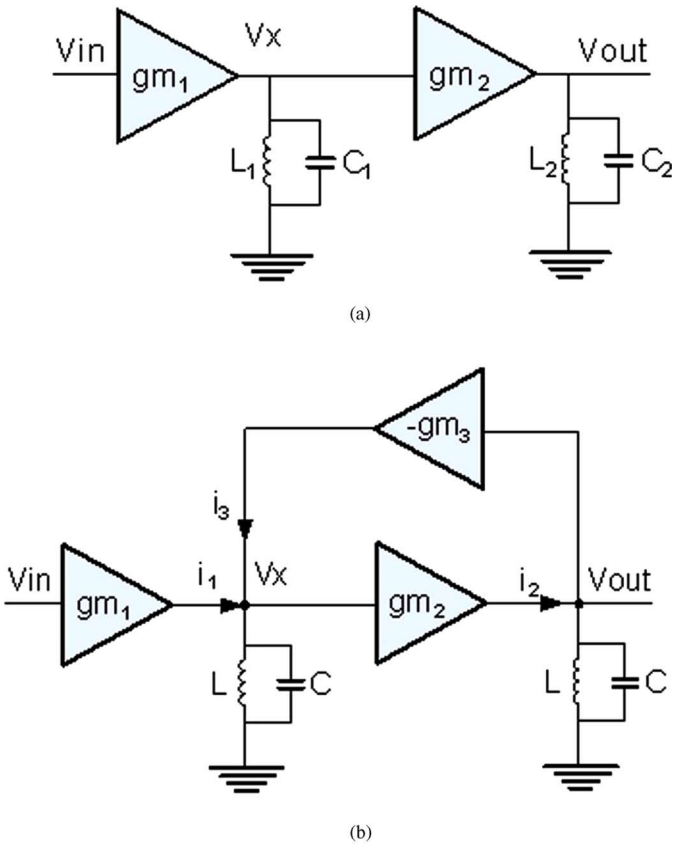

Fig. 12. Two investigated structures. (a) Cascaded resonators. (b) Resonant coupling.

where

$$\omega_0^2 = \frac{1}{LC}, \quad \omega_\Delta^2 = \frac{g_{m2}g_{m3}}{2C^2} \quad \text{and} \quad \begin{cases} \omega_1^2\omega_2^2 = \omega_0^4 \\ \omega_1^2 + \omega_2^2 = 2\left(\omega_0^2 + \omega_\Delta^2\right). \end{cases} \tag{18}$$

From (18), the defined bandwidth of the filter is given by

$$BW = \omega_2 - \omega_1 = \sqrt{2}\omega_\Delta = \sqrt{\frac{g_{m2}g_{m3}}{C^2}}. \tag{19}$$

Equation (17) says that the center frequency is $\omega_0 = (1/\sqrt{LC})$, and the two generated poles are ω_1 and ω_2. Equation (19) says that the bandwidth of the filter depends on the feedback G_m -cell - g_{m3}.

In (18), there is a correlation between the two poles ω_1 and ω_2. In other words, the shape of the ac response of the filter can become insensitive to process and temperature variations.

For more details on the insensitivity of the resonant-coupling structure mentioned above, the ratio $1/Q = BW/\omega_0$ of the filter in Fig. 12(b) has been investigated. When BW/ω_0 is less dependent on process and temperature variations, the shape of frequency response of the filter is more stable.

For the filter structure shown in Fig. 12(b),

$$\frac{BW}{\omega_0} = \frac{\sqrt{\frac{g_{m2}g_{m3}}{C^2}}}{\frac{g_m}{C}} = \sqrt{\frac{g_{m2}g_{m3}}{g_m^2}} \tag{20}$$

where ω_0 is replaced by g_m/C.

Both of the ratios g_{m2}/g_m and g_{m3}/g_m in (20) are insensitive to process and temperature variations. Thus, the resonant-coupling structure in Fig. 12(b) is insensitive to process and temperature variations.

The *LC* resonators are designed as a G_m–C integrator [15], which is a well-known technique. Fig. 13 shows the complete filter schematic derived from the resonant-coupling structure shown in Fig. 12(b). In Fig. 13, the *LC* resonators in Fig. 12(b) are implemented with G_m–C integrators which composed of transconductors g_m and capacitors C, of which the ratio g_m/C determines the center frequency of the filter. Transconductors g_{m1}, g_{m2} and g_{m3} operate for the same roles to those designed in the structure shown in Fig. 12(b).

Fig. 14 shows bandwidth tuning by controlling g_{m3} value. G_{m3} value is tuned by varying the control voltage (V_{gm3}) applied to the transistors M_3 and M_6 of that G_m-cell as shown in Fig. 4. The flatness of the pass-band is kept small over the tuning. The bandwidth of the filter increases when the g_{m3} value increases and vice versa.

A similar technique [16] was adopted by transforming a *LC* ladder filter into a coupled resonators structure by a well-known equation that $s^2 = (s^2 + \varpi_0^2)/(s\varpi_C)$, in which ϖ_0 and ϖ_C are center frequency and bandwidth.

IV. Experimental Results

The fourth-order G_m–C filter shown in Fig. 13 is designed in a 65 nm CMOS process. Fig. 15 shows the physical layout and the printed circuit board of the implemented filter occupying an area of 0.5×0.5 mm^2. The designed filter excluding the output buffer draws 11 mA from 1.2-V supply. The buffer at the output is included for matching with the 50 Ohm measurement equipment. Fig. 16 shows the measured frequency responses of the implemented filter. Fig. 16(a) shows the frequency response of the filter with 80 MHz center frequency. The 2 dB in-band gain of the filter in Fig. 16(a) is 5 dB lower than the simulation result, which is because of the output buffer of the chip. The filter attenuates the signals at the frequencies of $0.5f_0$ and $3f_0$ of the center frequency f_0 by 17 dB and 27 dB, respectively. Fig. 16(b) shows the zoom-in of the frequency response. Because of the Resonant-coupling structure, the achieved bandpass ripple in Fig. 16(b) is smaller than 0.1 dB in whole bandwidth of 10 MHz at 80 MHz center frequency. Fig. 16(c) describes frequency responses over continuous-frequency tuning. Compared to the cascade method shown in Fig. 12(a) in which the two resonators are totally independent on each other, the implemented structure has the advantage of stable frequency response as analyzed above. However, the stability over process and temperature variations is based on the matching of the two identical resonators shown in Fig. 12(b). Thus, in this design, the gain variation over frequency tuning shown in Fig. 16(c) is due to the asymmetrical layout causing variations on bias conditions. Besides, in Fig. 10(c), the negative resistance composed of transistors M_{15} and M_{14} is in pseudo structure. In order to match with the output of the transconductor, the DC level of the negative resistance is designed to be the same to that of the output of the transconductor. On the other hand, the value of the negative resistance is strongly dependent on the bias current flowing

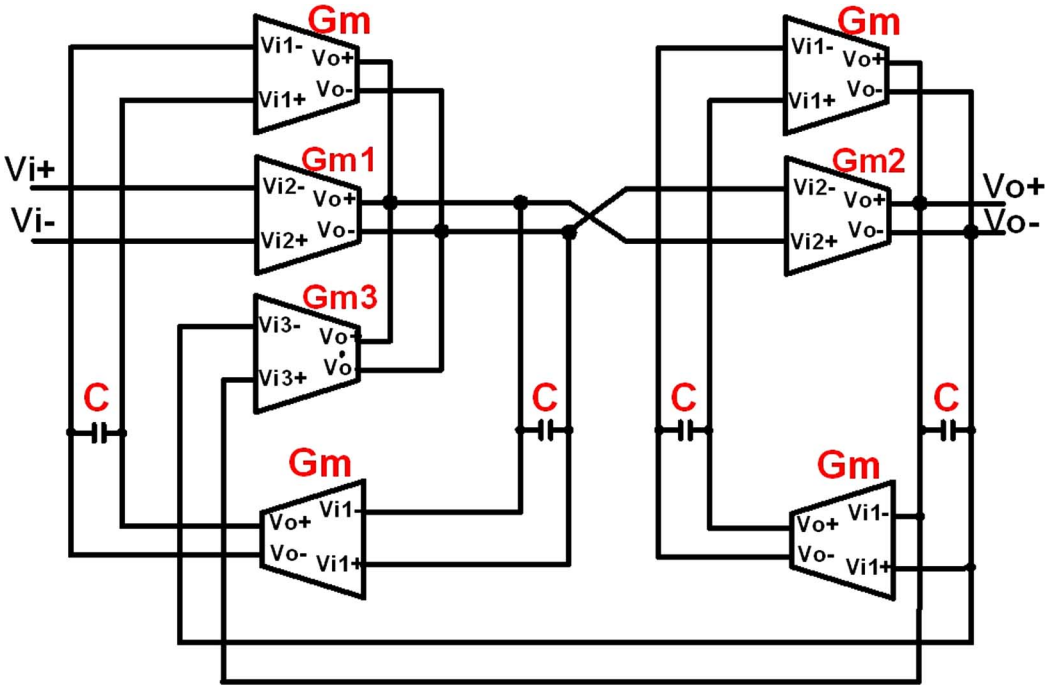

Fig. 13. The complete structure of the filter.

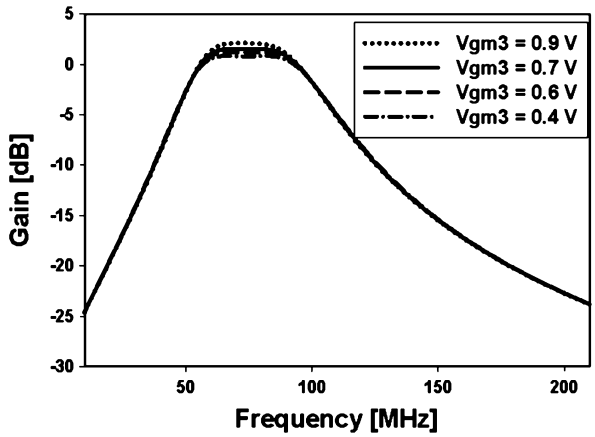

Fig. 14. Simulated Q-factor of the filter over g_{m3} tuning.

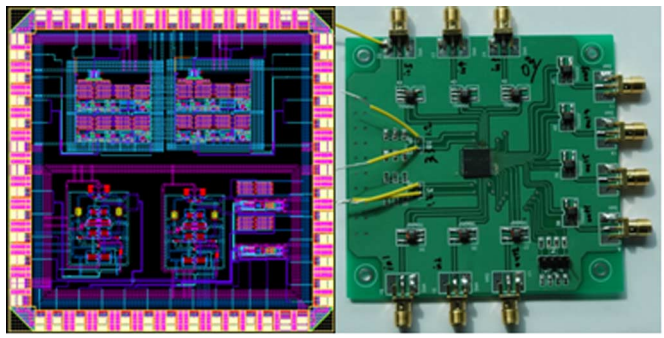

Fig. 15. Physical layout and printed circuit board of the implemented filter.

through it. Meanwhile, when the value of the voltage Vctr applied to transistors M_3 and M_6 is changed to tune the center frequency of the filter, the current flowing through transistors M_3 and M_6 varies causing the DC current flowing through pMOS and nMOS transistors of the negative resistance to be unbalanced. Thus, the value of the output DC level has been changed bringing out the value of the negative resistance to alter. Thus, the amplitude of the AC response of the filter varies in a range from 2 dB to 4 dB as the center frequency is tuned in a range from 60 MHz to 85 MHz.

Fig. 17 shows the measured frequency response versus the simulation results and the measured filter response variation over temperature range from 0 °C to 80 °C. In Fig. 17(a), the measured frequency response of the filter is compared with the two cases of simulation results, the case including and the case excluding the output buffer. There is a 5 dB difference in gain of these two cases of simulation causing by the output buffer. The measured result shows the gain almost the same to the simulated one, though there is about 6% variation in center frequency, which can be compensated by frequency tuning scheme. In Fig. 17 (b), frequency responses over temperature range from 0 °C to 80 °C with samples at 0 °C, 25 °C, and 80 °C have been shown. The shape of the filter varies little from 0 °C to 80 °C, which agrees with the calculation in (20).

Fig. 18 shows the measured noise figure (NF) of the whole filter including the output buffer, where the NF is 21.5 dB at center frequency of 80 MHz. The IIP3 of −2 dBm is shown in Fig. 19 for two input tones of 79 and 81 MHz. The measured IIP3 is 2 dB lower than the simulation result, which appears to be caused by the output buffer. Fig. 20 shows the IIP3 variations versus the continuous frequency tuning and temperature variation. Fig. 20(a) describes the variation of IIP3 values of the filter versus the continuous frequency tuning. The IIP3 variation over the tuning range is 0.6 dBm, which agrees with the characteristic described in Fig. 8, in which G_m tuning does not raise linearity

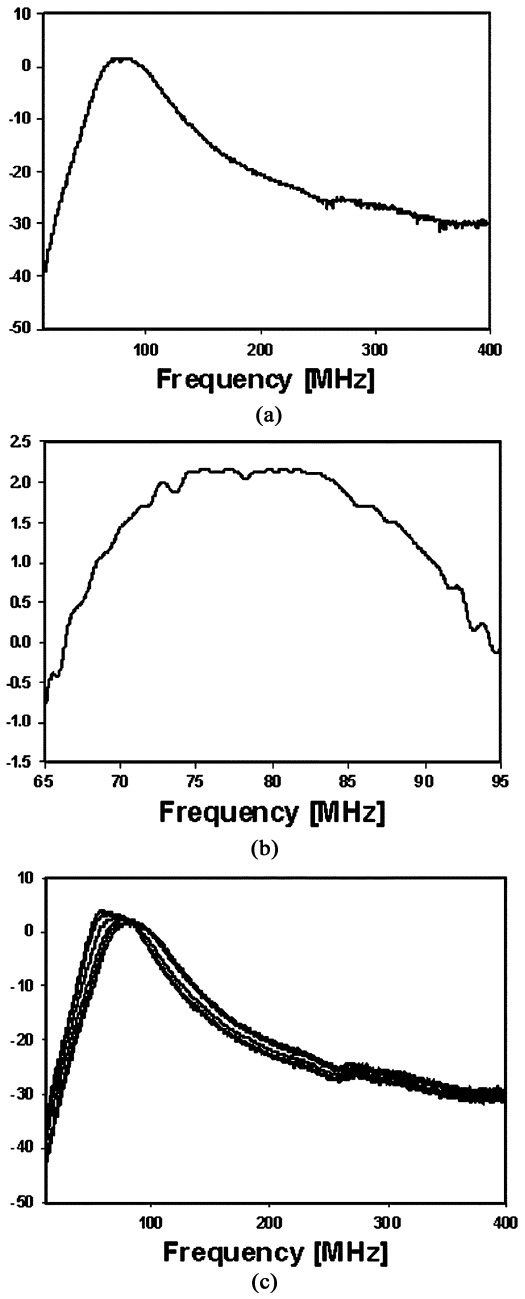

Fig. 16. Measured frequency response of the implemented filter. (a) Frequency response with 80 MHz center frequency. (b) Zoom-in pass-band of the frequency response. (c) Frequency response in continuous-time tuning.

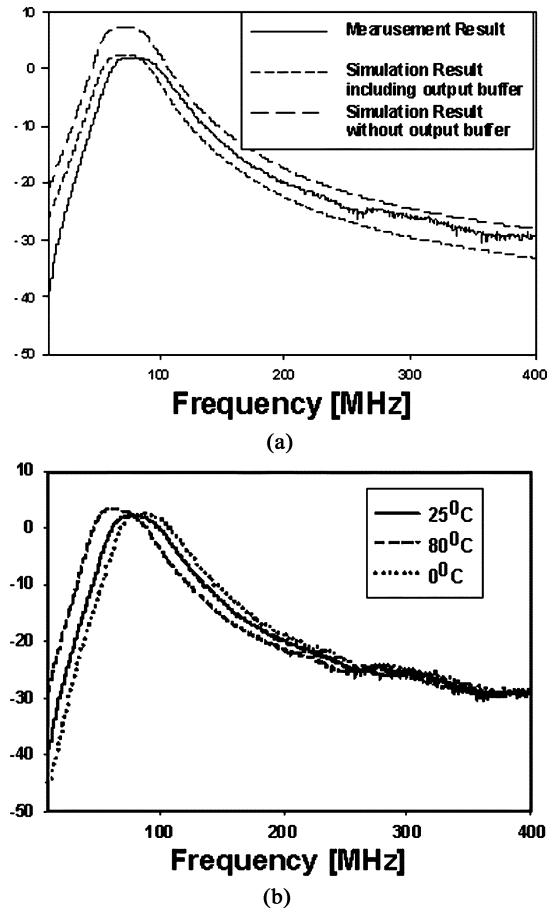

Fig. 17. (a) Measured frequency response of the filter versus simulation results. (b) Frequency responses over temperature range from 0°C to 80°C with samples at 0°C, 25°C, and 80°C.

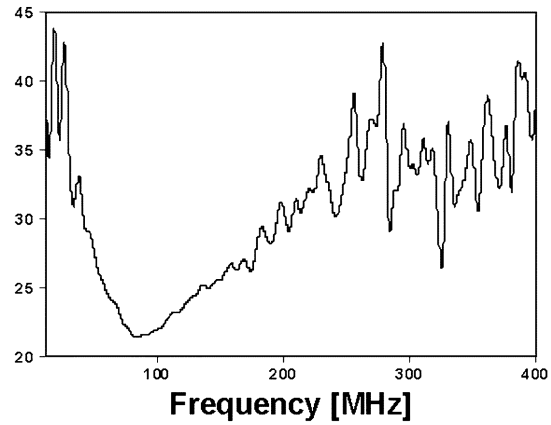

Fig. 18. Measured noise figure of the filter including output buffer.

problem. Fig. 20(a) shows the IIP3 variation versus temperatures which have been sampled in a range from 0°C to 80 °C in steps of 10 °C. The IIP3 values measured vary from −1.5 dBm to −3.2 dBm. The 1.7 dBm range of IIP3 variation agrees with the simulation shown in Fig. 9(b), where the G_m'' value does not change much as the temperature varies. Table I compares the performance of the implemented filter with those of other reported filters working under similar conditions. Compared to other works, this work has advantages of low power consumption, low noise figure, high IIP3, low in-band ripple and low supply voltage.

V. Conclusion

This paper has reported a linearization technique for transconductors used in a resonant-coupling G_m–C filter. The proposed transconductor is suitable for high-frequency applications which require a low voltage supply and a large input range. The achieved results show the advantages of flat bandpass and stable ac shape of the resonant-coupling structure.

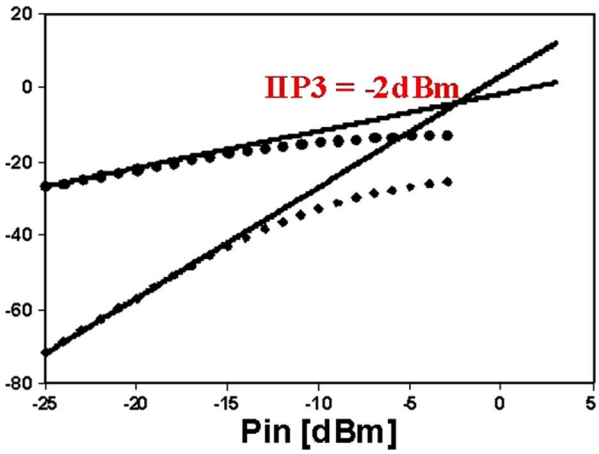

Fig. 19. Measured IIP3 of the filter with two tones of 79 MHz and 81 MHz at the input.

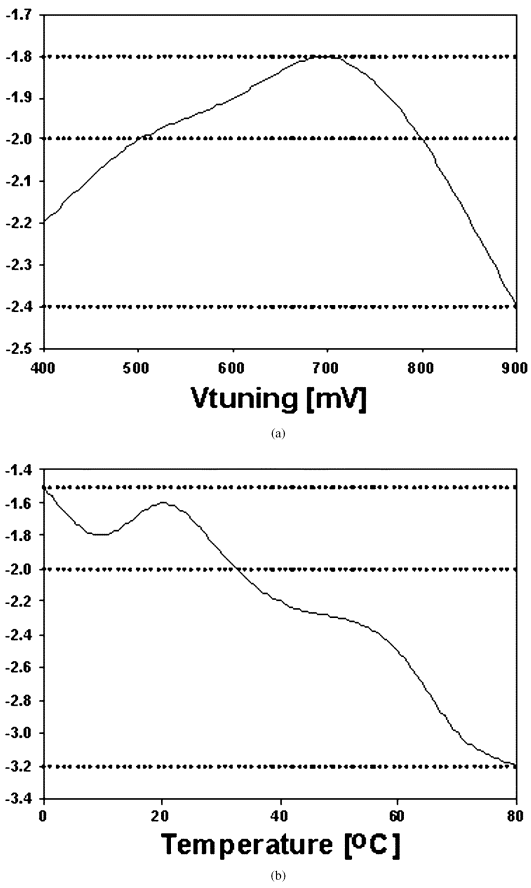

Fig. 20. Measured IIP3 variations versus the tuning voltages and temperatures (a) for the tuning voltage ranging from 400 mV to 900 mV, and (b) for the temperature variation.

The designed filter has advantages such as low power and integration in CMOS technology compared to SAW filter. Though the unwanted rejection ratio is achieved higher with SAW filter, the rejection ratio of the designed filter can be increased by adding some stages or by raising the value of the negative resistances. There is a trade-off in designing this type of filter that as the bandwidth of the filter increases, the flatness of the pass-band reduces. This is because of that the distance of the two poles created is too far to keep the in-band ripple small when the bandwidth increases. Three stages generating three poles solve this problem though it is more difficult to control the correlations between those poles. With good performance at 80 MHz, this work also promises other applications on higher frequencies with tuning systems.

TABLE I
FILTER PERFORMANCE PARAMETERS

	[17]	[18]	[19]	[20]	[21]	This work
Order	6	2	-	6	6	4
F_0 (MHz)	70	85	80	100	100	80
BW (MHz)	0.2	0.6	1.8-5	10	10	10
Pass-band gain (dB)	30	2-12	19.55	0	13.5	2
In-band ripple (dB)	-	-	-	4	-	0.1
IIP3 (dBm)	-10	-1	-2.8	-	2	-2
NF (dB)	46	-	-	-	-	21.5
Current (mA)	36	7.5	20	10	10	11
Technology	0.5μm HP	HF3 CMOS	0.25μm BiCMOS	0.6μm CMOS	90nm CMOS	65nm CMOS
Size	0.8×1.2 mm^2	-	0.6×0.6 mm^2	1.1×0.4 mm^2	-	0.5×0.5 mm^2
Supply Voltage (V)	2.5	±2.5	3.3	2.95	1.4	1.2

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