A Two-Channel Asynchronous SAR ADC With Metastable-Then-Set Algorithm

Sang-Hyun Cho, Chang-Kyo Lee, Sang-Gug Lee, and Seung-Tak Ryu

***Abstract*—A low power dual-channel asynchronous successive approximation register (ASAR) analog-to-digital converter (ADC) is presented. A metastable-then-set (MTS) algorithm is proposed with the aim of eliminating unnecessary decision operations in ASAR and its effects on power consumption and performance have been measured. The proposed flag synchronization technique minimizes the crosstalk between two asynchronous ADCs. A prototype ADC was implemented in 0.13-μm CMOS technology and operated under a 1.2 V supply. At a sampling rate of 17.5 MS/s, the ADC achieves a peak signal-to-noise and distortion ratio of 51.3 dB at 1.73 MHz input frequency. The measured total power dissipation of a single channel ADC is 570 μW and the figure of merit is 103 fJ/step.**

***Index Terms*—Asynchronous SAR, dual channel, metastability, metastable-then-set (MTS), SAR analog-to-digital converter (ADC).**

I. Introduction

As advanced CMOS technologies enhance the operational speed of microelectronics, successive approximation register (SAR) analog-to-digital converters (ADCs) have recently become a very popular ADC architecture, having a low power characteristic and utilizing new design techniques [1]–[7]. With this trend, recently reported SAR ADCs cover a wide range of performances (see Fig. 1) from low frequency applications such as wireless sensor networks (Group A) [5] to gigahertz applications including optical communications (Group C) [4].

Motivated by the various usages of SAR ADCs, this paper exploits an application of ASAR ADC in a two-channel design. The proposed metastable-then-set (MTS) algorithm eliminates unnecessary operations from the conventional ASAR operations and removes the speed bottleneck from the metastability. In order to reduce the crosstalk between the two asynchronous ADCs, a flag synchronization technique is proposed as well.

This paper is organized as follows. In Sections II and III, the proposed MTS algorithm and its implementation are explained. Section IV presents the overall architecture of the two-channel ADC with the flag synchronization technique. Section V discusses the measurement results and the effects of the MTS algorithm. Section VI concludes this paper.

II. MTS Algorithm

The self-triggering operation of ASAR ADCs removes the need for a high speed internal clock and speeds up the total conversion [2]. However, when the input to the comparator is very small, the latching operation suffers from metastability and conversion takes an unusually long time. Fig. 2(a) depicts a simple block diagram of a typical ASAR ADC with several important waveforms [see Fig. 2(b)]. Except for the first latching command ($\phi_{\rm latch}$), all the following latching operations are self-conducted by sensing the comparator output with an XOR function. The XOR sets the flag signal to notify the bit-decision completion when the output is regenerated. The time for the following operations such as digital-to-analog converter (DAC) settling is then defined by $\rm flag_{EXT}$ with fixed pulse width. As an example of the operation of the ASAR ADC, a sampled input signal ($V_{\rm SH}$) slightly higher than 3/4 $V_{\rm REF}$ is considered. After the MSB decision is completed, the MSB-1 bit decision takes place and it takes much longer time than others decisions due to the metastability ($V_{\rm DAC} \approx V_{\rm SH}$). The remaining LSBs are sequentially decided to be zeros by following the conventional SAR algorithm. In order to guarantee that the conversion is finished in a given time, the metastability problem must be resolved.

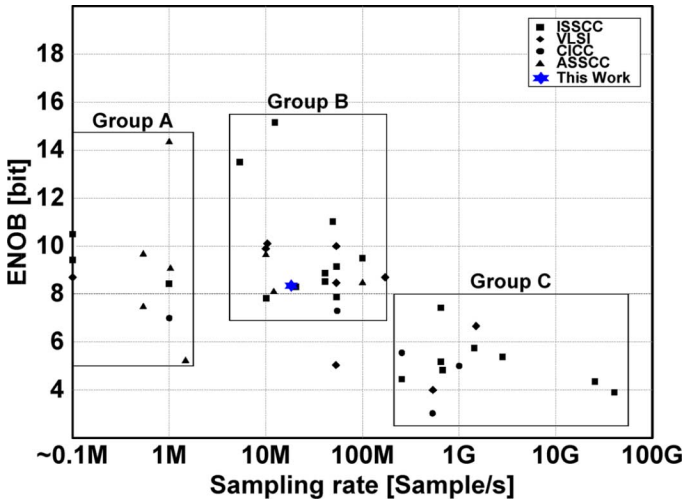

Fig. 1. Effective number of bits (ENOB) versus sampling rate of SAR ADC: papers from major conferences within the past 9 years.

Unlike other designs that try to conduct all the decision cycles [2] or assign unresolved codes after conversion [12], the proposed metastable-then-set (MTS) algorithm sets unresolved codes on chip and completes the conversion when metastability is detected. By doing this, the MTS algorithm prevents the metastability from reducing the conversion speed and eliminates unnecessary decision cycles. Fig. 3 shows the modified block diagram of the ASAR ADC with a metastability detector (MD) for implementation of the MTS algorithm [see Fig. 3(a)] and its waveforms [see Fig. 3(b)]. $T_{\rm meta}$ from the ASAR logic rises with $\phi_{\rm latch}$. $T_{\rm meta}$ has a fixed pulse width of $t_{\rm MTS}$, which becomes the reference for the metastability decision. If the flag does not turn on before $t_{\rm MTS}$ has passed, the MD considers the ADC to be in a metastable state. The MSB-1 bit decision phase in Fig. 3 is in this situation. Once metastability is detected, the MTS algorithm sets the unresolved codes to $100\ldots0$ and completes the conversion.

The MTS algorithm eliminates all the following decision cycles after the occurrence of metastability. If the comparator enters metastable status when its input is less than α-LSB, the LSB decision cycle is eliminated with a probability of $\alpha/2$ due to the metastability occurring in the (LSB + 1) bit decision. This reduces the decision cycles by a factor of $(\alpha/2)\times(1/N)$ in an N-bit ADC. Similarly, the metastability that occurs in the (LSB + 2) bit decision eliminates two decision cycles of LSB + 1 and LSB with a probability of $\alpha/4$; therefore, the decision

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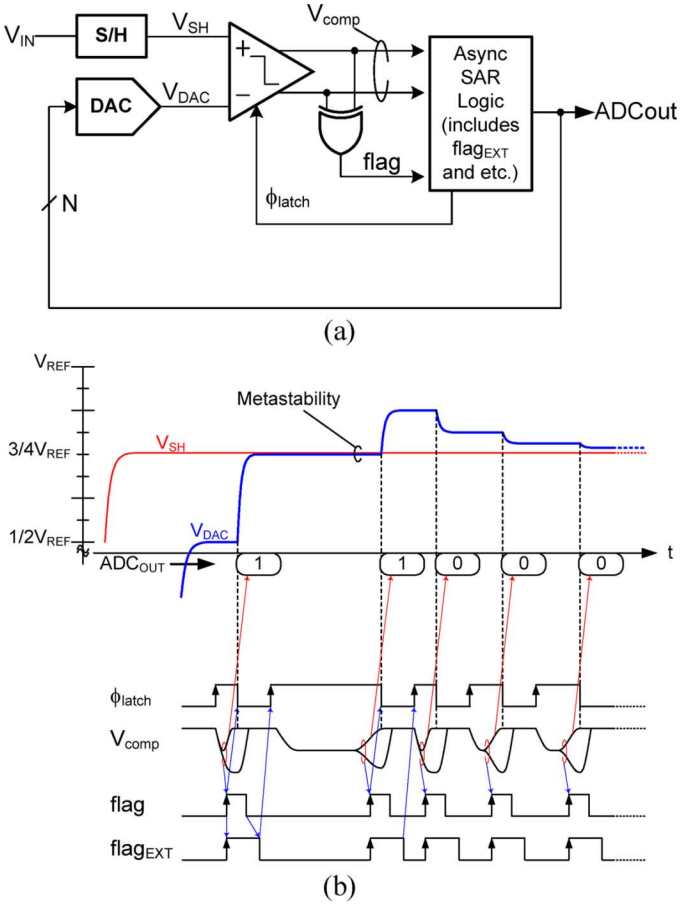

Fig. 2. (a) Block diagram of an asynchronous SAR ADC and (b) its timing diagram.

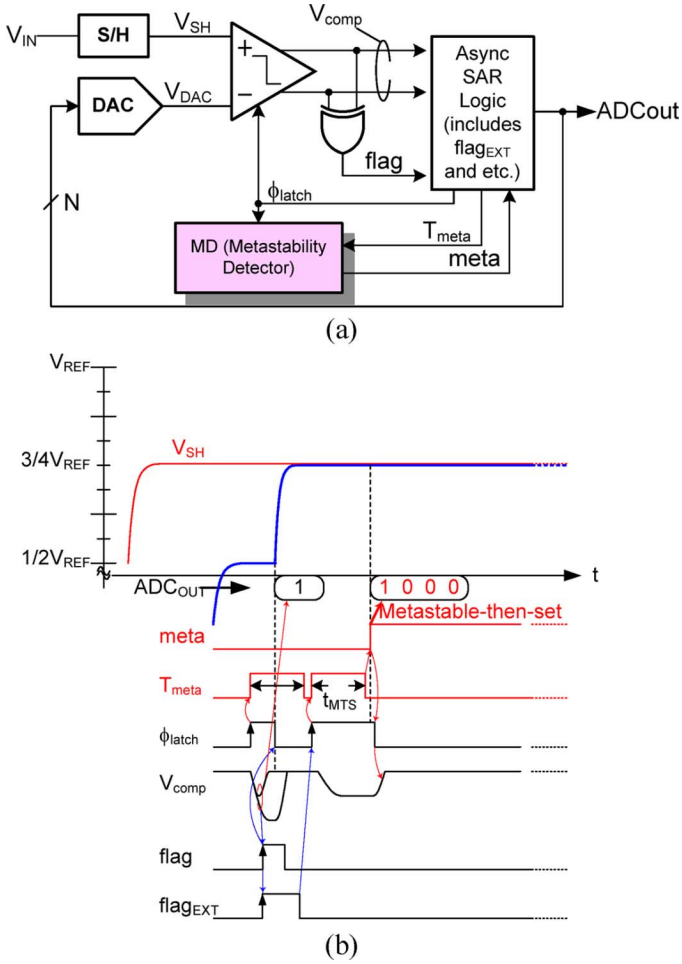

Fig. 3. (a) Modified asynchronous SAR ADC for the MTS algorithm and (b) its timing diagram.

cycle is reduced by a factor of $(\alpha/4)\times(2/N)$. As a result, the decision cycle saving factor (DCSF) can be defined as

$$\mathrm{DCSF}=\sum_{k=1}^{N-1}\frac{\alpha}{2^k}\frac{k}{N}. \tag{1}$$

The saved decision cycles owing to the MTS algorithm in a 10 bit design is approximately 10% when α is 0.5. Even though the amount of saved cycles may not be substantial, this savings is almost free and, moreover, the algorithm guarantees complete conversion in a given time in spite of the metastability. Note that the MTS algorithm is more effective in low resolution ADCs based on (1). Also, any power consumption proportional to the number of cycles such as that from the control logic is reduced by as much as that in (1). However, considering that the range of the metastability depends strongly on the PVT variations, it might be desirable to design α to be less than 0.5 to guarantee linearity.

III. MTS Implementation

In order to validate the MTS algorithm at a prototype level, an MD block was designed with the operational principle shown in Fig. 4. T_{meta} with a constant pulse width of t_{MTS} in Fig. 3(b) is replaced by a ramp signal (ramp) for test purposes. The ramp rises with ϕ_{latch}; if the ramp reaches a decision threshold (V_{TH_meta}) before the latching is complete (falling of ϕ_{latch}), i.e., before the flag appears, then the situation is considered to be metastable and the meta signal turns on. Thus, the time when ramp meets V_{TH_meta} is defined as t_{MTS}. The

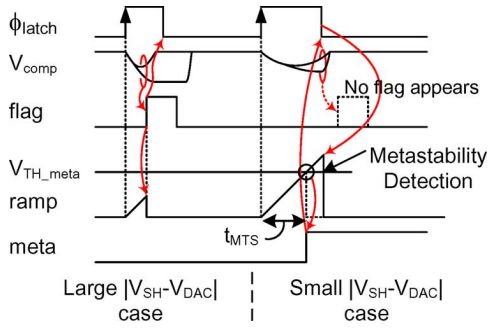

Fig. 4. MTS implementation-based ramp generation for testability.

ramp signal is reset when the flag (in normal conversion) or meta (in metastable status) appears. t_{MTS} is a key variable to control α, as explained in Section II, and it is adjusted externally by changing the slope of the ramp. By increasing the slope of the ramp under a fixed V_{TH_meta}, t_{MTS} reduces and α increases.

Fig. 5(a) shows the hardware implementation of the MD explained above. The ramp generator has a simple integrator composed of a current source (I_{MD}) and a capacitor (C_{MD}). At the rising edge of ϕ_{latch}, the integrator begins to charge C_{MD}. Integration finishes either when flag $=1$ (decision completion) or when metastability is detected (when node A reaches the logic threshold of the following inverter, inv_1). Here, the logic threshold of inv_1 plays the role of V_{TH_meta} in

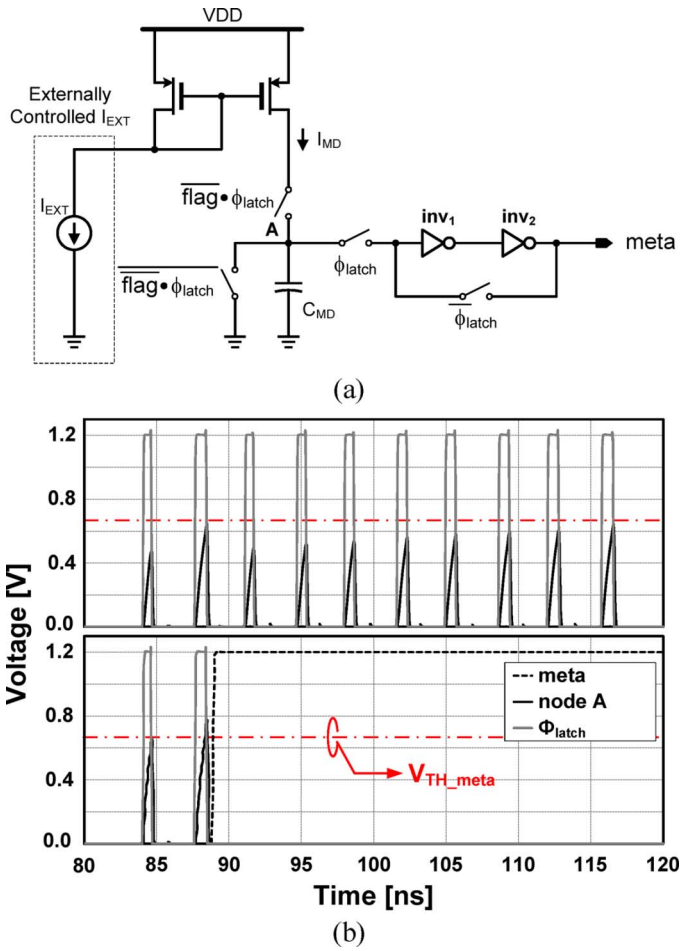

Fig. 5. (a) Hardware implementation of metastable detector and (b) its simulation result: transient simulation waveforms of the metastable-status detector in the case (upper) without metastable-status occurrence and (lower) with metastable-status occurrence.

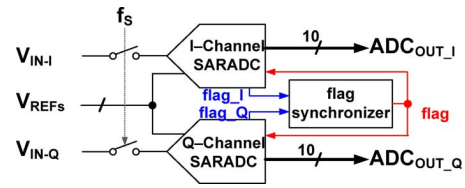

Fig. 6. Overall architecture of the two-channel ADC.

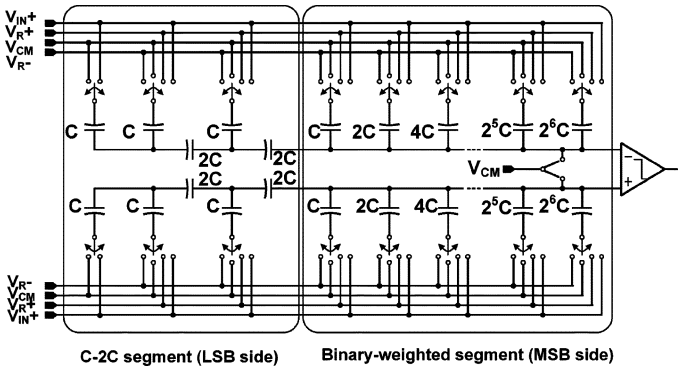

Fig. 7. 10 b DAC architecture in the prototype ADC.

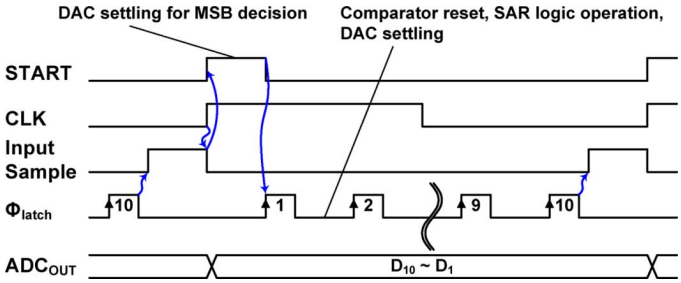

Fig. 8. Timing diagram for the MTS SAR ADC.

Fig. 4, and the value is approximately half the supply voltage. When metastability is detected, a latch composed of inv_1 and inv_2 holds the $\mathrm{meta} = 1$ until the next input is sampled. The amount of I_{MD} is controlled externally to control the slope of the ramp.

Fig. 5(b) shows the simulation waveforms of the MD in Fig. 5(a) for two cases: (upper waveform) without and (lower waveform) with metastability occurrence. The lower waveform verifies that the metastability is detected when node *A* touches V_{TH_meta}, and as a result, the remaining decisions are omitted with no further latching commands.

IV. Overall Architecture

A dual channel 10 b SAR ADC based on the MTS algorithm is implemented. Fig. 6 shows the overall architecture: it is composed of two ADCs that share common voltage references and a flag synchronizer.

A. Capacitor DAC

Each ADC in the prototype employs a segmented binary-weighted capacitor DAC, as shown in Fig. 7. Segmentation is undertaken from the LSB side to reduce the impact of the parasitic effect. Considering the capacitor matching requirements and the effect of the parasitic capacitances of the floating capacitors (2C) on the DAC linearity, two C-2C ladders are used in the LSB segments after the behavioral-level yield estimation. The total capacitance of the DAC is around 5.2 pF with a unit capacitor of 40 fF. The DAC has only a 9 bit configuration owing to use of the power efficient tri-level straightforward DAC switching method [8], [9].

B. Timing Diagram

Fig. 8 shows the timing diagram of the designed single channel ADC. The external clock (*CLK*) triggers a start up pulse generator ($\mathrm{START} = 1$) [not shown in the block diagram in Fig. 3(a)]. While $\mathrm{START} = 1$, the preparation for the MSB decision is complete. At the falling edge of START, the comparator starts to resolve the MSB with a rising edge of ϕ_{latch}. Except for the MSB, the remaining decisions are self-triggered, as explained in Section II. Note that, in this design, the ADC begins to sample the input signal (*Input Sample*) as soon as the last bit decision (10th ϕ_{latch}) completes, unlike the conventional designs in [10] and [11] where the sampling timings are defined by the duty cycle controlled external clock. Thus, the proposed sampling method is more practical, because the clock is not required to have any specific duty. Note that when metastability occurs, the meta directly sets *Input Sample* signal for the next input sampling.

C. Dual Channel ADC

For good matching performance between the two ADCs, voltage references (V_{R+}, V_{CM}, and V_{R-} in Fig. 7) are shared by both ADCs.

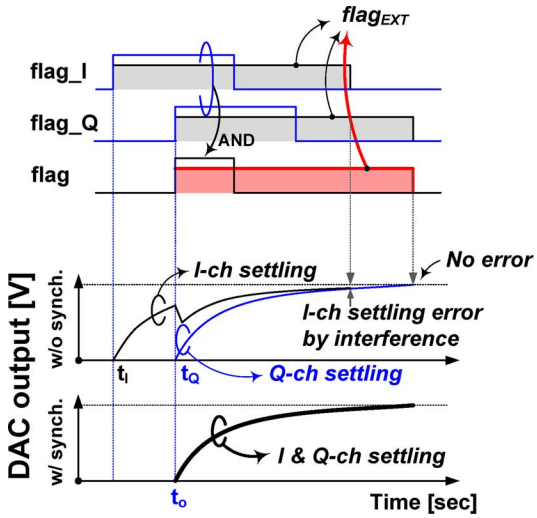

Fig. 9. Effect of the flag synchronizer.

Special care is required in sharing references for two asynchronously operating ADCs. If the DAC of the Q-channel starts to charge its capacitors when the DAC settling of the I-channel is almost completed, the settling accuracy of the I-channel will be significantly degraded. Therefore, the charging operations of the two DACs need to be synchronized. For this, a flag synchronizer was implemented, as illustrated in Fig. 6. Fig. 9 depicts the operation of the flag synchronizer. The synchronizer takes two flag signals from both ADCs ($flag\_I$ and $flag\_Q$) and generates a common flag signal. The DAC operations of the two ADCs are controlled by this common flag. Due to this modification, the ASAR logic in the ADC core is slightly modified. By doing this, the two DACs begin to settle simultaneously and no interference occurs from the reference voltages. When metastability occurs, a meta signal must be used instead of $flag\_x$, where x is I or Q, i.e., $\text{flag} = (\text{flag}\_I + \text{meta}\_I) \cdot (\text{flag}_Q + \text{meta}\_Q)$. Note that this solution constitutes a trade-off between the conversion speed and settling accuracy. A behavioral simulation shows that the flag synchronization method can reduce the conversion speed of a single channel ADC by a maximum of 10%. Comparator offset mismatch was not considered in the design, because this kind of static error can be easily corrected by post-processing.

V. Measurement Results

A. General Measurements

A prototype dual-channel 10 b SAR ADC has been fabricated in a 0.13-μm CMOS technology. A chip photo is shown in Fig. 10. The active area of the single-channel ADC is 500×700 μm^2 and the dual-channel occupies 500×1550 μm^2. The measured frequency spectrum of a single channel ADC while the other channel is in normal operation is shown in Fig. 11. The input frequency is 1.73 MHz and the sampling rate is 17.5 MS/s. Fig. 12 shows the dynamic performances measured at 17.5 MS/s with three input frequencies: 1.75, 5, and 8 MHz. The measured peak signal-to-noise and distortion ratio is 51.3 dB. Considering the 10 b design, the results are poorer than expected. The major reason for this was found in the layout: In the DAC array shown in Fig. 7, the 2C capacitor in the binary-weighted segment has quite long bottom plate routing compared with other capacitors. This long routing metal of 2C in conjunction with the common top-plate routing significantly increased its actual value, and as a result, this limited the measured linearity to 8 b in DNL. The total power consumption of the single channel ADC is 570 μW under a 1.2 V supply at 17.3 MS/s. The measured ENOB is 8.3 b and the figure of merit is 103 fJ/conversion-step. The performance is summarized in Table I.

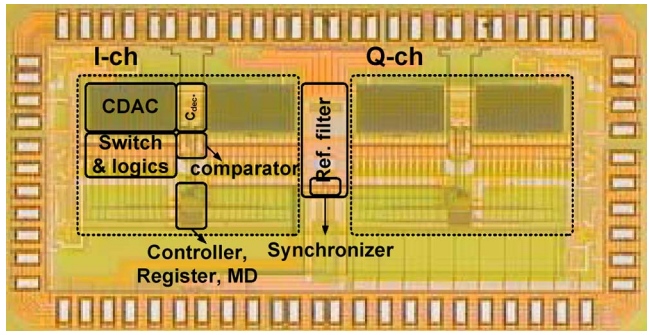

Fig. 10. Chip photograph.

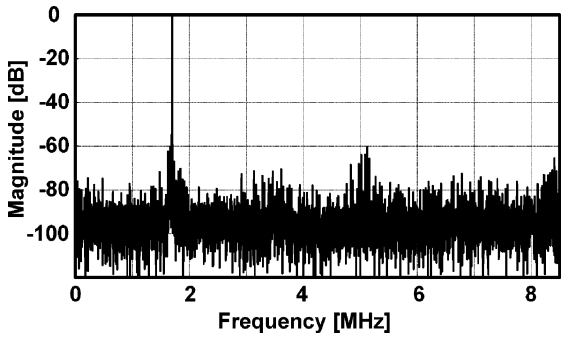

Fig. 11. Measured FFT result for 1.73 MHz signal at 17.5 MS/s ($t_{\text{MTS}} = 1.1$ ns).

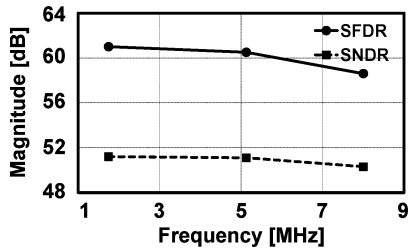

Fig. 12. Input frequency sweep at 17.5 MS/s ($t_{\text{MTS}} = 1.1$ ns).

TABLE I
Summary of Measurements

Process	CMOS 0.13 µm	
Active Area (single)	500x1550 (500x700) µm^2	
Sampling Rate	17.5 MS/s	
Power Consumption (single channel)	Analog	66 µW @ 1.2 V
	Digital	372 µW @ 1.2 V
	DAC Switching	132 µW @ 1.2 V
	Total	570 µW @ 1.2 V
ENOB	8.3 bits	
FOM	103 fJ/conv. step	

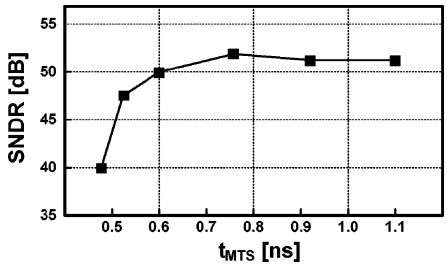

Fig. 13. Dynamic performance according to change of t_{MTS}.

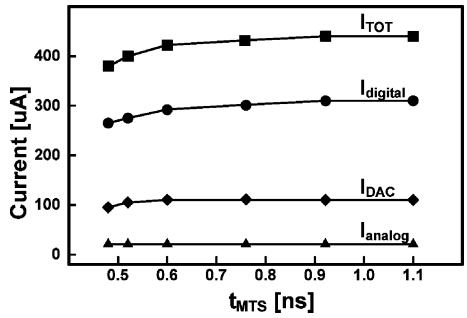

Fig. 14. Current consumption according to change of t_{MTS}.

B. Verification of the MTS Algorithm

In addition to resolving the metastability problem, the MTS algorithm reduces the number of decision cycles. As α is increased, greater savings of decision cycles is expected, and further power reduction is thus anticipated (at the cost of performance degradation after some point). These effects were measured under variation of the metastability decision time, t_{MTS}, by sweeping the integrator current (I_{MD}) in Fig. 5. The measured SNDR performance and the current consumption with respect to t_{MTS} are shown in Figs. 13 and 14, respectively. When t_{MTS} is as low as 0.6 ns, the SNDR degradation is approximately 1.1 dB with 18 μA total current (I_{TOT}) savings. Further reduction of t_{MTS} significantly reduces SNDR, although the current is saved further. Since the current drawn by the digital block (I_{digital}) is proportional to the number of decision cycles, the effect on I_{digital} is dominant. On the other hand, the current savings from the DAC switching (I_{DAC}) is not as significant, because the probability of metastability occurrence in the MSB decision is very low and the power consumption in the LSB decision cycles is not significant due to low capacitances. The power savings effect of the MTS on the analog block (I_{analog}) is negligible since the current amount by the comparator is as low as 20 μA. The power savings effect by the MTS technique with this 10 b prototype ADC is not as significant. Thus, low power MD design is also important. This can be accomplished by using delay cells instead of an integrator in order to remove static power consumption. Even in this case, the dynamic power consumption should be considered as well. When (1) and Figs. 13 and 14 are considered, a better power savings effect is expected in a lower resolution ADC, because the percentage of omitted decision cycles by MTS increases and greater performance degradation is allowable.

VI. Conclusion

This paper investigates the potential usage of an ASAR ADC for a dual-channel ADC with solutions for metastability and crosstalk. The MTS algorithm not only solves the metastability problem but also shows possible power savings. The flag synchronization technique reduces the crosstalk between two channels and makes it possible to share a common reference for better dynamic performance.

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