A Passive Mixer for a Wideband TV Tuner

Viet-Hoang Le, Hoai-Nam Nguyen, In-Young Lee, Seok-Kyun Han, and Sang-Gug Lee

***Abstract*—This brief presents the design of a direct conversion mixer for a wideband television tuner operating at 48–860 MHz. The mixer consists of a transconductance stage, a passive current switching stage, and a transimpedance amplifier stage. In the switching stage, by adopting an opposite phase auxiliary switching quad configured in parallel with the main switching quad, the unwanted harmonics at the output of the switching stage are suppressed, thereby preventing mixer linearity degradation at low input frequencies. The proposed mixer is implemented in a 0.13-μm CMOS technology, and measurements show more than a 19.5-dB voltage gain, 12-dB noise figure, and 8-dBm IIP3 over the entire operating band of 48–860 MHz while dissipating 4.5 mA from a 1.2-V supply.**

***Index Terms*—CMOS mixer, current switching mixer, harmonic suppression, high linearity, passive mixer, television (TV) tuner, wideband mixer.**

I. Introduction

With the introduction of digital broad-band television (TV) services, the quality of TV images has been remarkably improved, as shown in the case of enhanced/high-definition TV. Digital broadcasting also allows mobile reception. With these developments, there is increased demand for smaller TV tuners that consume less power while providing higher performance and high data rates, as well as for handheld TV receivers.

TV tuners need to cover a wide frequency range of 48–860 MHz, creating a problem of strong interference due to crowded channels. Hence, the receiver should have good linearity in order to suppress the intermodulation interference and thereby ensure a sufficient signal-to-noise ratio. In the receiver chain, the mixer is the last block of the radio-frequency (RF) front end and tends to dominate the receiver linearity performance. High linearity is a key performance requirement for the mixer. Depending on the bias current of the switching stage, mixers can be classified as either active or passive types. Recently, passive mixers have been widely adopted for direct conversion (DC) receivers owning to their flicker-noise-free characteristic [1], [2]. This brief presents a DC passive mixer that adopts a novel feedforward cancellation scheme in order to improve linearity performance for a wideband TV tuner.

Manuscript received November 23, 2010; revised March 9, 2011; accepted April 16, 2011. Date of publication July 5, 2011; date of current version July 20, 2011. This work was supported by a National Research Foundation of Korea (NSF) grant funded by the Korean Government [Ministry of Education, Science and Technology (MEST)] (Grant No. 2010-0018899). This paper was recommended by Associate Editor A. Liscidini.

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Digital Object Identifier 10.1109/TCSII.2011.2158262

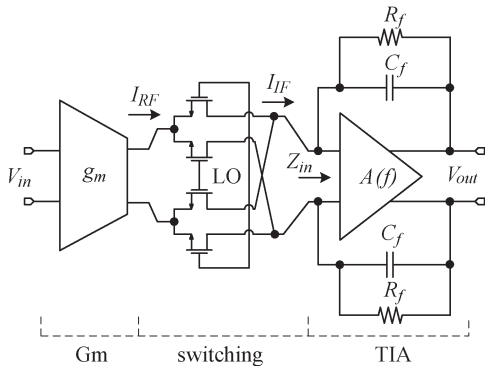

Fig. 1. Block diagram of conventional passive mixer.

The mixer described in this brief is for a conventional DC TV tuner but is not limited for other architecture tuners. This brief is organized as follows: Section II briefly explains the nonlinearity sources in the mixer and describes the operation of the conventional/proposed current passive mixer. Section III presents the simulated and measured results of the implemented chip, and Section IV concludes this brief.

II. Circuit Designs

A block diagram of the conventional current switching passive mixer is shown in Fig. 1, The mixer consists of a transconductance (Gm) stage, a switching stage, and a transimpedance amplifier (TIA) stage.

The overall voltage conversion gain of the mixer in Fig. 1 can be expressed as [3]

$$\frac{V_{\rm out}(f_{\rm out})}{V_{\rm in}\,(f_{\rm in})} \approx \frac{2}{\pi} g_m \left(\frac{R_f}{1 + j2\pi f_{\rm out} R_f C_f} \right) \tag{1}$$

where $f_{\rm out}$ is the output frequency at intermediate frequency (IF), $f_{\rm in}$ is the input RF, g_m is the total transconductance of the Gm stage, and R_f and C_f are the feedback resistor and capacitor of the TIA, respectively. In this architecture, the time-domain output current of the switching stage can be expressed as follows:

$$I_{\rm IF} \approx \frac{2}{\pi} g_m \cos(\omega_{\rm RF} - \omega_{\rm LO})t + \frac{2}{\pi} g_m \cos(\omega_{\rm RF} + \omega_{\rm LO})t + \sum_{n=3,5,7\ldots}^{\infty} \frac{1}{n} \frac{2}{\pi} g_m \cos\left(\omega_{\rm RF} \pm n\omega_{\rm LO}\right) t. \tag{2}$$

In (2), the first term is the wanted IF, whereas the remaining terms are the unwanted signals. In the switching stage, there are two major sources of distortion: device nonlinearities and phase modulation of the switching instants [4], [5]. The first source is the nonlinearities of the switching transistors, whereas

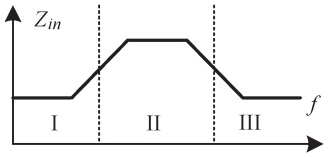

Fig. 2. TIA's input impedance behavior.

the second source is the phase modulation of the switching operation by strong RF or unwanted perturbation signals [4], [5]. In this mixer architecture, the TIA should provide low input impedance so as to avoid large voltage perturbation at the output of the switching stage, and the mixer's linearity can be thereby maintained. The input impedance of the TIA can be expressed as

$$Z_{\rm in} = \frac{Z_f(f)}{A(f)+1} = \frac{1}{A(f)+1}\left(\frac{R_f}{1+j2\pi R_f C_f}\right) \quad (3)$$

where $Z_{\rm in}$ is the input impedance of the TIA, $Z_f = R_f//C_f$, and $A(f)$ is the forward voltage transfer function of the operational amplifier (op-amp) in the TIA. Because of the limited bandwidth of the op-amp, $A(f)$ decreases with frequency. Hence, the input impedance of the TIA initially increases with frequency, starting at around 5 MHz in this design [3], [6]. Then, due to $Z_f(f)$, which decreases with frequency, the input impedance levels off and becomes flat; this starts occurring at around 50 MHz. At even higher frequency (beyond 200 MHz), the input impedance starts to decrease due to parasitic capacitance shown at the input of the TIA. The qualitative behavior of the input impedance of the TIA is described in Fig. 2 [3], [6]. When the RF is more than 200 MHz, the unwanted frequencies [RF leakage, RF+local oscillator (LO)] fall into region III in Fig. 2. In this region, as shown in the figure, the input impedance of the TIA is low, and thus, the perturbation voltage swing at the output and input of the switching stage is small and does not affect the switching operation. When the RF is in a range of 50–200 MHz, the unwanted frequencies (RF leakage, LO+RF) fall into region II in Fig. 2, leading to significant perturbation voltage at the output and input of the switching stage. This large voltage perturbation affects the mixer's switching operation and leads to degradation of the linearity.

A block diagram of the proposed current switching passive mixer is shown in Fig. 3. The switching stage of the proposed mixer has an additional switching quad, as compared with the conventional mixer. In this architecture, the Gm stage, main switching quad, and TIA operate in the same manner as in the conventional architecture. As shown in Fig. 3, the auxiliary switching quad is identical to the main switching quad but configured with opposite polarity. The auxiliary switching quad also performs frequency conversion, such as the main switching quad, and all the high-frequency signals appear at the output with opposite polarity, except for the wanted low IF, which is blocked by capacitor C_b. Thus, all the high-frequency signals at the output of the switching stage are cancelled, but the wanted low IF remains.

From Fig. 4, assuming that the output impedance of the main $(Z_{\rm main})$ and auxiliary $(Z_{\rm aux})$ switching quads are resistive (R_0) and the input impedance of the TIA $(Z_{\rm in})$ is very small, then the Gm and the switching stage can be modeled as a voltage-controlled current source with output impedance, as shown in Fig. 4, where $I_{\rm IF} \approx (2/\pi) g_m V_{\rm RF}$ and $Z_{\rm main} = Z_{\rm aux} = R_0$. In Fig. 4, the TIA is modeled as a current-controlled voltage source $V_{\rm IF}$, which is equal to $I_{bb}(R_f/1 + j2\pi f_{\rm out} R_f C_f)$. From Fig. 4, output current I_{bb} of the switching stage can be given by

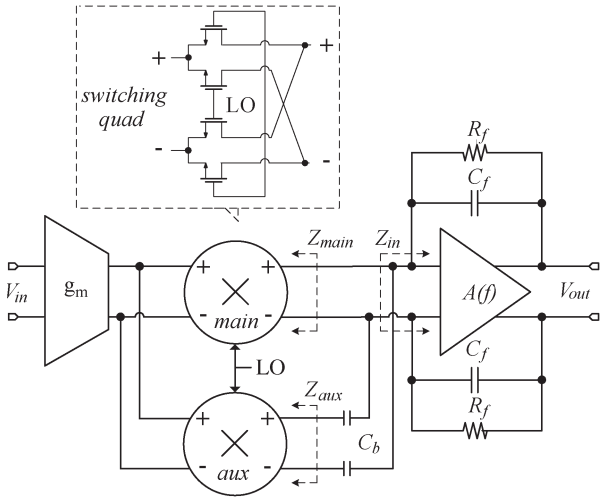

Fig. 3. Block diagram of the proposed passive mixer.

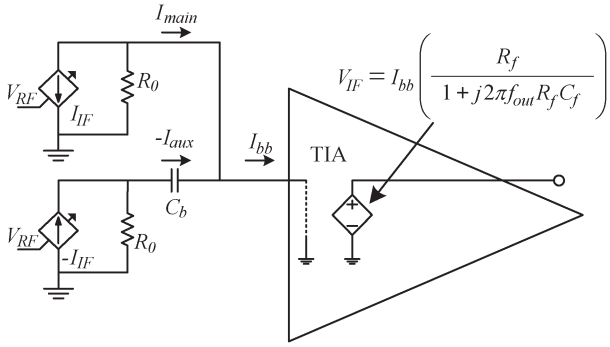

Fig. 4. Equivalent circuit of the proposed mixer.

$$I_{bb} = I_{\rm main} - I_{\rm aux} \approx I_{\rm IF} - I_{\rm IF}\left(\frac{R_0}{R_0 + \frac{1}{j2\pi f_{\rm out} C_b}}\right) = I_{\rm IF}\left(\frac{1}{1+j2\pi f_{\rm out} R_0 C_b}\right) \quad (4)$$

where $I_{\rm main}$ and $I_{\rm aux}$ are the output current from the main and auxiliary switching quads, respectively, and C_b is the blocking capacitor. The overall voltage conversion gain of the proposed mixer can be then given by

$$\frac{V_{\rm out}(f_{\rm out})}{V_{\rm in}(f_{\rm in})} \approx \frac{2}{\pi} g_m \left(\frac{1}{1+j2\pi f_{\rm out} R_0 C_b}\right)\left(\frac{R_f}{1+j2\pi f_{\rm out} R_f C_f}\right). \quad (5)$$

Compared with (1), output baseband voltage $V_{\rm out}(f_{\rm out})$ in (5) experiences a second-order low-pass filtering, which provides a higher amount of attenuation for the high-frequency

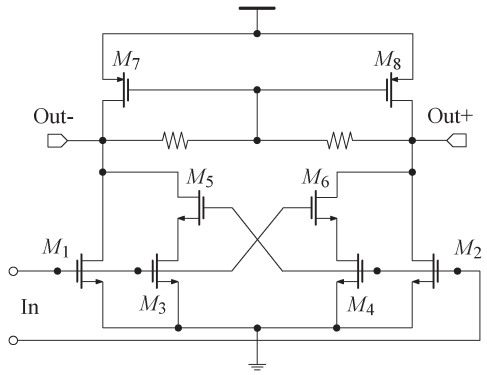

Fig. 5. Simplified circuit schematic of the Gm stage.

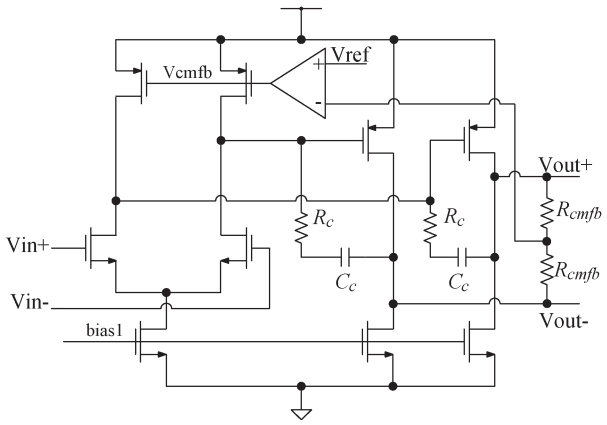

Fig. 6. Simplified circuit schematic of the op-amp for the TIA.

unwanted signals, including the third-order intermodulation harmonic. As a result, the mixer's IIP3 is improved.

In this design, while R_0 is the output impedance of the Gm stage and depends on the structure of g_m, C_b can be a design parameter chosen to decide the cutoff frequency of the low-pass filter. The output impedance of the Gm stage can be varied within a range from several hundreds to a kiloohm. Therefore, the value of C_b can be chosen from 15 to 100 pF to achieve 3-dB bandwidth of 10 MHz. In this design, to reduce chip size and avoid wanted signal gain reduction, C_b is chosen as a large-enough value of 10 pF to sufficiently suppress the unwanted harmonics. R_f and C_f are chosen as 1 kΩ and 4 pF, respectively.

Fig. 5 shows a simplified circuit schematic of the Gm stage, where the main differential pair consists of transistors M1 and M2. The auxiliary circuit, which consists of M3–M6, creates a third-order distortion that cancels the distortion of the main differential pair, which leads to better linearity [7]. The transistor sizes of M1–M6 are all chosen as 16 μm at the minimum channel length, whereas the size of M7 and M8, respectively, is 32 μm at the minimum length, and every transistor's bulk is connected to its own source. The Gm stage is designed to dissipate 2.7 mA from a 1.2-V supply.

A simplified circuit schematic of the op-amp for the TIA is shown in Fig. 6. The amplifier has a simple conventional two-stage topology with a common-mode feedback circuit. All the transistors' bulks are connected to a common ground. The op-amp draws 1.8 mA from a 1.2-V supply.

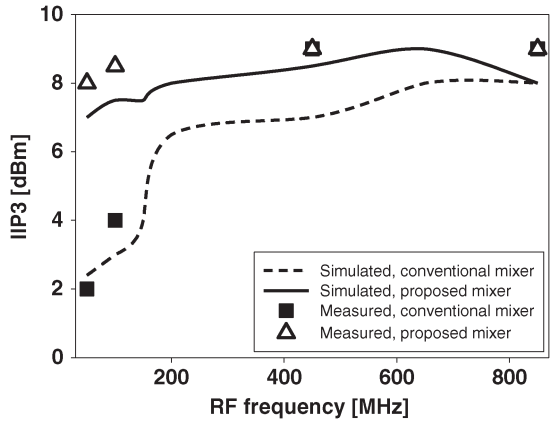

Fig. 7. Simulated and measured IIP3s of the conventional and proposed mixers.

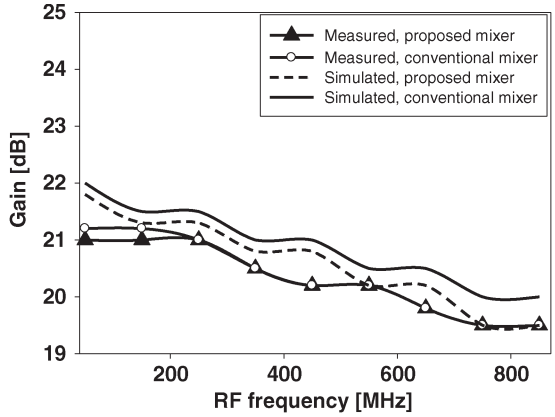

Fig. 8. Simulated and measured gains of the conventional and proposed mixers.

III. Simulation and Measurement Results

The proposed mixer is implemented in a 0.13-μm CMOS process. Baluns are used to convert single-ended to differential at the input, output, and LO of the mixer. An external 100-Ω resistor was placed in parallel with the mixer RF input to provide input matching for measurement purposes [3]. However, the increase in noise figure (NF) caused by this resistor is excluded in the simulated/measured results presented in this brief. In the measurement, the external LO power level is -2 dBm.

Fig. 7 shows the simulated and measured IIP3s of the conventional (see Fig. 1) and proposed (see Fig. 3) mixers. The IF is fixed in this measurement. A two-tone intermodulation test is performed, where the RF signals are $f_{\rm RF}$ and $f_{\rm RF} + (1$ MHz$)$, and the LO frequency is set to be $f_{\rm RF} - (2.5$ MHz$)$. The down-converted fundamental tone is at 2.5 MHz, and the third-order harmonic tone third-order intermodulation (IM3) is at 4.5 MHz. In this test, $f_{\rm RF}$ is swept from 48 to 860 MHz. The mixer's IIP3 results of all the bands in the operating frequency range (48–860 MHz) are then calculated, and the results are presented in Fig. 7. As shown in Fig. 7, for the RF input frequency below 200 MHz, the IIP3 of the conventional mixer starts to significantly degrade, whereas in the proposed mixer, the IIP3 remains nearly the same as that at high frequency. Fig. 8 shows the simulated and measured gains of the conventional and proposed mixers. In Fig. 8, the gain of the proposed mixer is slightly

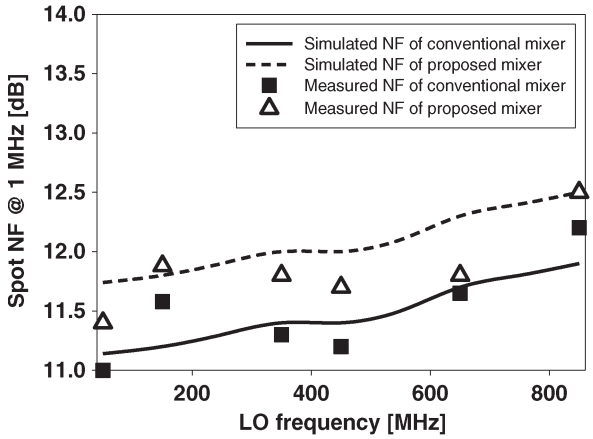

Fig. 9. Simulated and measured NFs (at 1 MHz) of the conventional and proposed mixers.

TABLE I
SUMMARY OF THE COMPARISON OF MIXER PERFORMANCES

	Proposed mixer	Conventional mixer	[8]	[9]
Frequency [MHz]	48~860	48~860	48~860	48~860
Gain [dB]	19.5~21	19.5~21.3	35	1~3
Noise Figure [dB]	11.4~12.4	11~12.2	8	13.5
IIP3 [dBm]	8~9	2~9	-15	12.3
DC Power [mW]	5.4	5.4	~	34.8
Technology [μm]	CMOS 0.13	CMOS 0.13	CMOS 0.18	CMOS 0.09

reduced at high RFs due to additional parasitic capacitances caused by the auxiliary switching quad. Fig. 9 shows the simulated and measured NFs of the conventional and proposed mixers. The measurement of the NF of the mixer is double sideband (DSB); the result is a spot DSB NF at an IF of 1 MHz, whereas LO is swept to cover the whole frequency band of interest. Due to the additional parasitic capacitances created by the auxiliary switching quad, the proposed mixer shows a 0.7-dB higher NF than that of the conventional mixer [3]. As shown in Figs. 7–9, overall, the measurement results are in good agreement with the simulation results. Table I summarizes the performances of the proposed mixer in comparison with that of the conventional mixer and those in other works. Compared with the conventional mixer, the proposed mixer shows a 3- to 6-dB improvement in the IIP3 values at low operating frequencies (below 200 MHz) at a cost of a 0.7-dB higher NF and 0.3-dB lower gain. The mixer reported in [8] showed higher gain but much worse linearity performance, whereas that in [9] shows very low gain and a higher NF in comparison with the proposed mixer.

Fig. 10 shows the chip microphotograph, where the chip size is 0.1 mm^2, excluding the pads.

IV. CONCLUSION

A current switching passive mixer for a TV tuner has been presented. The issue of mixer linearity degradation at low-frequency input is addressed and is found to be due to the presence of unwanted harmonics at the output of the switching stage. The proposed mixer eliminates the harmonics by adopting an identical auxiliary switching quad in parallel with the main switching quad but configured in the opposite phase so as to subtract unwanted harmonics at the output of the switching stage. Compared with the conventional mixer, the proposed mixer shows 3- to 6-dB improvement in the IIP3 values at low RFs (46–150 MHz) at the cost of a very small amount of gain and NF degradation. The measured IIP3 of the mixer is more than 8 dBm over the entire frequency band of 48–860 MHz while showing a conversion gain of more than 19.5 dB and an NF of less than 12.4 dB. The mixer dissipates 4.5 mA from a 1.2-V supply.

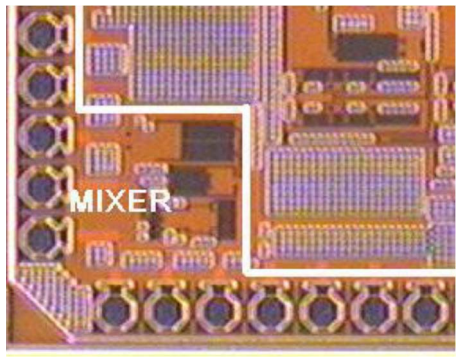

Fig. 10. Chip microphotograph of the proposed mixer.

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