Letters

An Integrated High-Performance Active Rectifier for Piezoelectric Vibration Energy Harvesting Systems

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***Abstract*—In this letter, a highly efficient active full-bridge rectifier is proposed for piezoelectric (PE) vibration energy harvesting systems. By replacing the passive diodes with an operational amplifier-controlled active counterpart and adding a switch in parallel with the transducer, the proposed rectifier solves the dc-offset problem of the comparator-based active diode, minimizes the voltage drop along the conduction path, and extracts more power from the transducer, all of which lead to better power extraction and conversion capability. The proposed rectifier, implemented in 0.18-μm CMOS technology, shows 90% power conversion efficiency and 81 μW output power, with values corresponding to 1.5 times and 3.4 times the values for a conventional full-bridge rectifier.**

***Index Terms*—Active rectifier, CMOS, full-bridge rectifier, operational amplifier, piezoelectric (PE), transducer, vibration energy harvesting.**

I. Introduction

HARVESTING energy from the environment (solar, thermal, kinetic, etc.) is a promising alternative to batteries and and it has been receiving much more attention lately due to the increasing demand for wireless sensor networks, implantable medical electronics, tire-pressure sensor networks, etc. [1], [2]. Piezoelectric (PE) vibration energy harvesting is appealing because of its moderate power density versus internal light and electromagnetic/electrostatic vibration. The output of the PE transducer is an ac quantity that requires conversion into dc by a rectifier [3]–[5]. The power converters reported for vibration energy mostly consist of a rectifier followed by a buck or boost dc–dc converter. The overall efficiency of a PE energy harvesting system depends on the power extraction and conversion efficiency of the rectifier, as well as on the conversion efficiency of the dc–dc converter.

To improve the power extraction ability of the conventional full-bridge rectifier (CFB), a switch-only (SO) rectifier is proposed in which a switch is connected in parallel with the transducer [2]. The SO rectifier can improve the extracted power by two times compared to that of the conventional rectifier by turning ON a switch to instantly discharge the capacitor when the transducer current crosses zero. However, the forward voltage drops across the rectifying diodes are a significant source of conduction power loss in [2]. One way of reducing voltage drop is to superimpose a bias voltage onto the gate of the MOSFET that effectively cancels the drop associated with threshold voltage $V_{\rm TH}$ [6]. However, an additional bias voltage generator circuit is needed, which adds complexity to the rectifier design. Many active synchronous rectifiers using comparator-controlled rectifying switches are currently considered the most promising solutions for overcoming the forward voltage drop issue [7]–[9]. However, the comparator-based active rectifier has leakage and oscillation problems caused by the dc offset of the comparator, which could significantly degrade the conversion efficiency. In [10], an operational amplifier-based half-wave rectifier is proposed to solve the leakage and oscillation problems that exist in comparator-based rectifier; however, the output power is low due to the poor extraction ability.

In this letter, an active full-bridge rectifier which adopts a switch in parallel with the transducer and an operational amplifier-based active diode is proposed. The proposed rectifier shows both good power extraction and conversion ability which is not achieved by all previous reported rectifiers.

II. Proposed Rectifier Design

A. Proposed Rectifier

Fig. 1 shows the schematic of the proposed rectifier, the voltage/current waveforms, and the simplified equivalent circuit schematics. In Fig. 1(a), the PE transducer, when excited by sinusoidal vibrations, is modeled as a sinusoidal current source $i_P(t) = I_P \sin(2\pi f_P t)$ in parallel with a capacitor C_P and an internal resistor R_P, where I_P is the current amplitude and f_P the excitation frequency [2]. A switch SW is connected in parallel with the PE transducer. Of the four MOSFET-based rectifying diodes, the PMOS transistors are configured in a cross-coupled structure while the NMOS transistors are implemented in combination with op-amps (with offset voltage $V_{\rm OS}$ of given polarity). C_L is used to store the harvested energy and R_L is the load resistor.

As shown in Fig. 1(b), during the steady-state operation of the rectier, the positive half cycle of the input signal injection period can be divided into three different operational states. During state 1, initially, I_P is used to charge C_P only, and if

Manuscript received March 3, 2011; revised May 17, 2011; accepted June 26, 2011. Date of current version January 9, 2012. Recommended for publication by Associate Editor C. K. Tse.

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Digital Object Identifier 10.1109/TPEL.2011.2162078

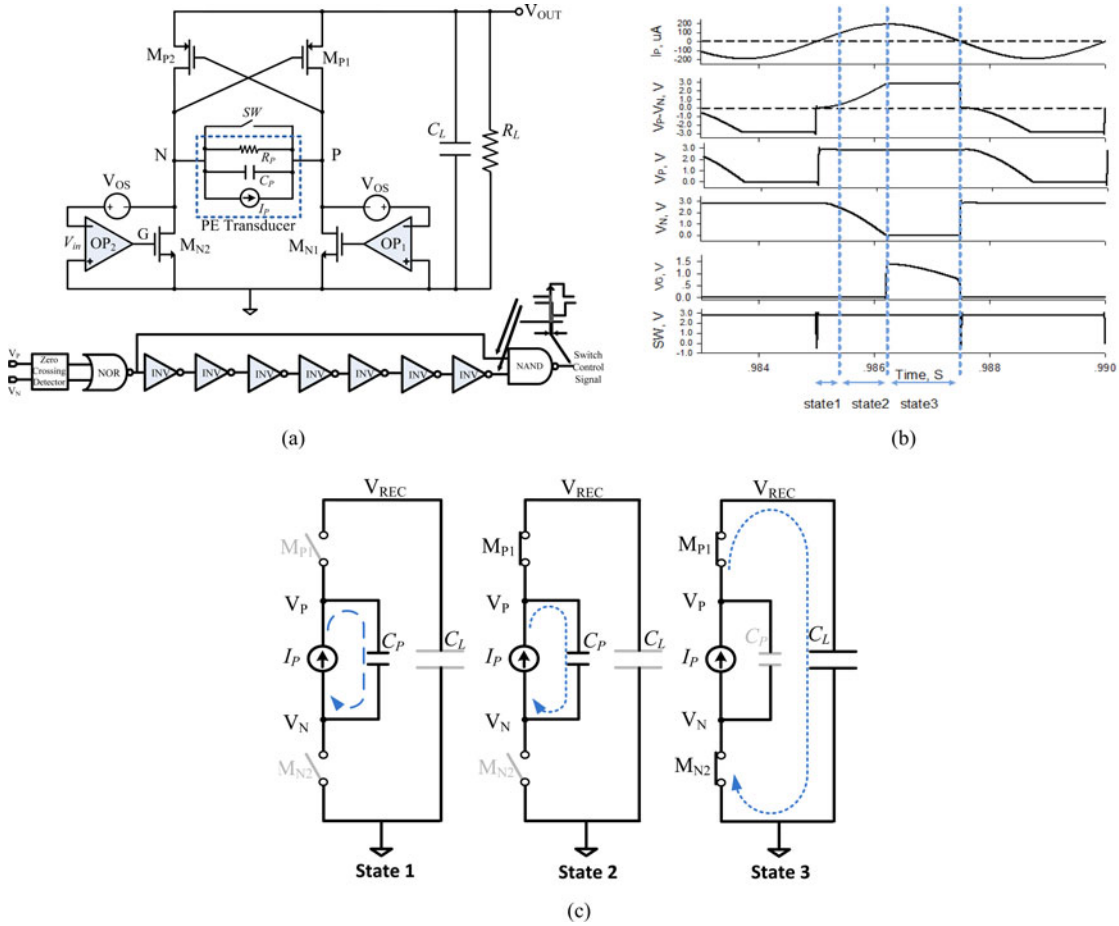

Fig. 1. (a) Simplified circuit schematic of the proposed rectifier. (b) Simulated voltage and current waveforms of the proposed rectifier. (c) Equivalent circuit of operating states 1, 2, and 3.

$0 < V_{\rm PN} < |V_{\rm THP}|$, where $|V_{\rm THP}|$ is the threshold voltage of M_{P1}, M_{P1} is OFF. Since $V_N > 0$, M_{N2} is also OFF and no current flows through M_{P1} and M_{N2}, the equivalent circuit looks like as shown in Fig. 1(c). As I_P increases further such that when $V_{\rm PN} \geq |V_{\rm THP}|$, M_{P1} turns ON and the rectifier enters into state 2. In state 2, since M_{P1} functions as a closed switch with a very small voltage drop, node P is shorted to the rectifier output ($V_{\rm OUT}$), and since V_N is still larger than 0 V, M_{N2} remains OFF and there is no current flowing into the output. However, as I_P keeps flowing into C_P, $V_{\rm PN}$ continues to increase. As can be seen from the equivalent circuit shown in Fig. 1(c), since node P is shorted to the output node, the increase in $V_{\rm PN}$ leads to the decrease in V_N. When $V_N \leq V_{\rm OS}$, the output of the op-amp is switched to high and turns ON transistor M_{N2}, and thus the rectifier enters into state 3. In state 3, since both M_{P1} and M_{N2} are ON, a current path to the output is formed [see the equivalent circuits shown in Fig. 1(c)], and I_P starts flowing into the load capacitor C_L. Since the load capacitor C_L has a much larger value than that of C_P, I_P will mainly flow into C_L with $V_{\rm OUT}$ given by $V_{\rm PN} - |V_{\rm DSP}| - V_{\rm DSN}$, where $V_{\rm DSP}$ and $V_{\rm DSN}$ are the drain-source voltages of M_{P1} and M_{N2}, respectively. Both M_{P1} and M_{N2} operate in the linear region; therefore, increasing the size of M_{P1} and M_{N2} leads to smaller ON resistances of the switch and drain-source voltage drop, thereby maximizing the voltage conversion efficiency. The amplitude of the charging current decreases in time [see Fig. 1(b)], and when I_P reduces to 0, the switch SW in Fig. 1(a) turns ON for a brief period and discharges C_P instantly by shorting nodes P and N so that $V_{\rm PN} = 0$. At this time, both M_{P1} and M_{N2} turn OFF as well. Once C_P has been discharged, the switch SW turns OFF and the positive half cycle ends. In the proposed rectifier, the switch control circuit, as shown in Fig. 1(a), is realized by a zero-crossing detection circuit followed by a pulse generator, which is adopted from [2]. The switch control signal is based on the delay of an inverter chain; hence, it is subjected to process variation which could lead to the pulsewidth variation of the control signal, and therefore the variation in power efficiency. However, as long as the control signal is large enough to discharge C_P completely, this variation would have negligible effect on power efficiency. The effect of process variations on the switch control signal and resulting power efficiency has been estimated with Monte Carlo simulations, and proved to be negligible with less than 1% variations in power efficiency. The rectier will operate similarly in the negative half cycle, except that now only M_{P2} and M_{N1} are involved. The adoption of the switch SW helps to save the waste of I_P to discharge C_P before the start of the next half cycle so that more energy can be transferred to the output.

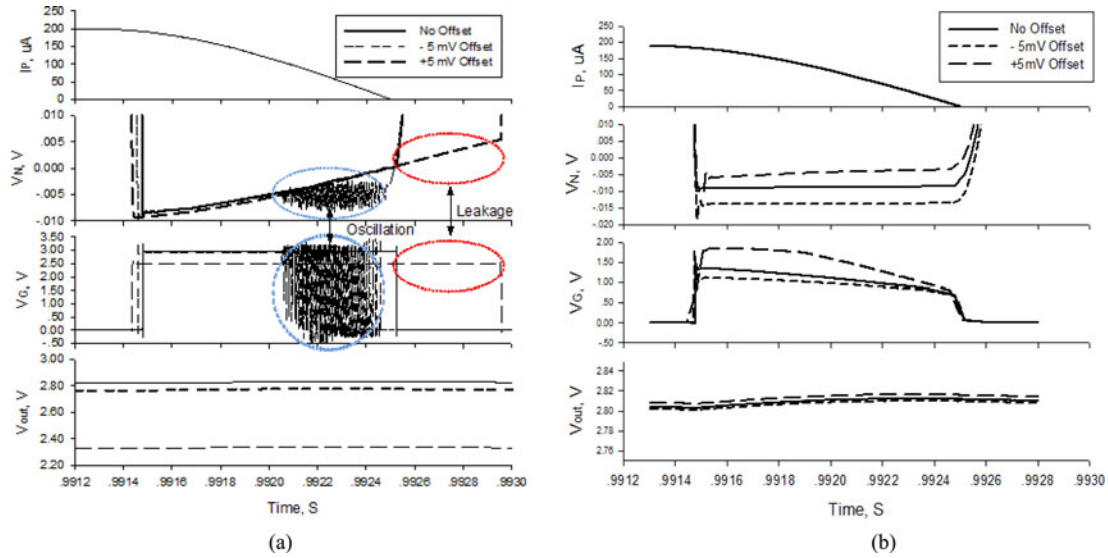

Fig. 2. Simulated waveforms of rectifier for three values of offsets. (a) Omparator-based rectifier. (b) Proposed rectifier.

B. Active Diode Operation

Fig. 2 shows the steady-state time-domain behavior of the transducer current I_P during state 3, the voltages at node $N(V_N)$, $G(V_G)$, and the output ($V_{\rm OUT}$) for the circuits shown in Fig. 1(a) for two different implementations of active diodes: 1) active diode with comparator [6] and; 2) active diode with op-amp as shown in Fig. 1(a). The simulation is done for three different values of input referred offset voltages (w.r.t. ground) in the comparator and op-amp, which could be caused by the process variations and mismatches: 0, $+5$, and -5 mV, respectively. As can be seen in Fig. 2(a), for the comparator-based case, when the offset voltage is negative, V_N and V_G show oscillation as IP approaches zero. The reason for the oscillation is that, with the -5 mV offset, the threshold voltage of the comparator becomes negative. From Fig. 2(a), it can be seen that when I_P is gradually reduced, V_N increases from its negative value. When V_N becomes higher than the offset voltage (-5 mV), V_G is switched to low and M_{N2} turns OFF. Then, the rectifier operates in state 2, as shown in Fig. 1(c); therefore, I_P is used for charging C_P only, which leads to a decrease in V_N again. When V_N goes below the offset voltage (-5 mV), V_G is switched to high again and M_{N2} turns ON again. This ON and OFF operation of M_{N2} will be repeated, with the oscillation of V_N and V_G as shown in Fig. 2(a), until I_P goes to 0. This oscillation in V_N and V_G leads to power loss (reduction in $V_{\rm OUT}$), as shown in Fig. 2(a). Now, with the $+5$ mV offset, the threshold voltage of the comparator becomes positive, and when I_P reduces to 0, V_N approaches 0 as well. Since V_N is less than the offset voltage ($+5$ mV), the output of the comparator remains high. Therefore, since M_{N2} is ON, the state 3 current path shown in Fig. 1(c) still exists, which leads to output current leakage into C_P. As can be seen in Fig. 2(a), in the comparator-based rectifier, this leakage problem leads to a significant power loss, which is indicated by the reduction in $V_{\rm OUT}$.

As shown in Fig. 1, by adopting the op-amp (with voltage offset) based active diode, the aforementioned reverse leakage and oscillation problem can be resolved. Fig. 3 shows the schematic and the simulated ac response of the op-amp for the proposed rectifier. Since the op-amp works with near ground input and the supply voltage of op-amp comes from the harvested energy, common-gate topology is adopted with an optimized design for low-power dissipation [10]. As shown in Fig. 3, the transistors in the op-amp are biased to operate in the subthreshold region such that the op-amp dissipated a total current of 90 nA while providing the dc gain of 60 dB, and unit gain bandwidth of more than 250 kHz.

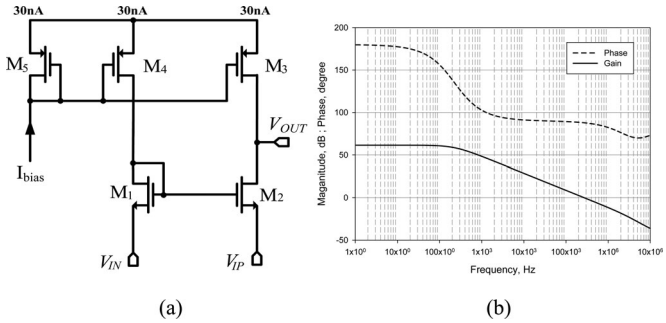

Fig. 3. (a) Ground input compatible operation amplifier. (b) Simulated frequency response of the operational amplifier.

From Fig. 1, when the rectifier operates in the region of state 3, a regulation loop is formed within the op-amp and M_{N2} circuit such that

$$V_{\rm in} + V_{\rm OS} + V_{\rm DS} = 0 \tag{1}$$

where $V_{\rm in}$ is the input voltage of the op-amp and $V_{\rm DS}$ the drain-source voltage of M_{N2}. The offset voltage $V_{\rm OS}$ with the given polarity can be obtained by the mismatch in the aspect ratio of the op-amp's input transistors. In the proposed rectifier, $V_{\rm OS}$ is designed to be 20 mV. The value of $V_{\rm OS}$ is not critical as long as it is large enough so that the process variations and mismatches do not change its sign. Monte Carlo simulations have been performed to estimate the possible spread of $V_{\rm OS}$.

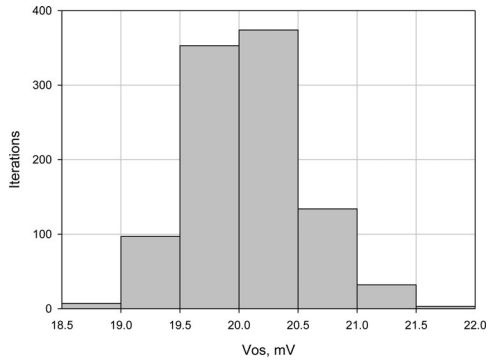

Fig. 4. Monte Carlo simulation of $V_{\rm OS}$ of the designed operational amplifier.

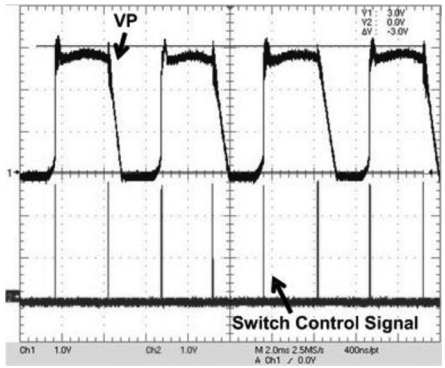

Fig. 5. Measured voltage waveforms of V_P and a switch control signal for the proposed rectifier.

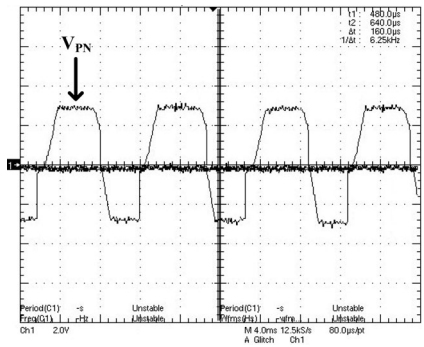

Fig. 6. Measured waveform of the output voltage across the PE transducer for the proposed rectifier.

Fig. 4 shows the simulation result of 1000 Monte Carlo iterations on $V_{\rm OS}$ with process and mismatch variations. As can be seen in Fig. 4, the Monte Carlo simulation shows the mean $V_{\rm OS}$ value of 19.8 mV with the standard deviation (σ) of 0.49 mV (68%). Even with 3σ variation (99.7%), the spread of $V_{\rm OS}$ is sufficiently small, so $V_{\rm OS}$ does not change its sign. Moreover, the mismatches in $V_{\rm OS}$ between the two op-amps can occur due to the process variations. This effect has also been estimated by the Monte Carlo simulation and there was less than 1% degradation in power efficiency for the 25% mismatches in the two offset voltages for two op-amps.

For the op-amp's dc gain of A, the voltage at the gate of M_{N2} (node G) is given by

$$V_G = AV_{\rm in} = -A(V_{\rm OS} + V_{\rm DS}). \tag{2}$$

From (2), for large op-amp gain, $V_{\rm in} \approx 0$ and $V_{\rm DS} \approx -V_{\rm OS}$. Therefore, when the rectifier operates in state 3, with given polarity of the op-amp's offset voltage $V_{\rm OS}$, the drain voltage of M_{N2} remains below $-V_{\rm OS}$, which guarantees that no oscillations of the driving signal will take place. The regulation loop in the active diode senses the voltage across the drain-source terminal of M_{N2} and modulates the gate voltage V_G for the given value of the drain current I_P. At the point where I_P goes to 0, M_{N2} turns OFF and the regulation loop opens; therefore, the unwanted discharge from C_L is prevented. In order to test the immunity of the proposed rectifier to the offset caused by process variation and mismatch, $\pm$5 mV of offsets [in addition to the $V_{\rm OS}$ shown in Fig. 1(a)] are applied to the op-amp, as can be seen in Fig. 1(a). As can be seen from Fig. 2(b), the proposed rectifier shows no oscillation or output leakage for the additional offsets of 0 and $\pm$5 mV; therefore, $V_{\rm OUT}$ remains nearly constant.

III. Measurement Results

The proposed rectifier shown in Fig. 1 is implemented in 0.18-μm CMOS technology. For comparison, the CFB and SO rectifiers are also implemented. For the measurement of the three rectifiers, instead of an actual PE transducer, an equivalent transducer is used, which consists of an ac voltage source in series with a capacitor C_P. R_P is not used because of its large value. For the ac voltage source, a 200-Hz sine wave with 3 V peak-to-peak is used. Under the condition of $C_P = 25$ nF and $C_L = 1$ μF, the rectified output voltage is measured across a load resistor R_L. Since the energy transfer from the PE transducer to the load depends on the value of the load resistance, R_L is varied from 10 to 150 kΩ, seeking the optimum value. Fig. 5 shows oscilloscope waveforms of the proposed rectifier, which include V_P and switch control signal. The waveforms obtained are consistent with the operation of the proposed rectier as described in Sections II. Fig. 6 shows the oscilloscope waveform of the output voltage of the PE transducer. From Fig. 6, the proposed rectier brings the voltage to ground almost instantly, thereby helping to save the waste of I_P to discharge C_P so that more energy can be transferred to the output. Fig. 7 shows the measured rectified output voltage $V_{\rm OUT}$ of different rectifiers. From Fig. 7, the final output voltages of CFB, SO, and proposed rectifiers are 1.1, 2, and 2.78 V under 50, 75, and 95 kΩ of optimized load conditions, respectively, and the corresponding output power are 24, 53, and 81 μW, respectively. According to the equations in [2], the theoretical maximum output power of CFB, SO, and the proposed rectifier are 45, 90, and 90 μW, respectively, which means that the peak power conversion efficiency are 57%, 58%, and 90%, respectively. Therefore, the output power of the proposed rectifier are 3.4 and 1.5 times those of the CFB and SO rectifiers, and the conversion efficiency is 1.5 times that of both the CFB and SO rectifiers. Fig. 8 shows a chip microphotograph of all three rectifiers with a size of 0.4 mm $\times$ 0.6 mm. Table I compares the performance of the proposed rectifier with those

TABLE I
PERFORMANCE SUMMARY AND COMPARISONS

Parameters	*CFB*	*[2]*	*[6]*	*[10]*	*This Work*	*Units*
Input Amplitude [V_{PN}]	*2*	*2.8*	*2*		*2.8*	V
V_{OUT}	*1.1*	*2*	*1.9*	-	*2.78*	V
Frequency	*200*	*200*	*200k-1.5M*	*200*	*200*	Hz
Voltage Drop	$2V_{TH}$	$2V_{TH}$	$2V_{DS}$	V_{DS}	$2V_{DS}$	mV
V_{OUT}/ V_{PN}	*55%*	*75%*	*95%*	/	*99%*	-
P_{OUT}	*24*	*53*			*81*	μW
Peak Power Efficiency	*57%* R_L=*50k*Ω	*58%* R_L=*75k*Ω	*82-87%* R_L=*100*Ω	*90%* R_L=*400k*Ω	*90%* R_L=*95k*Ω	

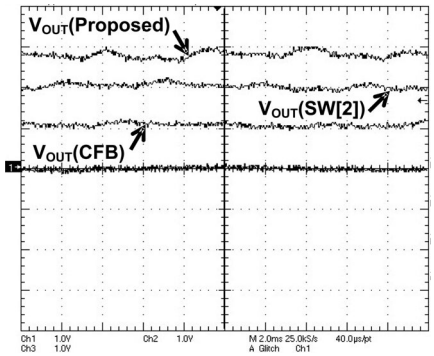

Fig. 7. Measured rectified output voltage V_{OUT} of different rectifiers.

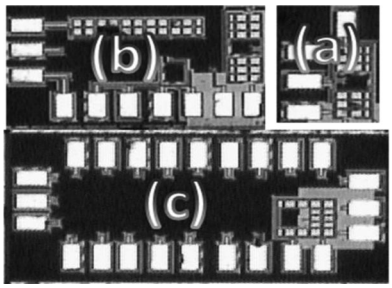

Fig. 8. Chip microphotograph. (a) Conventional full-bridge rectifier. (b) Passive switch only rectifier. (c) Proposed rectifier.

of other reported rectifiers. As can be seen from Table I, the proposed rectifier shows the best efficiency and output power.

IV. CONCLUSION

An integrated power efficient active full-bridge rectifier is proposed for PE vibration energy harvesting systems. By replacing the passive diodes with an operational amplifier-based active counterpart, the proposed rectifier minimizes the voltage drop along the conduction path and solves the dc-offset problem of the comparator-based active diode which could deliver the maximum forward current to the load, while minimizing the leakage current. By adding a switch in parallel with a transducer, the proposed rectifier extracts more power from the transducer. All of which lead to more power extraction and far better power conversion efficiency compared to the previously reported rectiers. Implemented in 0.18-μm CMOS technology, measurement results show that the proposed rectifier improves the output power by 3.4 and 1.5 times over output power of conventional full-bridge and passive SO rectifiers, and improves the efficiency by 1.5 times compared to that of both conventional full-bridge and passive SO rectifiers.

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