A Long Reset-Time Power-On Reset Circuit With Brown-Out Detection Capability

Huy-Binh Le, Xuan-Dien Do, Sang-Gug Lee, and Seung-Tak Ryu

***Abstract*—A compact low-power on-chip power-on reset circuit with a brown-out detection capability is presented. With a pico-farad-order on-chip MOS capacitor, a long reset time is achieved. A prototype design implemented in a 0.18-μm CMOS process provides a reset signal with duration of hundreds of milliseconds. The embedded brown-out detection circuit can detect the event, as long as the brown-out duration is longer than the millisecond range. The chip consumes only 1 μA under a 1.8-V supply and occupies a 120 μm $\times$ 100 μm active area.**

***Index Terms*—Brown-out detection, brown-out reset (BOR), power-on detection, power-on reset (POR).**

I. Introduction

When powering up electronic systems, a certain amount of time is necessary for the power supply to settle to its steady-state value. During this transitional period, unless a reset command is provided, the initial status of memory elements such as digital registers and analog integrators cannot be defined and thus the entire circuit behavior cannot be determined also. Thus, these circuits require a certain command signal for circuit initialization during or after the power-up period, which is referred to as power-on reset (POR). The POR signal should hold circuits in the reset state until the power supply reaches a steady-state level where all the circuits can correctly operate.

Sudden disturbances during normal operation are also the troublesome transient behaviors of the supply voltage. Due to excessive supply noise or heavy current drawn by the load, the supply voltage can abruptly drop and the circuits under the supply can malfunction. This phenomenon is known as a brown-out event. In many applications, it is necessary to generate a reset signal whenever the supply voltage drops below a certain level for a certain time; this signal is referred to as a brown-out reset (BOR) signal. To generate this signal, both the magnitude and duration of the disturbance must be examined. The BOR signal must return to zero when the supply recovers from the disturbance and other circuits recover their states.

Fig. 1 shows representative timing diagrams of supply voltage V_{DD} and the desirable reset signal. The definitions of the terms in the figure are as follows. $V_{\rm final}$ is the steady-state value of the supply voltage. $V_{\rm low}$ is the lowest supply level at which the circuits can correctly operate; if the supply voltage falls below this level, a BOR signal should be generated and reset the circuits. $V_{\rm min}$ is the minimum voltage of the supply at which the reset switch is turned on by the reset signal (i.e., the threshold of the reset switch). T_0 is the rising time of the supply voltage from the power-on command. T_1 is the rising/falling time of a brown-out event, and $T_{\rm int}$ is its duration. $T_{\rm POR}$ $(T_{\rm BOR})$ is the reset time counted from the moment when the reset switch turns on (i.e., when POR/BOR signal is larger than $V_{\rm min}$), and $T_{\rm POReff}$ $(T_{\rm BOReff})$ is the effective reset time counted from the moment the supply voltage reaches $V_{\rm final}$ during a power-on event (brown-out event). For a short glitch on the supply, there is not much difference between $T_{\rm BOR}$ and $T_{\rm BOReff}$.

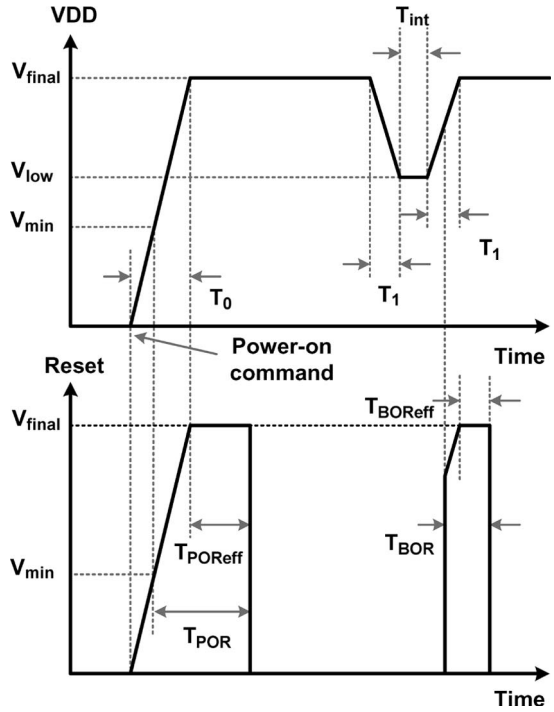

Fig. 1. Timing of POR and BOR.

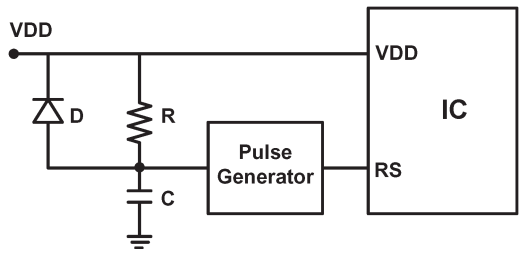

Fig. 2. External POR circuit.

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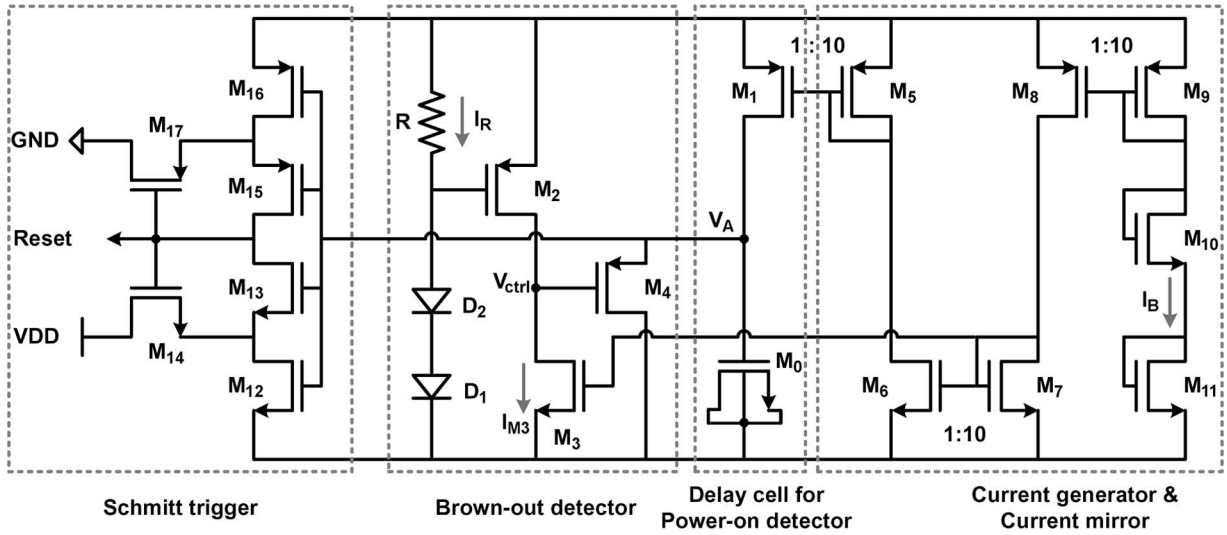

Fig. 3. Proposed POR circuit with BOR detection function.

A POR circuit can be built upon a delay element and a pulse generator, as shown in Fig. 2 [1]. The delay element could be implemented utilizing a large external resistor and capacitor in series so that the capacitor tracks the supply with a low-pass characteristic and provides sufficient reset time. Diode D is for rapid discharge of the capacitor upon power down. Regarding on-chip implementation of POR and BOR functions, several design issues arise, including the problem of large RC components. The RC time constant of the delay element must be comparable to the rising time of the supply voltage (see T_0 in Fig. 1), which can be up to tens or hundreds of milliseconds in many applications [1]–[3]. Furthermore, modern large-size integrated circuits (ICs) with numerous functional blocks require long-enough reset time to initialize all the subcircuits that are spread over the chip. For example, in an IC with a built-in oscillator, the initial settling time may vary from the millisecond to second ranges depending on the oscillating frequency [2]. These two conditions require large RC components for a sufficient time constant for POR signal generation. The second condition also asks for a long reset time when a brown-out event is detected. The large on-chip capacitor issue could be solved by adopting capacitor scale-up techniques in other applications [4], [5]. However, it is not easy to adopt such circuit techniques because they must properly work before the supply reaches the steady state (i.e., during the power-up time). Nevertheless, not many on-chip CMOS POR circuits have been reported thus far. They, instead, have focused on low power consumption and showed considerably short reset time due to the limited RC time constant. The POR circuit for low-voltage applications presented in [6] showed a submicrosecond reset time. A zero steady-state current consuming POR design was reported with a BOR detection capability [7]; however, the reported reset time during power-on and brown-out events was only in the microsecond range. Although the delay element for POR circuits could be designed to be very compact with low power consumption [8], the reset time was strongly dependent on the rising time of the power supply, which was limited to less than 1 ms.

In this brief, a compact on-chip POR circuit with a brown-out (BOR) detection capability is designed and is shown to present sufficient reset time. This brief is organized as follows. Section II explains the proposed circuit and its behavior, and Section III discusses the measured performance. Section IV concludes this brief.

II. Proposed POR Circuit

Fig. 3 shows the proposed POR circuit with an embedded BOR detection function. The circuit consists of four functional subcircuits, namely, a current generator and cascaded mirrors, a delay cell for the power-on detector, a brown-out detector, and a Schmitt trigger. Three diode-connected transistors, i.e., $M_9 - M_{11}$, form a current generator, and the cascaded current mirrors, i.e., $M_9 - M_8$, $M_7 - M_6$, and $M_5 - M_1$, scale down the current generated by M_9 so that nominal current through M_1 is in a subnanoampere value, as long as it is in the saturation region. The pMOS current source M_1 and an nMOS capacitor M_0 comprise the delay cell for the power-on detector. The brown-out detector consists of a branch composed of R, D_1 and D_2, current sources M_2 and M_3, and current sinking transistor M_4. The common outputs V_A of both the delay cell for the power-on detector and the brown-out detector are connected to a Schmitt trigger so that a clean reset pulse can be generated.

The operational principle of the proposed circuit is as follows: When power is switched on, supply voltage gradually rises and the current generator $(M_9 - M_{11})$ remains off until the supply voltage reaches the turn-on voltage of the current generator, i.e., $V_{I\_\mathrm{ON}} = V_{\mathrm{gs9}} + V_{\mathrm{gs10}} + V_{\mathrm{gs11}}$. Thus, V_A, the drain voltage of current source M_1, remains low. During this transition period, the output of the Schmitt trigger $Reset$ continues to rise by tracking the supply voltage and turns on the reset switches connected to it (the corresponding reset switch is not shown in the schematic) when it reaches $V_{\min}$ in Fig. 1. When the supply voltage exceeds V_{I_ON}, the current generator and cascaded mirrors turn on and M_1 starts to charge M_0 with a subnanoampere-order current, and thus, V_A starts to rise. When V_A exceeds the high switching point of the Schmitt trigger V_{SPH}, the $Reset$ signal switches back to low and finishes the reset phase. The whole circuit connected to this reset signal then starts to operate at normal operation. The duration of the reset signal can be set by current through M_1, the size (capacitance) of M_0, and the value of V_{SPH}. Of course, as V_{SPH} is higher, a

longer reset time is achieved. When M_0 charging is completed, M_1 is in a weak inversion region and operates as a very large resistor.

Aside from the powering-up period, the supply voltage can be disturbed during normal operation by certain circumstances such as instant heavy current drawing from the load or a sudden power failure. If such brown-out events occur and the power supply falls below a certain level $V_{\rm low}$, where the IC fails to correctly operate, a reset pulse should be generated in order to prevent circuit malfunction. However, the power-on detector may not be able to react to such a fast glitch because V_A does not rapidly drop due to the small drain current of M_1. Considering this case, a designated brown-out detection circuit is added. During normal operation under steady-state V_{DD}, M_2 is on due to the IR drop through resistor R and it pulls the $V_{\rm ctrl}$ node high. This, in turn, disables M_4 since V_A is at V_{DD} during normal operation. When the power supply falls below $V_{\rm low} = V_{D1} + V_{D2} + V_{\rm gs2}$ (i.e., when a brown-out event occurs), M_2 turns off and current source M_3 pulls $V_{\rm ctrl}$ down to the ground (GND) level. This turns on M_4, and in turn, the V_A node is rapidly discharged. When V_A drops below the low switching point of the Schmitt trigger $V_{\rm SPL}$, the Schmitt trigger turns on and generates a reset pulse. As is well known, the values of $V_{\rm SPH}$ and $V_{\rm SPL}$ can be set by changing the sizes of the transistors, i.e., $M_{12} - M_{17}$ [9]. In the present design, $V_{\rm SPH}$ and $V_{\rm SPL}$ have been chosen to be about 1.45 and 0.8 V, respectively, i.e., when V_A crosses 1.45 V while it increases, the reset signal turns off, and when V_A reduces and reaches 0.8 V, the reset signal turns on.

In this design, the total static current is dominated by the currents flowing through D_1 and $D_2(I_R)$, $M_3(I_{M3})$, and $M_9(I_B)$. In order to lower the power consumption, these currents need to be minimized

$$I_R = \frac{V_{DD} - V_{D1} - V_{D2}}{R}. \tag{1}$$

Although larger R reduces I_R, as (1) depicts, considering the cost due to chip size, its value has been chosen as 2 MΩ.

Current through M_3, I_{M3}, determines how fast control voltage $V_{\rm ctrl}$ can be dropped when a brown-out event is detected. Equation (2) depicts how I_{M3} is determined

$$I_{M3} = \frac{\Delta V \cdot C_P}{\Delta t}. \tag{2}$$

Here, ΔV is the required dropout voltage of $V_{\rm ctrl}$ from V_{DD} to turn M_4 on ($\Delta V > |V_{\rm th\_M4}|$), C_P is the parasitic capacitance at the gate of M_4, and Δt is the minimum time that the supply voltage stays below $V_{\rm low}$ from the moment the brown-out event is detected (i.e., during the time M_2 is off). With 50 fF of C_P and 0.5 V of $V_{\rm th}$ in the present design, bias current I_{M3} needs to be larger than 25 nA in order for $V_{\rm ctrl}$ to drop with the amount of ΔV within $\Delta t = 1$ μs. The designed nominal values for I_R, I_{M3}, and I_B are 0.3, 0.05, and 0.5 μA, respectively, at a 1.8-V supply. With ±10% variation of the supply voltage, the total dc current varies by about ±30%, which corresponds to $0.7-1.3$ μA. Process corner simulations (SS/FF/TT) with temperature from -20 °C to 100 °C showed total static current variation of up to 40% as a worst case. The current consumption can be further reduced with the cost of increased chip size or with slight modification in the $M_9 - M_{11}$ branch. Meanwhile, the turn-on voltage for brownout $V_{\rm low}$ can be determined by the number and sizes of diodes and the size ratio of M_2 once current through M_3 has been fixed. In this design, $V_{\rm low}$ has been set at 1.5 V. For the worst case in various corner conditions with 10% of V_{DD} variation, 20% of R variation, and temperature range from -20 °C to 100 °C, the value of $V_{\rm low}$ is within ±100 mV from the designed value. In addition, for the same PVT conditions, the simulation results for POR/BOR reset time show up to 30% of variation.

Now let us consider the minimum duration of the supply drop that the brown-out circuit can respond to (minimum of $T_{\rm int}$). First, assume that the power supply drops to $V_{\rm low}$ and stays for an interval of $T_{\rm int}$. For simplicity, it is assumed that $V_{\rm ctrl}$ quickly drops to GND as soon as V_{DD} reaches $V_{\rm low}$. The current that flows through M_4 during this event is

$$i_{D4} = -\frac{1}{2}\mu_p C_{\rm ox}\left(\frac{W}{L}\right)_4 (V_{GS4} - V_{\rm th})^2 = -\frac{1}{2}\beta_4 (V_A - V_{\rm th})^2 \tag{3}$$

where $V_{\rm th}$ is the threshold voltage of pMOS transistor M_4. Capacitor M_0 is then discharged by i_{D4}

$$i_{D4} = C\frac{dV_A}{dt} \tag{4}$$

where C is the equivalent capacitance of M_0, and current through M_1 is ignored because current through M_4 has been designed to draw much more current than M_1 while M_4 is on. The capacitance variation of M_0 is simply neglected since it is always on during the brown-out event owing to M_4's V_{GS}. From (3) and (4), the minimum time of $T_{\rm int}$, i.e., $T_{\rm int\_min}$, for M_0 to discharge its voltage V_A from $V_{\rm final}$ to $V_{\rm SPL}$ and to change the output of the Schmitt trigger can be calculated as

$$\begin{aligned} T_{\rm int\_min} &= \int_0^{t_{\rm min}} dt = \int_{V_{\rm final}}^{V_{\rm SPL}} \frac{C}{i_{D4}} dV_A \\ &= \frac{2C}{\beta_4}\left(\frac{1}{V_{\rm SPL} - V_{\rm th}} - \frac{1}{V_{\rm final} - V_{\rm th}}\right). \end{aligned} \tag{5}$$

Hence, the interval of a brown-out event $T_{\rm int}$ should be larger than $T_{\rm int\_min}$ so that the brown-out circuit can detect the situation and generate a reset signal. The value of $T_{\rm int\_min}$ can be designed with the size of M_4, equivalent capacitance of M_0, and the high-to-low switching point of the Schmitt trigger $V_{\rm SPL}$.

Fig. 4 shows the simulated transient responses of the circuit shown in Fig. 3 with a power-on event and a brown-out event. In the test bench, power supply voltage V_{DD} rises from 0 to 1.8 V with a rising time of $T_0 = 100$ ms. The initial voltages of V_A and $V_{\rm ctrl}$ are assumed to be fully discharged at GND. As shown, $V_{\rm ctrl}$ and V_A remain low until the supply voltage reaches $V_{I\_ON} = 1.5$ V. Thus, M_{15} and M_{16} are on and the $Reset$ signal follows V_{DD}. V_A starts to slowly increase once the supply voltage exceeds 1.5 V. When V_A reaches $V_{\rm SPH} = 1.45$ V, the Schmitt trigger switches to low and drops the reset signal.

The brown-out event contains a 0.3-V voltage drop from the steady-state V_{DD}, i.e., $V_{\rm low} = 1.5$ V, with a 10-μs duration value and a 10-μs rising/falling time. During the brown-out event, when the supply voltage drops to 1.5 V, $V_{\rm ctrl}$ falls and it activates M_4, and V_A is then rapidly discharged by the current of M_4. As soon as V_A crosses $V_{\rm SPL}$ (0.8 V), the Schmitt trigger switches to high to provide a reset signal. The reset pulse stays

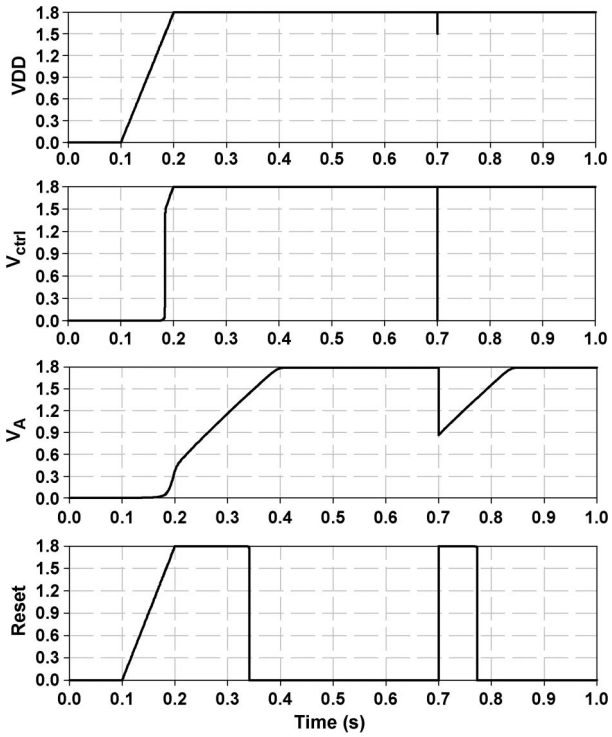

Fig. 4. Simulated transient responses during power-on and brown-out events.

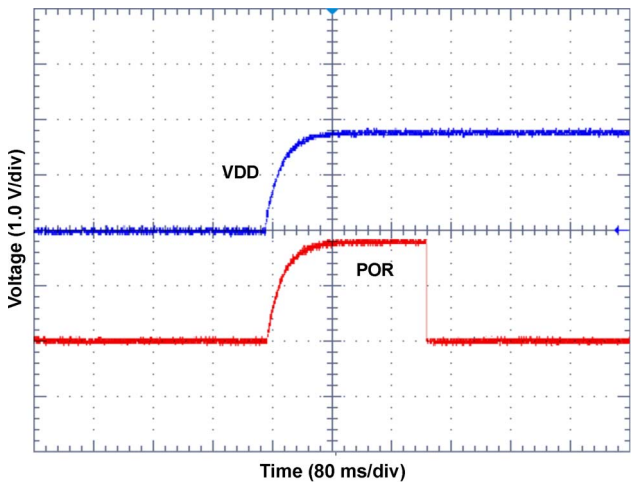

Fig. 5. Measured POR reset pulse for a power-on event with a 80-ms rising time.

until the supply voltage recovers from $V_{\rm low}$. The minimum duration of a brownout that the BOR circuit can detect through this simulation is about 1 μs. This value agrees well with the value calculated in (5), i.e., $T_{\rm int\_min} = 0.93$ μs.

III. Measurement Results

A prototype chip has been implemented in a 0.18-μm CMOS process for a 1.8-V supply. Fig. 5 shows the captured reset waveform for a power-on event with an 80-ms rising time. The reset signal (POR) tracks V_{DD} and stays high for a short duration period before returning to zero. This shows successful reset signal generation during powering up. Fig. 6 shows the measured reset time $T_{\rm POR}$ and the effective reset time $T_{\rm POReff}$ with respect to the rising time of the power-on event T_0. Here, the minimum voltage of the reset signal to turn on the reset

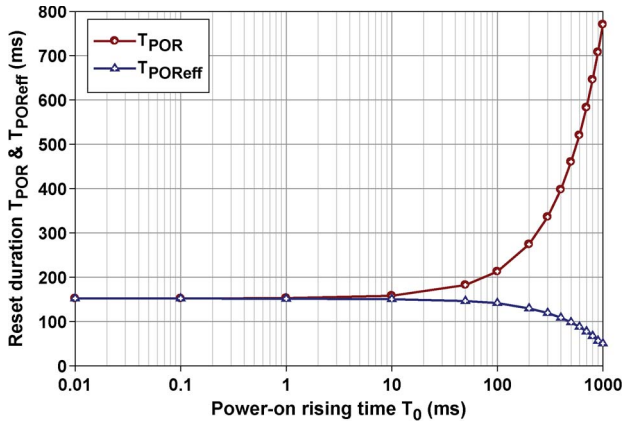

Fig. 6. Measured reset time with respect to the rising time of a power-on event.

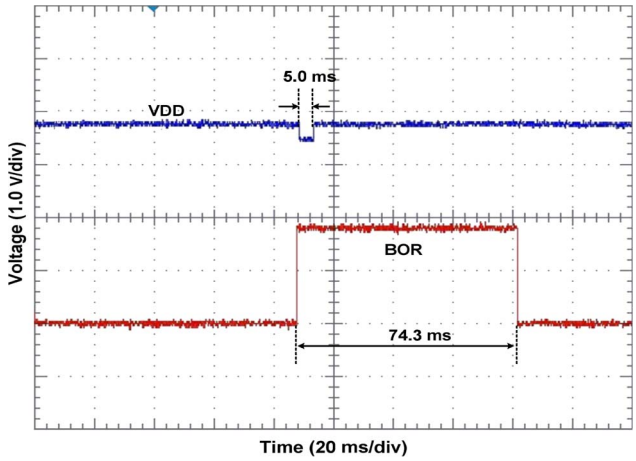

Fig. 7. Measured output reset waveform with a 0.3-V drop of supply voltage ($V_{\rm low} = 1.5$ V) in $T_{\rm int} = 5$ ms.

switches is assumed to be the threshold voltage of a MOS transistor, i.e., $V_{\rm min} = V_{\rm th} = 0.5$ V. With slower power-on rising time T_1, longer reset time $T_{\rm POR}$ and shorter effective reset time $T_{\rm POReff}$ are obtained. Nevertheless, the minimum POR reset time is 150 ms. Note that POR works for a very long rising time, i.e., more than 1 s.

Tests for brown-out events were also performed. Fig. 7 shows the measured output waveform of the BOR signal for a disturbance with 0.3-V dropout voltage and 5-ms duration with 100-μs rising/falling time T_1. The measured BOR reset time in this case is 74.3 ms. Fig. 8 shows the measured brown-out detection level $V_{\rm low}$ versus the duration of a brown-out event for several slopes of the supply disturbance. This graph shows that the designed circuit generates a reset signal (BOR) when the monitored power supply drops below 1.5 V, as long as the brown-out duration is larger than 10 μs. Interestingly, for a wide range of rising/falling time of the disturbance (10 μs$-$1 ms), the brown-out detection level change is within 0.1 V of the designed value. This means that the voltage drops of $V_{\rm ctrl}$ and V_A by the brown-out event are sufficiently fast for such a disturbance.

Fig. 9 presents the measured effective reset time versus the disturbance duration during brown-out events. Here, the voltage drop of the disturbance $V_{\rm low}$ is given based on the values depicted in Fig. 8. The circuit can provide an effective reset

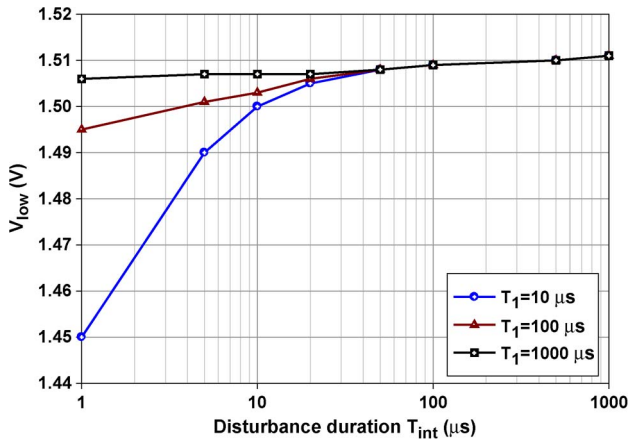

Fig. 8. Measured brown-out detection level versus the duration of a brown-out event.

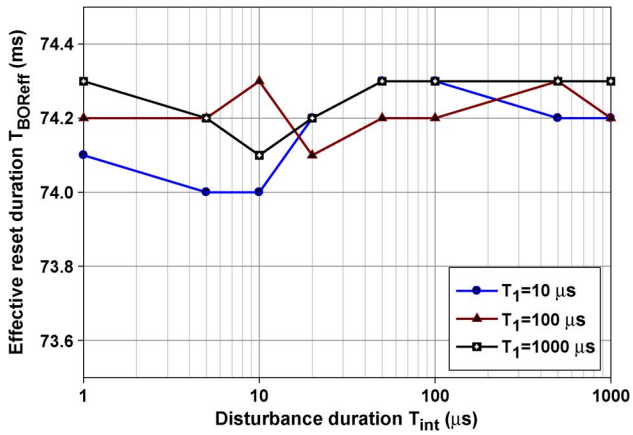

Fig. 9. Measured effective reset time with respect to duration of a brown-out event.

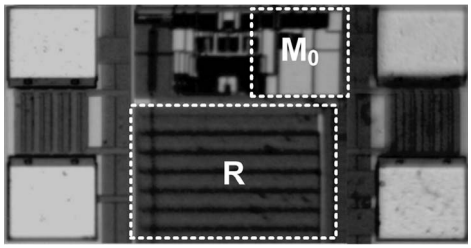

Fig. 10. Chip photograph.

time of about 74 ms during a brown-out event regardless of the rising/falling time.

Fig. 10 shows a photograph of the proposed circuit. The chip occupies a 120 μm $\times$ 100 μm active area, where resistor R and capacitor M_0 dominate the total chip size. The chip consumes a 1-μA static current, which is dominated by the current flowing through D_1/D_2, the current flowing through M_3, and the bias current through M_9. A performance summary and comparisons are provided in Table I.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Parameters	This design	[2]	[3]	[4]
Process	CMOS 0.18 µm	CMOS 0.25 µm	CMOS 65 nm	CMOS 0.5 µm
Supply	1.8 V	1.8 /2.5 V	1.1 V	1.8 ~ 5.0 V
Brown-out detection	Yes	No	Yes	Yes
Power-on rising time	≤ 1000 ms	≤ 50 ms	≤ 25 ms	≤ 1.0 ms
Power-on reset time	> 100 ms @ T_0 < 500 ms	≥ 500 ns	µs range	1.0 µs ~ 50 ms
Brown-out reset time	74 ms	No	µs range	NA
Static power	1.0 µA	NA	0	0
Active size	120 x 100 µm^2	115 x 345 µm^2	120 x 60 µm^2	35 x 55 µm^2

IV. CONCLUSION

An on-chip POR circuit with the capability of brown-out detection has been implemented with emphasis on long reset time. The proposed circuit can be used for various applications that require long reset time (on the order of hundreds of milliseconds) such as large-scale system-on-a-chip. The proposed circuit can also deal with a wide range of power-on rising time or brown-out transition time (from tens of microseconds to more than 1 s) while still providing long reset signals and a robust brown-out detection level. The circuit is fully integrated in a CMOS process with a small silicon area.

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