A New Approach to Low-Power and Low-Latency Wake-Up Receiver System for Wireless Sensor Nodes

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***Abstract*—A new wake-up receiver is proposed to reduce energy consumption and latency through adoption of two different data rates for the transmission of wake-up packets. To reduce the energy consumption, the start frame bits (SFBs) of a wake-up packet are transmitted at a low data rate of 1 kbps, and a bit-level duty cycle is employed for detection of SFBs. To reduce both energy consumption and latency, duty cycling is halted upon detection of the SFB sequence, and the rest of the wake-up packet is transmitted at a higher data rate of 200 kbps.**

The proposed wake-up receiver is designed and fabricated in a 0.18 μm CMOS technology with a core size of 1850x1560 μm² for the target frequency range of 902–928 MHz. The measured results show that the proposed design achieves a sensitivity of −73 dBm, while dissipating an average power of 8.5 μW from a 1.8 V supply.

***Index Terms*—Duty cycling, fast turn on/off, latency, low power, wake-up receiver, wireless sensor node.**

I. Introduction

LOW POWER implementation of wireless sensor nodes presents a considerable design challenge; and the transceiver of a wireless sensor node accounts for a majority of the power consumption [1], [2]. Low power transceivers for wireless sensor node applications have been proposed, but the power consumption of these transceivers is still excessive for deployment in ubiquitous sensing networks [3], [4]. As a result, other topologies have been developed to reduce power consumption [2]–[9]. The most common approach is the protocol based duty-cycling, in which the main receiver periodically monitors the channel for a wake-up signal [2]. Since the receiver is in sleep mode most of the time, the power consumption is significantly reduced, but at the cost of increased latency.

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To improve latency, reactive wake-up receivers, which operate continuously at a reduced power consumption, were proposed [5]–[7]. While the latency is improved, the wake-up receiver has a limited signal sensitivity for a given power consumption.

To further reduce the average power consumption while maintaining sensitivity, a duty cycling scheme is applied to a wake-up receiver in [8]. It should be noted that previously reported low power transceivers [3], [4] and reactive wake-up receivers [5]–[7] could be duty-cycled as well. However, as for the case of main receivers, duty cycling of wake-up receivers increases the latency of the receiver.

This work proposes a new method to reduce both energy consumption and latency. The proposed wake-up receiver offers two modes of operation, monitoring (MO) mode for receiving the start frame bits (SFBs) of the wake-up packet and identification (ID) mode for the rest of the data, namely node identification data. The wake-up receiver is duty-cycled only in MO mode, which is similar to extreme bit-level duty-cycling adopted in pulsed radios [9]. In ID mode, duty-cycling of the wake-up receiver halts and the data is received at a higher data-rate to reduce energy consumption and latency. The proposed design is fabricated in a 0.18 μm CMOS technology.

The remainder of the paper is organized as follows: In Section II, previously reported receiver schemes are analyzed in terms of average power consumption, transmitter and receiver energy consumption, and latency. Section III describes the proposed system including the format of the wake-up packet data and the operation of the wake-up receiver. The proposed data transmission methodology is then compared with previously reported schemes. Section IV reviews implementations of relevant wake-up receivers. Section V summarizes the measured performance of the wake-up receiver and compares it against existing ones.

II. Previously Reported Receiver Schemes

In this section, previously reported low power receiver schemes are analyzed and compared in terms of power consumption, energy consumption and latency. This analysis is useful in evaluating the performance of the proposed wake-up receiver [10]. Since the power consumption of the transmitter is a crucial factor in characterizing any wireless system, the energy required to wake up the intended receiver must also be considered in order to properly evaluate the overall performance of the proposed system. Note that low energy consumption, rather than power consumption, is a critical issue for any battery operated device such as wireless sensor nodes.

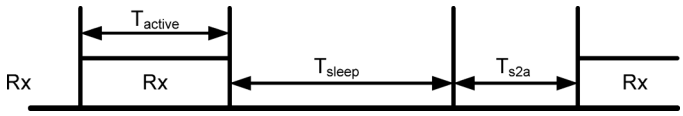

Fig. 1. Timing sequence of the protocol based duty-cycling.

The following four parameters are used throughout this paper.

$P_{\mathrm{avg},Rx}$: Average power consumption of the receiver in the channel monitoring state.

$E_{\mathrm{avg},Rx}$: Average energy consumption of the receiver to wake up the intended receiver.

$E_{\mathrm{avg,Tx}}$: Required average energy consumption of the transmitter to wake up the intended receiver.

L_{avg} : Average latency of a sensor node to wake up the intended receiver.

In the following analysis, it is assumed that (i) a packet is free of collision and (ii) there is no strong interference in the channel. In other words, wake-up packet data is successfully received as long as the entire packet arrives within the active period of the receiver.

A. Protocol Based Duty-Cycling Scheme

In protocol based duty-cycling, sensor nodes are heavily duty-cycled to reduce power consumption, spending most of the time in a low power sleep mode [2]. When a transmitter attempts to establish a data link with a certain sensor node, it sends a short wake-up packet to the receiver and waits for a reply. If the receiver is in the active mode when the wake-up packet arrives, the receiver sends an acknowledgement (ACK), and the data link is established. Otherwise, the transmitter repeatedly transmits the wakeup packet until either an ACK is received or it exhausts the maximum number of attempts.

Fig. 1 shows the timing sequence of the protocol based duty-cycling scheme. The main receiver listens to the channel during the active time period (T_{active}) and reverts to the sleep mode for (T_{sleep}). T_{s2a} represents the transition time from the sleep mode to the active mode. Thus, the average power consumption is obtained as

$$P_{\mathrm{avg},Rx} = \eta P_{Rx} + \left(\frac{T_{\mathrm{sleep}}}{T_{\mathrm{sleep}} + T_{s2a} + T_{\mathrm{active}}}\right) P_{\mathrm{sleep}} + \left(\frac{T_{s2a}}{T_{\mathrm{sleep}} + T_{s2a} + T_{\mathrm{active}}}\right) P_{s2a} \quad (1)$$

$$\eta = \frac{T_{\mathrm{active}}}{T_{\mathrm{sleep}} + T_{s2a} + T_{\mathrm{active}}} \quad (2)$$

where η is the duty-cycle and P_{Rx}, P_{sleep}, and P_{s2a} are the amounts of power consumption in the active mode, sleep mode, and transition mode, respectively. In general, since P_{sleep} is much smaller than P_{Rx} and T_{sleep} is much longer than T_{s2a}, the first term in (1) dominates the average power consumption. The minimum T_{active} is limited by the wake-up packet size, and hence T_{sleep} can be increased to reduce the average power consumption.

The minimum and maximum energy consumption as well as the latency of the scheme is illustrated in Fig. 2. Fig. 2(a) illustrates the case where the receiver is active during the first attempted transmission, which results in the minimum energy consumption of the receiver $(E_{Rx,\min})$, the minimum required energy consumption of the transmitter $(E_{Tx,\min})$ and the minimum latency $(L_{\min})$. In contrast, the wake-up packet arrives slightly after the active period of the receiver in Fig. 2(b), which results in the maximum energy consumption of the receiver $(E_{Rx,\max})$, the maximum required energy consumption of the transmitter $(E_{Tx,\max})$ and the maximum latency $(L_{\max})$.

The average energy consumption of the receiver $(E_{\mathrm{avg},Rx})$, the average required energy consumption of the transmitter $(E_{\mathrm{avg},Tx})$, and the average latency (L_{avg}) are expressed as

$$\begin{aligned} E_{\mathrm{avg},Rx} &= \frac{1}{2}(E_{Rx,\max} + E_{Rx,\min}) \\ &= \frac{1}{2}(T_{\mathrm{sleep}}P_{\mathrm{sleep}} + T_{s2a}P_{s2a} \\ &\quad + T_{\mathrm{active}}P_{Rx} + kT_bP_{Rx}) \end{aligned} \quad (3)$$

$$\begin{aligned} E_{\mathrm{avg},Tx} &= \frac{1}{2}(E_{Tx,\max} + E_{Tx,\min}) \\ &= \frac{1}{2}(T_{\mathrm{sleep}} + T_{s2a} + T_{\mathrm{active}} + kT_b)P_{Tx} \end{aligned} \quad (4)$$

$$\begin{aligned} L_{\mathrm{avg}} &= \frac{1}{2}(L_{\max} + L_{\min}) \\ &= \frac{1}{2}(T_{\mathrm{sleep}} + T_{s2a} + T_{\mathrm{active}} + kT_b) \end{aligned} \quad (5)$$

where k, T_b, and P_{Tx} are the number of wake-up bits, the bit duration, and the transmitter power consumption, respectively. Since P_{sleep} and P_{s2a} are typically low, the last two terms in (3) are dominant. Thus, the average energy consumption can be reduced by adopting the higher data-rate (or minimizing T_{active} and T_b). However, since a higher data-rate usually results in higher power consumption (P_{Rx}), increasing the data rate beyond a certain point fails to decrease energy consumption. Also, T_{active} is typically longer than kT_b since the wake-up packet should be received during the active time of the receiver. Consequently, this establishes a limiting factor on the ability of the protocol-based duty-cycling scheme to reduce energy consumption. While a larger value of T_{sleep} reduces power consumption, it increases the required energy consumption of the transmitter and latency as depicted in (4) and (5). Thus, (1), (4) and (5) establish a trade-off between average power consumption and latency as well as average power consumption and the required energy consumption of the transmitter.

B. Reactive Wake-Up Receiver Scheme

To overcome the limitation of the protocol based duty-cycling scheme, the reactive wake-up receiver scheme has been proposed [5]–[7]. Since a reactive wake-up receiver continuously monitors the channel, the latency and the required energy consumption of the transmitter are reduced substantially. Fig. 3

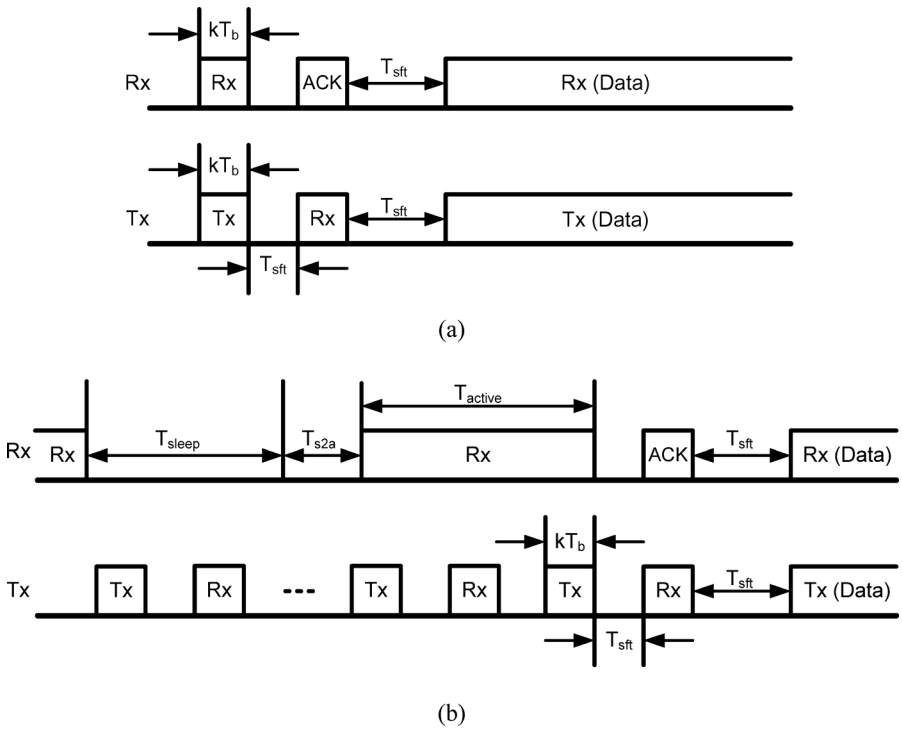

Fig. 2. Timing sequence of the (a) minimum and (b) maximum wake-up latency in the protocol-based duty-cycling scheme.

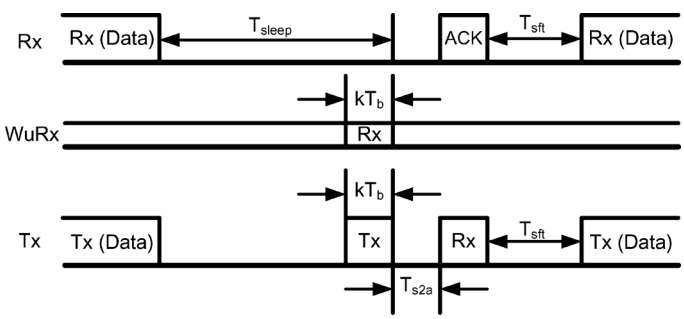

Fig. 3. Establishment of a data link for the reactive wake-up receiver scheme.

illustrates the procedure for establishing a data link. After detecting a correct wake-up packet (kT_b), the wake-up receiver activates the main receiver and an ACK is sent. An additional delay (T_{s2a}) results due to the activation time of the main receiver.

The average power consumption during the channel monitoring process can be estimated as

$$P_{\mathrm{avg},Rx} = P_{\mathrm{Wu}Rx} + P_{\mathrm{sleep}} \tag{6}$$

where $P_{\mathrm{Wu}Rx}$ is the power consumption of the wake-up receiver. Since the wake-up receiver is not duty-cycled, its active power dominates the average power consumption of the sensor node in (6). Compared with (1), even if $P_{\mathrm{Wu}Rx}$ is much smaller than P_{Rx}, the average power consumption of the scheme is larger than that of the protocol based-duty-cycling scheme because of an excessive duty-cycling ratio (η). The average energy consumption of the receiver $(E_{\mathrm{avg},Rx})$, the required energy consumption of the transmitter $(E_{\mathrm{avg},Tx})$ and average latency are given by

$$E_{\mathrm{avg},Rx} = T_{\mathrm{sleep}}(P_{\mathrm{Wu}Rx} + P_{\mathrm{sleep}}) \tag{7}$$

$$E_{\mathrm{avg},Tx} = kT_bP_{Tx} \tag{8}$$

$$L_{\mathrm{avg}} = kT_b \tag{9}$$

Comparing (4) and (5) to (8) and (9), a reactive wake-up receiver substantially reduces the average energy consumption of the transmitter and latency. However, when there is little activity on the channel, T_{sleep} increases and the average energy consumption of the reactive wake-up receiver becomes larger than that of the protocol-based duty-cycling scheme. This is due to the fact that continuously monitoring the channel, even at a reduced power level, consumes more energy than a main receiver operating in standby.

C. Duty-Cycled Wake-Up Receiver Scheme

The scheme reported in [8] is identical to the protocol based duty-cycling scheme except it employs duty-cycling at the wake-up receiver rather than the main receiver. When a wake-up packet is transmitted to the wake-up receiver in the active mode, the main receiver is activated and an acknowledgement (ACK) is sent. Fig. 4 shows the timing sequence of this scheme. During $T_{\mathrm{Wu,sleep}}$, the wake-up receiver is in sleep mode. $T_{\mathrm{Wu},s2a}$ is the amount of time required by the receiver to transition from the sleep mode to the active mode. The wake-up receiver monitors the channel only during $T_{\mathrm{Wu,active}}$.

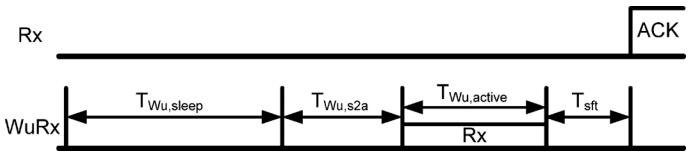

Fig. 4. Timing sequence of the duty-cycled wake-up receiver.

Thus, the average power consumption is as shown in (10)–(11) at the bottom of the page, where η_{Wu} is the duty-cycle ratio and $P_{\mathrm{Wu}Rx}$, $P_{\mathrm{Wu,sleep}}$, and $P_{\mathrm{Wu},s2a}$ is the power consumption of the active, sleep, and transition wake-up receiver mode, respectively. The average power consumption of the scheme in (10) is lower than that described in (1) and (6) due to the low active power $(P_{\mathrm{Wu}Rx})$ and duty-cycle ratio (η_{Wu}).

The minimum and maximum energy consumption along with the latency of the scheme is illustrated in Fig. 5. Similar to the protocol based duty-cycling scheme (Fig. 2), the minimum energy consumption of the receiver $(E_{Rx,\min})$ and transmitter $(E_{Tx,\min})$ as well as the minimum latency $(L_{\min})$ are achieved when the wake-up receiver is active for the first attempted transmission (Fig. 5(a)). In Fig. 5(b), the wake-up packet arrives slightly after the first active period of the wake-up receiver, thereby yielding the maximum energy consumption in both the receiver $(E_{Rx,\max})$ and transmitter $(E_{Tx,\max})$ while establishing the maximum latency $(L_{\max})$.

The average energy consumptions and latency of the receiver are then given as shown in (12)–(14) at the bottom of the page.

From (12), the 3rd term dominates the average energy consumption due to the low $P_{\mathrm{Wu,sleep}}$, $P_{\mathrm{Wu},s2a}$ and P_{sleep}. Since $P_{\mathrm{Wu}Rx}$ is lower than P_{Rx}, the average energy consumption in (12) is lower than that described in (3). Compared to (7), the average energy consumption in (12) is also lower than that of the reactive wake-up receiver scheme due to the larger T_{sleep} in (7). However, from (13) and (14), the required energy dissipation of the transmitter and average latency of the duty-cycled wake-up receiver are the same as that exhibited in the protocol-based duty-cycling scheme. As a result, this method achieves lower energy consumption than the protocol-based duty-cycling and reactive wake-up receiver schemes in the receiver side, but with no improvement in the required energy consumption of the transmitter or latency.

III. The Proposed Wake-Up Receiver System

In this section, the proposed wake-up receiver system is described. The format of the implemented wake-up data packet is discussed, as well as the system level operation of the proposed wake-up receiver. Additionally, the energy consumption and latency are analyzed.

A. Wake-Up Packet Format and the System Operation

Fig. 6(a) illustrates the proposed wake-up data packet, which is composed of the SFBs followed by the ID data. The SFB sequence indicates the start of the wake-up data packet. The ID data consists of a 6-bit ID start sequence bits (IDSBs), a 2-byte ID code, and one parity bit, where Manchester encoding is applied to the ID code and the parity bit. The ID code contains the node identification number and the broadcast mode, unicast or broadcast.

The proposed wake-up receiver operates in two different modes, monitoring (MO) and identification (ID). The receiver monitors the channel to detect the SFB sequence in the MO mode. Upon detection of the SFB sequence, it switches to

$$P_{\mathrm{avg},Rx} = \left\{ \begin{array}{l} P_{\mathrm{sleep}} + \eta_{\mathrm{Wu}} P_{\mathrm{Wu}Rx} + \left(\frac{T_{\mathrm{Wu,sleep}}}{T_{\mathrm{Wu,sleep}} + T_{\mathrm{Wu},s2a} + T_{\mathrm{Wu},active}} \right) P_{\mathrm{Wu,sleep}} \\ + \left(\frac{T_{\mathrm{Wu},s2a}}{T_{\mathrm{Wu,sleep}} + T_{\mathrm{Wu},s2a} + T_{\mathrm{Wu,active}}} \right) P_{\mathrm{Wu},s2a} \end{array} \right\} \tag{10}$$

$$\eta_{\mathrm{Wu}} = \frac{T_{\mathrm{Wu,active}}}{T_{\mathrm{Wu,sleep}} + T_{\mathrm{Wu},s2a} + T_{\mathrm{Wu,active}}} \tag{11}$$

$$\begin{aligned} E_{\mathrm{avg},Rx} &= \frac{1}{2}(E_{Rx,\max} + E_{Rx,\min}) \\ &= \frac{1}{2} \left\{ \begin{array}{l} T_{\mathrm{Wu,sleep}} P_{\mathrm{Wu,sleep}} + T_{\mathrm{Wu},s2a} P_{\mathrm{Wu},s2a} + (T_{\mathrm{Wu,active}} + kT_b) P_{\mathrm{Wu}Rx} \\ + (T_{\mathrm{Wu,sleep}} + T_{\mathrm{Wu},s2a} + T_{\mathrm{Wu,active}}) P_{\mathrm{sleep}} \end{array} \right\} \end{aligned} \tag{12}$$

$$\begin{aligned} E_{\mathrm{avg},Tx} &= \frac{1}{2}(E_{Tx,\max} + E_{Tx,\min}) \\ &= \frac{1}{2}(T_{\mathrm{Wu,sleep}} + T_{\mathrm{Wu},s2a} + T_{\mathrm{Wu,active}} + kT_b) P_{Tx} \end{aligned} \tag{13}$$

$$\begin{aligned} L_{\mathrm{avg}} &= \frac{1}{2}(L_{\mathrm{Wu},\max} + L_{\mathrm{Wu},\min}) \\ &= \frac{1}{2}(T_{\mathrm{Wu,sleep}} + T_{\mathrm{Wu},s2a} + T_{\mathrm{Wu,active}} + kT_b) \end{aligned} \tag{14}$$

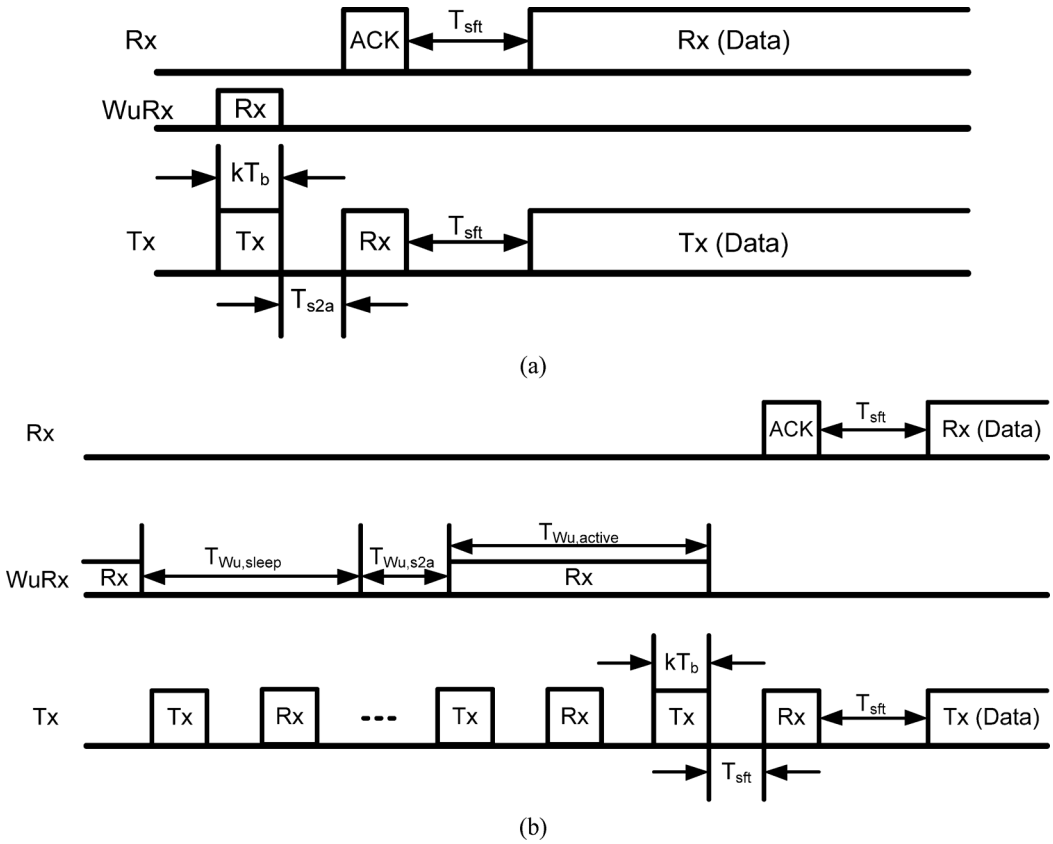

Fig. 5. Timing analysis of the (a) minimum and (b) maximum wake-up latency in the duty-cycled wake-up receiver scheme.

the ID mode and receives and processes the ID data. The IDSBs are inserted to signal the start of the ID data, which ensures reliable operation given the variation in the MO mode to ID mode transition time of different wake-up receivers.

The reactive wake-up receivers of [5]–[7] continuously search for the SFB sequence during the MO mode. Since the duty cycle of typical wireless sensor nodes is very low, the energy consumed for the search is mostly wasted. To address this problem, the proposed design adopts a duty cycling of the wake-up receiver at the bit level. In other words, the wake-up receiver is in the active mode for only a fraction of each bit duration. Fig. 6(b) illustrates that the duty cycle of the wake-up receiver is 0.6% at the bit level, or active for only 6 μs for each bit duration (1 ms). Suppose that the minimum-required-active-time of a wake up receiver is $\Delta_{\mathrm{on\_min}}$, which includes the transition time to turn on and turn off the receiver. Then the minimum active time period of the wake-up receiver to detect an SFB sequence is $m\Delta_{\mathrm{on\_min}}$, where m is the number of bits in the SFB sequence and $m = 8$ for the proposed data packet in Fig. 6(a). Note that in such a case each SFB bit is detected once and only once during each active time. To minimize the energy consumption during the MO mode, we need to (i) decrease the data rate of the SFB sequence and (ii) reduce the energy consumption during the active period of the receiver. Case (i) comes at the cost of increasing the latency. To meet the objective of case (ii), we need to minimize both $m\Delta_{\mathrm{on\_min}}$ and the power consumption of the wake-up receiver in active mode.

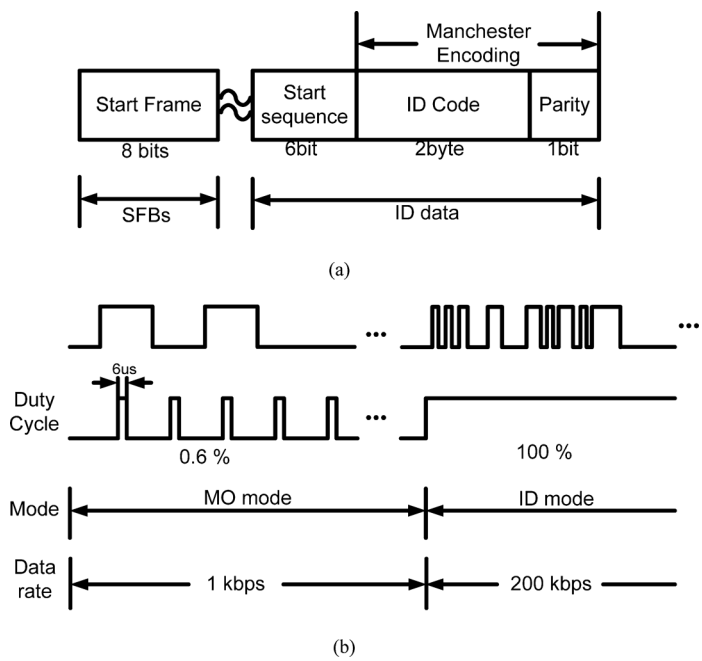

Fig. 6. The format of the wake-up data packet and operation of the proposed wake-up receiver system. (a) Format of the wake-up data packet. (b) Operation.

Since the ID data is ensured to follow the SFB sequence, the energy consumption during the ID mode is the product of the

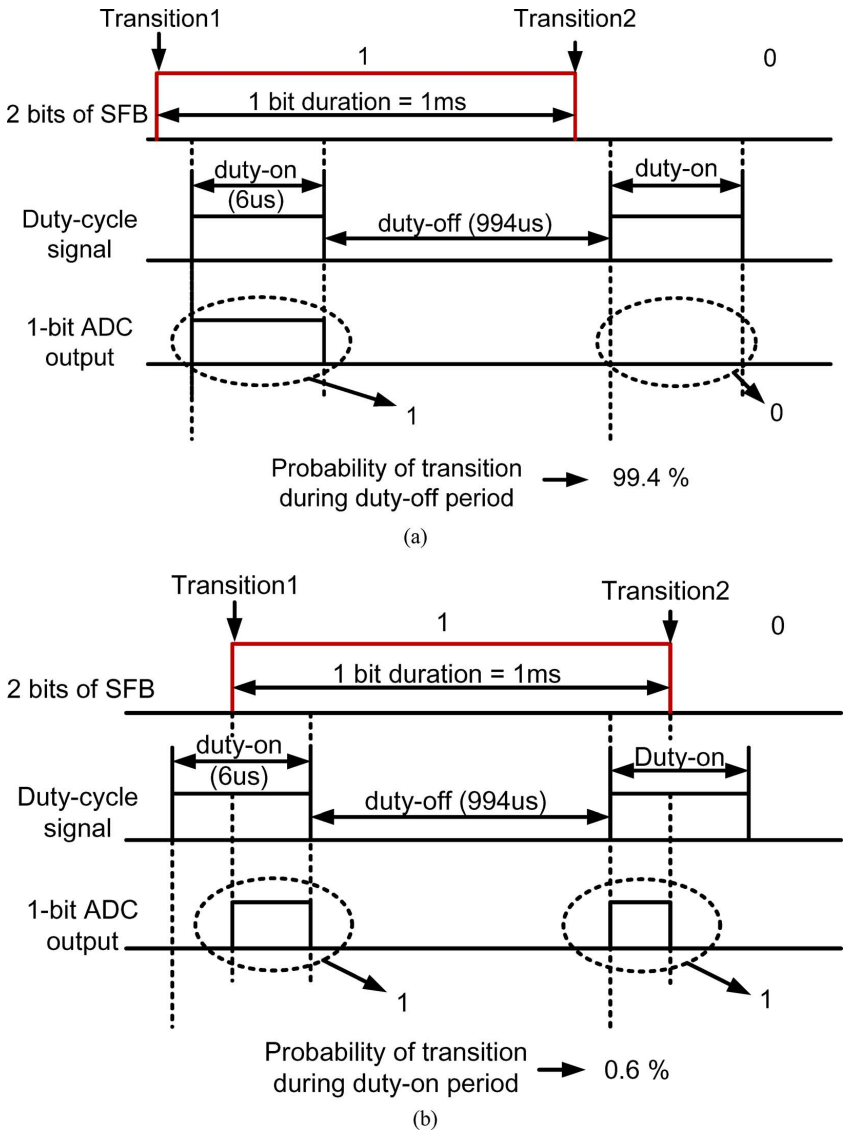

Fig. 7. The timing diagram of the SFB transition occurred in (a) duty-off period and (b) duty-on period.

total accumulative active time of the wake-up receiver and the power consumption of the receiver in the active mode. It implies that the data rate of the ID data should be as high as possible to minimize the total active time; and the maximum data rate is achieved when the wake-up receiver is turned on continuously. Note that application of a duty cycling scheme in the ID mode does not reduce the energy consumption, but simply increases the latency.

Fig. 6(b) shows the high level operation of the proposed wake-up receiver. The SFBs are transmitted at a low data-rate of 1 kbps, and hence the switching frequency of the wake-up receiver is set to 1 KHz. The wake-up receiver is active for only 6 μs (or 0.6% duty cycle) for each switching period of 1 ms during the MO mode. The ID data is transmitted at an increased data-rate of 200 kbps, while the wake-up receiver is turned on continuously during the ID mode. It is interesting to note that even though the size of the ID data is about three times that of the SFB sequence, the transmission time of the ID data (= 115 μs) is a fraction of the SFB transmission time (= 8 ms). The latency of the proposed receiver is 8.1 ms, which is a substantial improvement over the 1.15 s reported in [8].

While the bit-level duty cycling helps to minimize latency, the short sampling period employed by the receiver can cause detection errors, thereby degrading the sensitivity of the receiver. Fig. 7 illustrates the operation of the receiver when the SFB transition occurs in the duty-off and duty-on period. In Fig. 7(a), the SFB transitions occur within the duty-off period so that the two SFB bits are correctly sampled and no errors are incurred. In contrast, in Fig. 7(b), the SFB transitions occur within the duty-on period and a bit error results at the 1-bit ADC output. However, the probability of an SFB transition occurring within the duty-on period of the receiver is merely 0.6% (while that during the duty-off time is 99.4%). Thus, these transitions have little impact on the sensitivity of the proposed receiver.

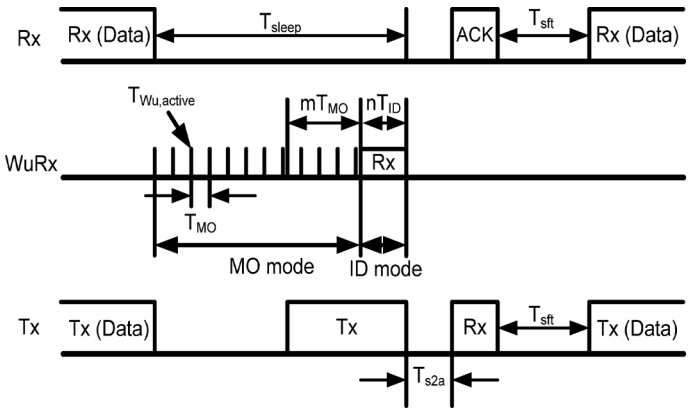

Fig. 8. Timing sequence to establish a data link for proposed wake-up receiver scheme.

B. Analysis of the Power and Energy Consumption and Latency

As discussed in Section II, the protocol based duty-cycling and duty-cycled wake-up receiver schemes suffer from large latency and required transmitter energy consumption. The reactive wake-up receiver scheme alleviates these problems, but becomes inefficient in the receiver energy consumption for a low channel activity.

Fig. 8 illustrates the timing sequence to establish a data link for the proposed wake-up receiver scheme. In the MO mode, the wake-up receiver is activate for a small fraction of the bit duration, $T_{\rm MO}$, and monitors the channel during the active time, $T_{\rm Wu,active}$, (which is equal or greater than minimum-required-active-time $\Delta_{\rm on\_min}$). After detection of the SFB sequence transmitted during the time interval $mT_{\rm MO}$, where m is the number of bits for the SFB sequence, the wake-up receiver transitions to the ID mode and receives the ID data at a higher data-rate. Once a wake-up data packet is detected during the time interval $(mT_{\rm MO} + nT_{\rm ID})$, where $T_{\rm MO}(T_{\rm ID})$ is the bit duration in the MO (ID) mode and $m(n)$ is the number of bits of the SFB sequence (ID data), the wake-up receiver activates the main receiver and the ACK is transmitted. As the proposed scheme essentially cycles the wake-up receiver within the duration of a single bit, we refer to this as bit-level duty cycling.

In the proposed wake-up receiver scheme, the average power consumption is given as

$$P_{\rm avg} = (\eta_{Wub} P_{{\rm Wu}Rx}) \left(\frac{T_{\rm sleep} - nT_{\rm ID}}{T_{\rm sleep}} \right) + P_{{\rm Wu}Rx} \frac{nT_{\rm ID}}{T_{\rm sleep}} + P_{\rm sleep} \quad (15)$$

$$\eta_{Wub} = \frac{T_{\rm Wu,active}}{T_{\rm MO}} \quad (16)$$

where η_{Wub} is the bit-level duty-cycle and $P_{{\rm Wu}Rx}$ is the power consumption of the wake-up receiver in the active mode. In (15), the first and second terms dominate the average power consumption of the receiver. Thus, the average power consumption can be decreased by reducing the bit-level duty-cycle (η_{Wub}) and/or $T_{\rm ID}$in the ID mode (equivalently increasing the data rate). Assuming that $P_{{\rm Wu}Rx}$ is much lower than P_{Rx} and $T_{\rm sleep}$ is much longer than $T_{\rm active}$ or $mT_{\rm MO} + nT_{\rm ID}$, comparison of (15) with (1) and (6) shows that the average power consumption of the proposed scheme is lower than that of the protocol-based duty-cycling and reactive wake-up receiver scheme.

The average energy consumption of the receiver and the transmitter as well as the latency of the proposed system are given as

$$E_{{\rm avg},Rx} = T_{\rm sleep} P_{\rm sleep} + (T_{\rm sleep} - nT_{\rm ID})\eta_{Wub} P_{{\rm Wu}Rx} + nT_{\rm ID} P_{{\rm Wu}Rx} \quad (17)$$

$$E_{{\rm avg},Tx} = (mT_{\rm MO} + nT_{\rm ID}) P_{Tx} \quad (18)$$

$$L_{\rm avg} = mT_{\rm MO} + nT_{\rm ID} \quad (19)$$

Similar to the average power consumption in (15), the average energy consumption of the receiver in (17) is also decreased by decreasing η_{Wub} and/or $T_{\rm ID}$. Furthermore, since $T_{\rm ID}$ is much smaller than $T_{\rm MO}$, the required energy consumption of the transmitter and latency are minimized by allocating a smaller m and larger n for a given wake-up data packet size of $(m + n)$. Comparing (17) with (3) and (7), the energy consumption of the proposed receiver is lower than that of the protocol based duty-cycling and reactive wake-up receiver schemes. Further, since $T_{\rm sleep}$ is typically much longer than $T_{\rm active}$ or $mT_{\rm MO} + nT_{\rm ID}$, the proposed scheme exhibits better performance over protocol-based duty-cycling and duty-cycled wake-up receiver schemes in the transmitter energy consumption and latency.

In summary, the proposed, bit-level duty cycling scheme is capable of simultaneously reducing average power and energy consumption for both the receiver and the transmitter, while also reducing the latency. The next section explores a wake-up receiver architecture that can facilitate the proposed scheme.

IV. Implementation of the Proposed Wake-Up Receiver

A. The Wake-Up Receiver Architecture

Wake-up receivers are often implemented with super-regenerative amplifiers due to their high sensitivity and relatively low power consumption [5]. The super-regenerative receiver (SRR) architecture exploits a different start-up time of an oscillator, which is determined by the presence of an RF carrier. Since the SRR detects the start-up time of a high output oscillator signal, high sensitivity can be achieved. Although the SRR can be duty-cycled using a quench signal, the time required for oscillations to build severely limits the speed of the receiver. Thus, SRRs are applicable only for low bit-rates. Consequently, they are not suitable for the proposed receiver requiring a rapid duty-cycling ratio (0.6%) and a high ID-mode data-rate.

The uncertain-IF architecture constitutes another implementation of a wake-up receiver [7]. It uses a low power ring oscillator to down-convert the RF signal to an IF frequency. Since the signal is amplified at an IF frequency, it achieves high sensitivity with low power consumption. However, a ring oscillator incurs a long transition time from sleep to active mode (T_{s2a}), which is unsuitable for a rapid bit-level, duty-cycling required for the proposed design.

The proposed wake-up receiver adopts an RF-diode based receiver architecture, which is similar to the first AM receiver

architecture [6]. This architecture is suitable for the proposed design since it achieves low power consumption and can easily accommodate fast duty-cycling. The RF-diode receiver consists of an amplifier, an envelope detector and an analog-to-digital converter (ADC). However, it has two fundamental drawbacks. First, since the envelope detector down converts the RF signal to the baseband signal, selectivity must be provided by narrow-band filtering at RF. Second, a high RF gain is required to overcome the sensitivity limitations of the envelope detector. Selectivity at RF can be achieved by adopting a high Q bulk acoustic wave (BAW) resonate filter [6] or saw-filter between the antenna and low noise amplifier. The poor sensitivity of the RF-diode based receiver, however, is not as easily mitigated as there exists a strong trade-off between power consumption and RF gain. In conventional RF-diode based receiver, the system noise figure is given as follows [11]:

$$F_{\rm tot} = 2F_{\rm amp} + \frac{N_{\rm LF}k_{\rm DC}^2}{N_{\rm src}A_v^2k^2} + \frac{N_{o,D}}{N_{\rm src}A_v^2k^2} \tag{20}$$

where $F_{\rm amp}$ represents the noise figure of the amplifier, $N_{\rm LF}$ the low frequency noise at the output of the amplifier, $k_{\rm DC}$ the DC gain of the detector, $N_{\rm src}$ the noise from the source resistance, A_v the voltage gain of the amplifier, k the conversion gain of the envelope detector, and $N_{o,D}$ the output noise power of the envelope detector, respectively. The last two terms tend to dominate the noise figure of the system due to the poor conversion gain of the detector (k). Increasing the voltage gain, A_v, of the preceding amplifier can reduce the noise contributions of these two terms, but a higher gain increases the power consumption.

As will be shown, the proposed method helps to alleviate this issue. Since the proposed wake-up receiver is heavily duty-cycled during the MO mode, a high gain does not dictate a high amount of power consumption. Consequently, the proposed wake-up receiver exploits the simple configuration of the RF-diode based design, as it can be quickly power cycled, to obviate this trade-off and achieve an improved sensitivity without increasing power consumption.

B. The Proposed Wake-Up Receiver Design

Fig. 9 shows the block diagram of the proposed wake-up receiver. It consists of an amplifier, a detector, an ADC and digital circuitry. The switch gates the power of the wake-up receiver to implement duty-cycling in the MO mode. After reception of a SFB sequence, the switch remains closed while receiving the ID data in the ID mode. The digital controller processes the wake-up data packets and controls the operation of the receiver. Use of a customized digital controller rather than a general purpose processor or DSP chip saves power for the proposed wake-up receiver system.

Fig. 10 shows the schematic of the cascaded amplifier. The first stage of the cascaded amplifier adopts an inverter-type amplifier with resistive feedback for reasonable gain and input-matching in the ultra-low power regime. Considering the non-quasi-static (NQS) effect of MOS transistors [12], the real part

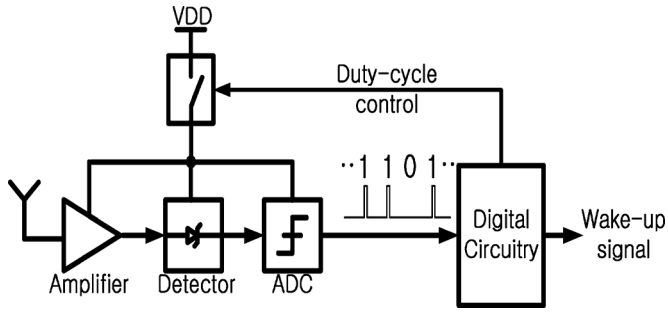

Fig. 9. The block diagram of the proposed wake-up receiver.

of the input impedance $(R_{\rm int})$ when looking into the intrinsic gate terminal of the MOS transistor is given by

$$R_{\rm int} \cong \frac{4n}{5(3n-1)^2 g_m} \tag{24}$$

where n is the subthreshold swing constant $(\cong 1.3)$ and g_m is the transconductance of the MOS transistor, respectively [12]. Since the transconductance of an inverter type amplifier is high due to current sharing, input matching is easily achieved even in the ultralow power operating regime. Since the gain of the inverter amplifier is $(g_{m,M1} + g_{m,M2})/\omega C_N$, where C_N is the parasitic capacitance at the drain node, the inverter amplifier provides a moderate gain. The off-chip inductor (L_g) cancels the imaginary part of the input impedance.

The subsequent stages of the cascaded amplifier adopt a current-reused structure to facilitate both a high gain and low current consumption. The 6th amplification stage of the cascaded amplifier utilizes an off-chip inductor and capacitor ($L_{\rm load}$ and $C_{\rm load}$) to provide a high impedance load at the input frequency. The rest of the amplification stages adopt resistive loads to meet the required current consumption, operating frequency, and chip size. The resistive loads sacrifice a negligible amount of voltage headroom due to the low bias current. A band-gap reference circuit [13], which includes a start-up circuit for a fast activation, provides accurate, sub-threshold region biasing. The cascaded amplifier draws 478 μ A from a 1.8 V supply. The band-gap reference circuit consumes 90 μ A of current from the same supply.

Fig. 11 shows the schematic of the envelope detector and I-V curve of a CMOS transistor operating in both the sub-threshold and saturation biasing region. In Fig. 11(a), the differential pair ($\rm M_1$ and $\rm M_2$) of the envelope detector operates in the sub-threshold region. When CMOS transistors operate in sub-threshold region biasing, the I-V characteristic closely resembles that of bipolar transistors (Fig. 11(b)). Thus, the RF input signal is rectified by the I-V characteristic of $\rm M_1$. Since the sum of the bias currents of $\rm M_1$ and $\rm M_2$ is fixed at $\rm I_{BIAS}$, the drain current of $\rm M_2 (I_{M2})$ is inverted with respect to the RF signal and extracted through a low pass filter ($\rm M_4$ and $\rm C_2$). To minimize the conversion loss, an active current mirror is used. The current consumption of the envelope detector and the bias circuit are 13 and 1 μ A from the 1.8 V supply, respectively.

A key design objective, in addition to low power consumption and high gain, is to minimize the minimum-required-ac-

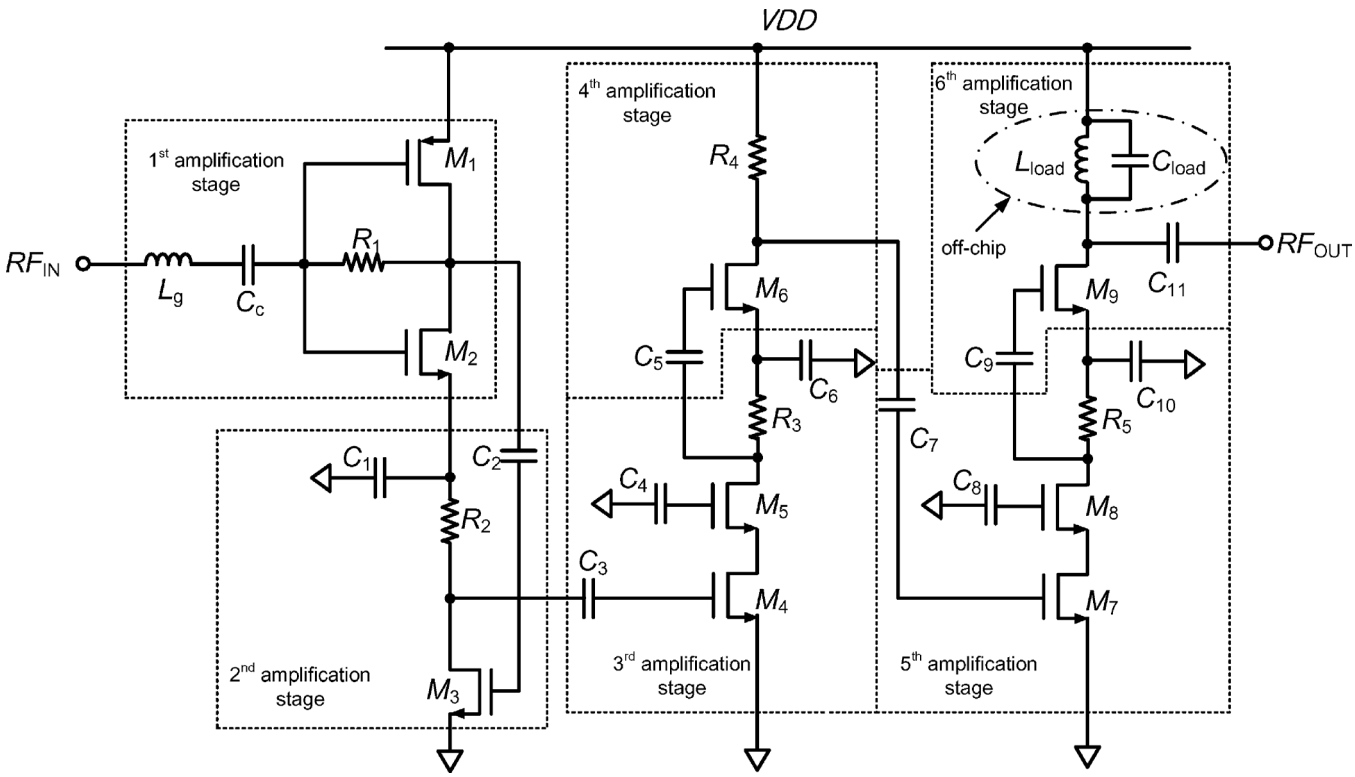

Fig. 10. The schematic of the cascaded amplifier.

tive-time, $\Delta_{\mathrm{on\_min}}$, which corresponds to minimizing the time needed to activate/deactivate the circuit. Since the bias current of the cascaded amplifier is large (to achieve a high RF gain), the turn-on time of the cascaded amplifier tends to be short. In contrast, the envelope detector draws a small bias current, leading to a relatively long turn-on/off. Fig. 12(a) and (b) show the conventional and proposed power on/off techniques, respectively. For the conventional power on/off technique, the bias circuit is switched on and off by toggling S_1, which then activates/deactivates the envelope detector. In contrast, the proposed power on/off technique allows the bias circuit to remain active while the envelope detector is switched on and off with S_3. Fig. 13(a) and (b) shows the waveforms of the conventional and proposed power on/off techniques, respectively. In Fig. 13, $\mathrm{S}_1, \mathrm{S}_2, \mathrm{S}_3$, and S_4 are closed for a logic low signal and on for a logic high. In the conventional technique, the bias circuit provides a stable bias voltage to the envelope detector after some startup time, thereby increasing the time required for the output of the envelope detector to settle once S_1 is closed (S_1 is transitions to a low). In the proposed technique, the bias circuit always provides a bias voltage, thus allowing the output of the envelope detector to reach its settling voltage immediately when S_3 is closed. While this slightly increases the power consumption, the shorter turn-on time of the envelope detector significantly reduces $\Delta_{\mathrm{on\_min}}$. To shorten the turn-off time, the discharging switches (S_2 and S_4) are connected to the output in Fig. 12. The two switches discharge the capacitor ($\mathrm{C_{L1}}$ and $\mathrm{C_{L2}}$) quickly, facilitating a fast turn off. It should be noted that the longest turn-on (turn-off) time of a block dictates the turn-on (turn-off) time of the wake-up receiver.

Fig. 14 shows the schematic of the 1-bit ADC, which consists of switched capacitors, a pre-amplifier, a D-latch/D filp-flop, and clock generator. The switched capacitors and the pre-amplifier cancel the input DC offset [14]. The cancellation is performed by closing a unity-gain loop around the pre-amplifier and storing the offset on the input coupling capacitors (C_1 and C_2). The reference voltage is controlled externally. The 1 MHz ADC clock is derived from a low-power, off-chip 24 MHz oscillator through the digital circuitry. The current consumption of the 1-bit ADC excluding the off-chip oscillator is 17 μA from the 1.8 V supply voltage. The proposed power on/off technique shown in Fig. 12(b) is also adopted by the pre-amplifier in the 1-bit ADC for fast turn-on and off time.

Fig. 15 shows the block diagram of the digital circuitry connected to an off-chip serial peripheral interface bus (SPI-Bus). The circuit contains two subsystems, a control logic block and a data decoder. The control logic block consists of an SFB sequence detector, a duty cycle control module, and a timer block. The control logic block generates the duty-cycle control signal in Fig. 8, which performs the bit-level duty-cycling in the MO mode or makes the transition of the operation mode. The decoder includes a transition finder, sync pattern detector, bit counter, de-serializer, parity check module and ID compare block. The decoder is enabled by the SFB detector of the control logic block upon detection of the SFB sequence. After detection of the IDSBs, the transition finder decodes the ID code, which is Manchester encoded. Next, the data is parallelized by the de-serializer and compared against the unique ID code of the receiver. If the ID data matches the code of the receiver, a wake-up signal is issued on the SPI bus to wake

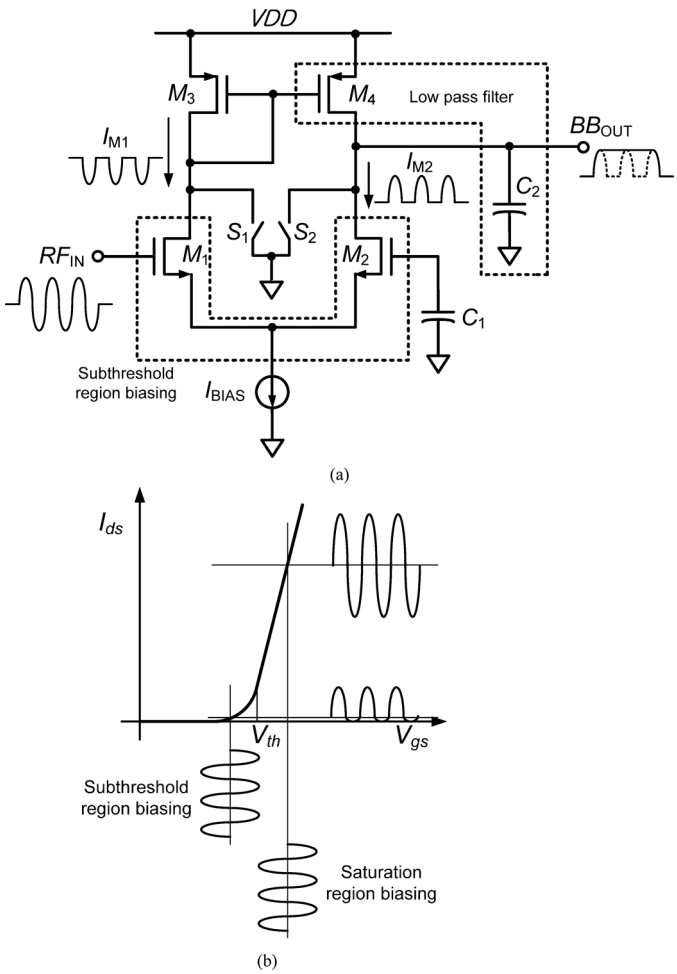

Fig. 11. (a) The schematic of the envelope detector and (b) CMOS transistor's I-V curve for the sub-threshold and saturation region biasing.

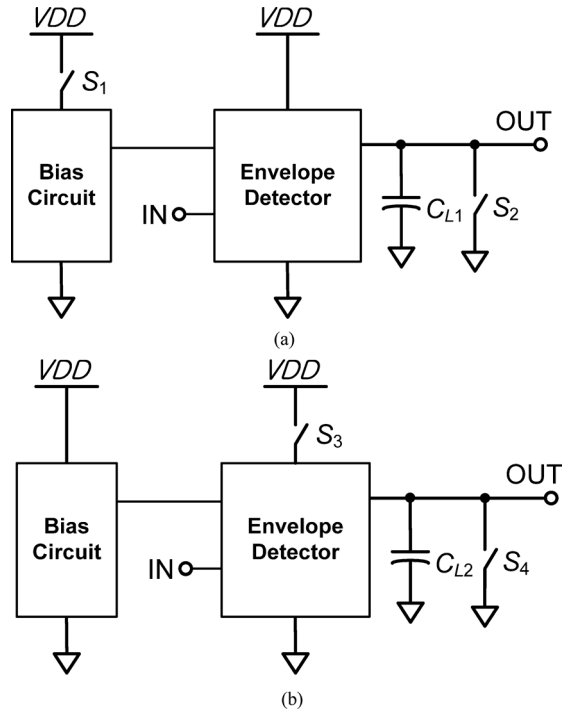

Fig. 12. (a) The conventional power on/off technique. (b) The proposed power on/off technique.

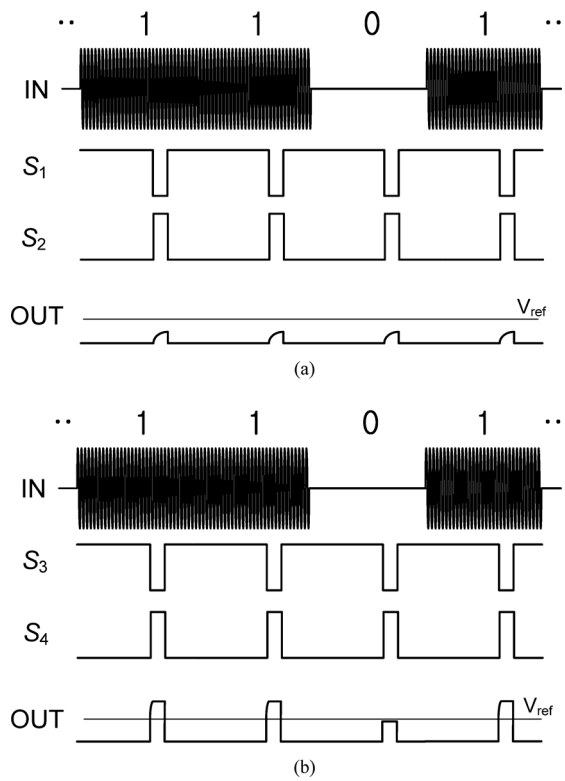

Fig. 13. (a) Waveforms of the conventional power on/off technique. (b) Waveforms of the proposed power on/off technique.

up the main transceiver. The digital circuitry was synthesized from a Verilog description and has around 4000 gates.

V. Measurement

The proposed wake-up receiver is designed and fabricated in a 0.18 μm CMOS technology for the target frequency range of 902–928 MHz. Table I summarizes measured DC currents of individual blocks from a 1.8 V supply for both the MO and ID mode. The wake-up receiver dissipates an average power of 8.4 μW for a duty cycle of 0.6% in the MO mode and a continuous power of 1.1 mW in the ID mode.

A. Measurement Setup

The measurement setup is shown in Fig. 16. In Fig. 16(a), the transmitter board, which is composed of commercial components (power-amplifier, PLL synthesizer, switch and modem implemented by FPGA), is used to generate the transmitter code signals. An oscilloscope is used to measure the waveforms of the envelope detector, 1-bit ADC, duty-control signal, and wake-up pulse. In Fig. 16(b), the vector signal generator (Agilent E4438C) is used to generate the OOK modulated signal-code for both the MO and ID modes of operation. For MO mode testing, an incorrect SFB code is intentionally transmitted to the receiver so that the BER can be measured without incurring ID mode operation. For ID mode testing, MO mode operation is deactivated through the SPI interface, thereby allowing measurement of BER. The OOK modulated

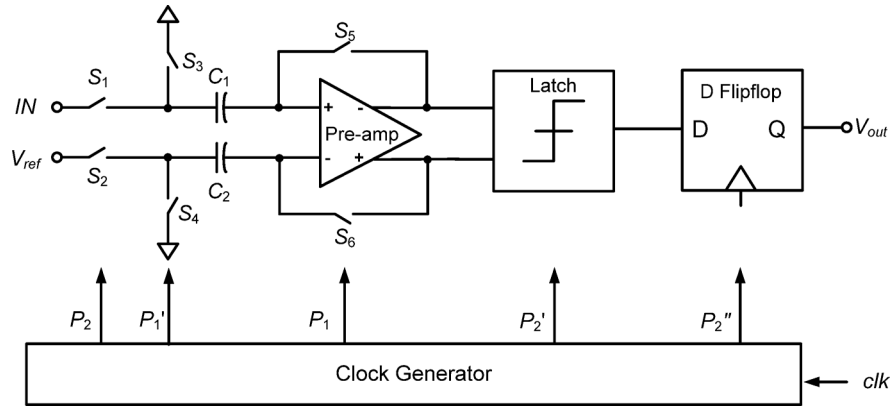

Fig. 14. The schematic of the 1-bit ADC.

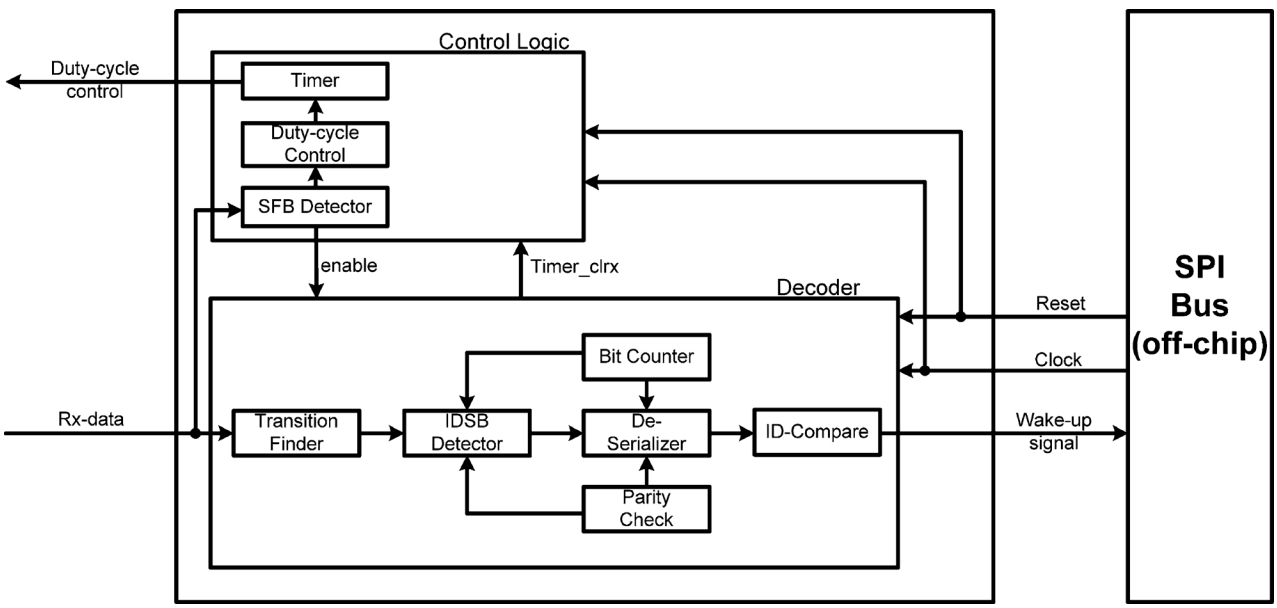

Fig. 15. Block diagram of the digital circuitry connected to SPI-Bus.

input signal-code is transmitted to the DUT, repeatedly and the 1-bit ADC output data is stored in the logic analyzer. The original bits and stored output data bits are compared using a MATLAB script in order to calculate the bit-error rate (BER) and the corresponding sensitivity of the wake-up receiver.

B. Measurement Results

Fig. 17 shows measured S-parameters of the cascaded amplifier. The input return loss, S11, is greater than 10 dB from 870 MHz to 910 MHz. The peak of S11 is shifted to a lower frequency (890 MHz) due to an inaccurate estimation of the input parasitic capacitance of the first amplification stage of the cascaded amplifier. The forward gain, S21, is from 34 to 42 dB for the target frequency range of 902–926 MHz and the peak gain is approximately 47 dB at 890 MHz.

Fig. 18 shows the measured voltages at the output of the envelope detector and 1-bit ADC during reception of one bit of data. The turn-on time of the wake-up receiver is 1.6 μs and the turn-off time of the wake-up receiver is negligible due to the instantaneous discharge of the output nodes through the two switches S_2 and S_4 in Fig. 12. The output of the ADC transitions high approximately two clock cycles after the input voltage reaches V_{ref} due to the switched capacitors, preamplifier, D flip-flop, and latch that comprise the ADC. It remains high for one clock cycle after the output of the envelope detector goes low due to the fast discharge switches, which are implemented in the preamplifier of the ADC. The output of the ADC is high for a total of 4 μs. Therefore, the minimum-required-active-time $\Delta_{\mathrm{on\_min}}$ of the wake-up receiver is about 6 μs, and a very small $\Delta_{\mathrm{on\_min}}$ reduces the power consumption of the receiver during the MO mode. Recall that the bias circuits for the envelope detector and 1-bit ADC remain active while the bandgap reference for the cascaded amplifier is duty-cycled.

Fig. 19 shows the voltage waveforms of the ADC, the duty-cycle control signal and the wake-up signal. A wake-up pulse is generated successfully at the end of the ID mode, which demonstrates correct operation of the wake-up receiver.

Fig. 20 shows the measured bit error rate (BER) versus the sensitivity of the proposed wake-up receiver in both the MO and

TABLE I
MEASURED POWER CONSUMPTION OF THE INDIVIDUAL BLOCKS

Average Power Consumption (μW)	Cascaded Amplifier	Envelope Detector	1-bit ADC	Band-gap Reference	Bias circuit for analog blocks	Total Power
MO mode (0.6 % duty cycle)	5.166	0.14	0.184	0.972	1.98*	8.442
ID mode (100 % duty cycle)	860.4	23.4	30.6	162	1.98	1078.4

Note: The value marked with "*" does not employ the duty-cycling scheme.

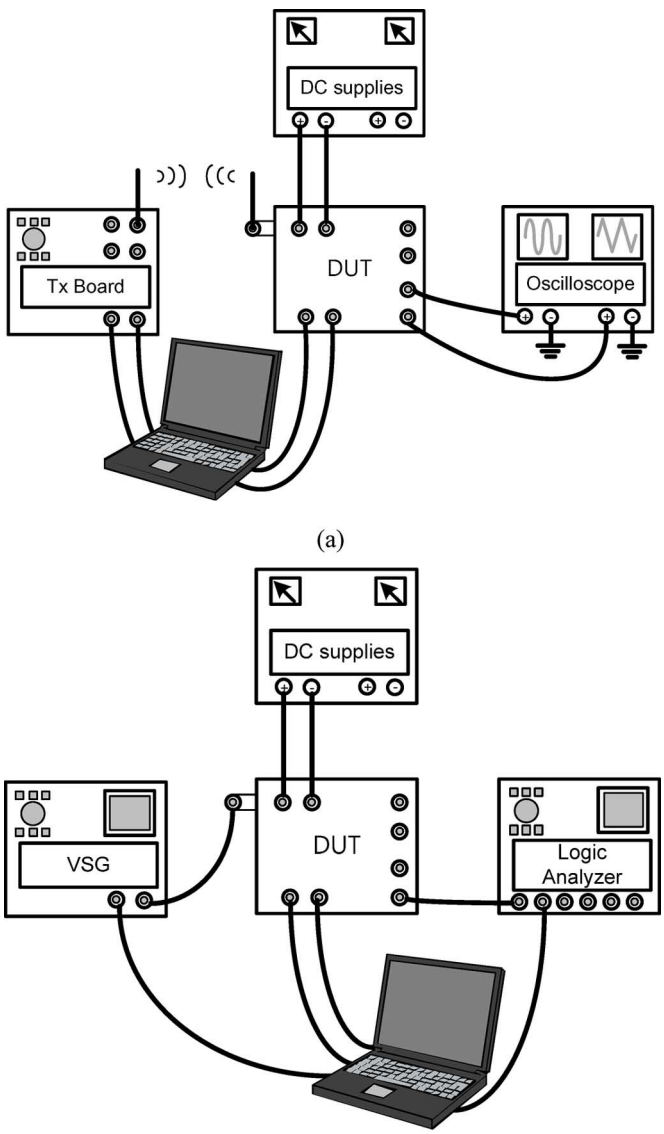

Fig. 16. Measurement setup of (a) the output waveforms and (b) the bit-error rate and the corresponding sensitivity.

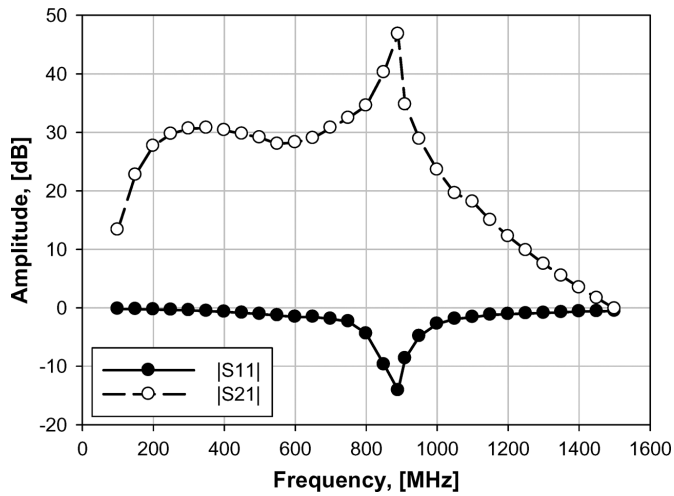

Fig. 17. Measured S-parameters of the cascaded amplifier.

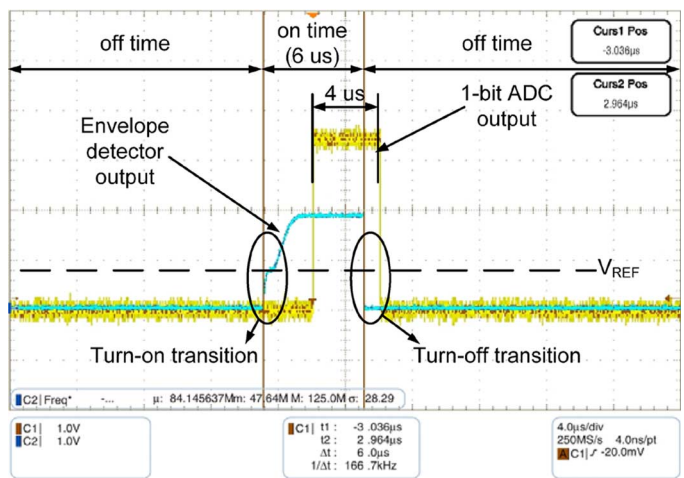

Fig. 18. Waveform of the envelope detector and the 1 bit-ADC during reception of 1bit of data.

ID modes. To achieve a BER of 0.001, the required sensitivity of the receiver is −75.8 dBm for a data rate of 1 kbps in MO mode The sensitivity decreases as the data rate increases; and the required sensitivity becomes −72 dBm for a data rate of 200 kbps. Note that, in the ID mode, the baseband blocks (envelope detector and 1-bit ADC) have less time to process the incoming data before a new bit arrives, thereby degrading the BER. Therefore, the BER increases despite the fact that the ID mode data-rate is less than the MO effective data-rate (167 kbps). The measured sensitivity is higher than the Tuned-RF receiver in [6] and almost the same as that of the un-certain IF wake-up receiver [7].

Table II compares performance of a few representative reactive wake-up receivers. It is difficult to make a fair comparison due to differences in operation and design environments such as processing technology, frequency band, sensitivity, and supply

TABLE II
COMPARISON OF PERFORMANCE FOR VARIOUS WAKE-UP RECEIVERS

	[2]	[3]	[4]	This Work
Carrier Freq. (GHz)	1.9	1.9	2	0.9
Technology	N/A	90 nm	90 nm	0.18 μm
Sensitivity (dBm)	-100.5	-50	-72	-73
Supply Current (μA)	400	130	104	4.7
Supply Voltage (V)	1.0	0.5	0.5	1.8
Power (μW)	400.0	75.0	52.0	8.5

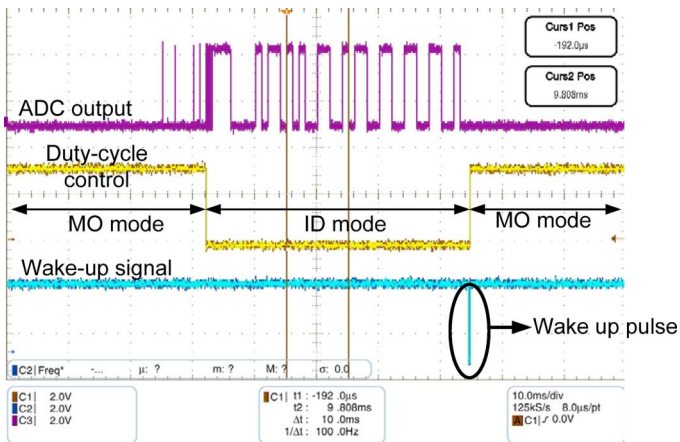

Fig. 19. Waveform showing the correct operation of the wake-up receiver.

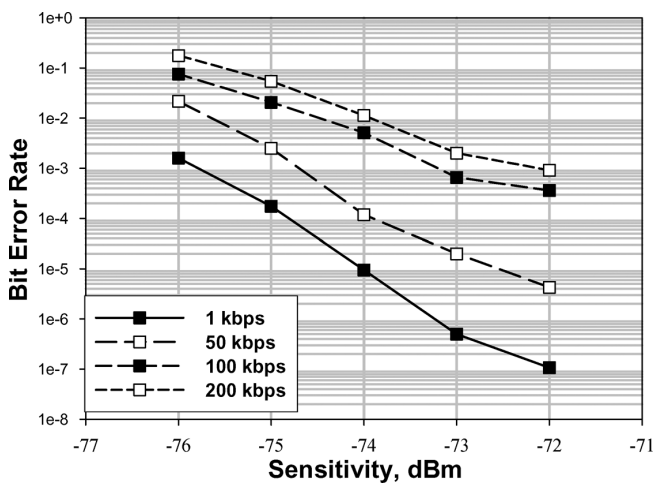

Fig. 20. BER versus the sensitivity of the wake-up receiver.

voltage. The proposed wake-up receiver and the uncertain-IF type receiver in [7] have similar sensitivity, but the proposed design dissipates about five times less power than the uncertain-IF type receiver. Finally it should be noted that the latency of the proposed receiver is about 100 times shorter than the one reported in [8].

Fig. 21 shows a microphotograph of the proposed wake-up receiver, in which the cascaded amplifier, envelope detector, and 1-bit ADC occupy the majority of the die area. The test pattern block is included to measure the turn-on/off time of the envelope detector and 1-bit ADC. The die size of the receiver is $1850 \times 1560\ \mu m^2$.

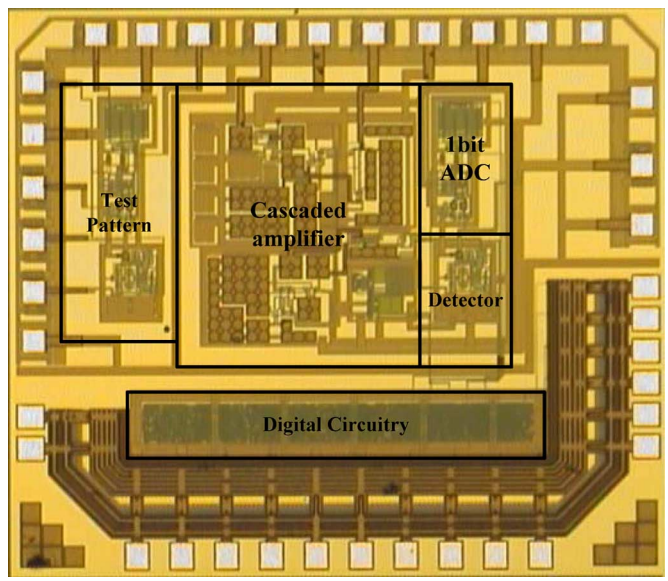

Fig. 21. Microphotograph of the proposed wake-up receiver.

VI. CONCLUSION

Duty-cycling is often utilized in order to reduce average energy and power dissipation. However, these designs often suffer from excess latency. To address this shortcoming, a new wake-up receiver system is proposed that employs two different data rates, constituting two modes of operation: MO and ID. A SFB sequence is transmitted at a low data rate of 1 kbps in the MO mode, and an aggressive bit-level duty cycle of 0.6% is applied to the wake-up receiver to reduce power consumption. Upon detection of the SFB sequence, the ID mode is asserted and the wake-up receiver operates continuously while the rest of the data packet is transmitted at a much higher data rate of 200 kbps. As a result, the average power consumption, energy consumption, and latency are reduced. The proposed wake-up receiver is designed and fabricated in a 0.18 μm CMOS technology with a core size of $1850 \times 1560\ \mu m^2$ for the target frequency range of 902–928 MHz. The measured results show that the proposed design achieves a sensitivity of -73 dBm, while dissipating an average power of 8.5 μW from 1.8 V supply.

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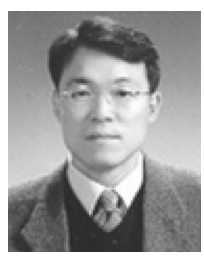

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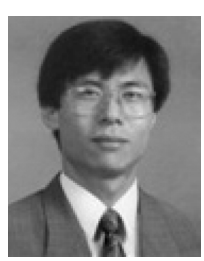

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