A Low-Noise Four-Stage Voltage-Controlled Ring Oscillator in Deep-Submicrometer CMOS Technology

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***Abstract*—This brief presents a low-voltage and low-noise ring voltage-controlled oscillator (VCO) where the phase noise performance is improved by reducing the total channel thermal noise injected into the output node of the VCO during the transition period of the output voltage swing. Implemented in a 65-nm CMOS technology, the proposed ring VCO operates from 485.7 to 1011.6 MHz. At 645 MHz, the measured phase noise is −110.8 dBc/Hz at an offset of 1 MHz while dissipating 10 mW from a 1-V supply.**

***Index Terms*—Phase noise, ring oscillator, transition period, voltage-controlled oscillator (VCO).**

I. Introduction

CMOS TECHNOLOGIES continue to be scaled down in order to lower costs, increase speeds, and achieve a higher level of integration. As a result, CMOS has flourished in wireless communication applications [1]. However, transceiver building blocks must now accommodate the shrinking supply voltage of deep-submicrometer technologies.

LC voltage-controlled oscillators (VCOs) (LC VCOs) are typically utilized in wireless transceivers due to their good phase noise performance [2]. However, LC VCOs exhibit a relatively narrow tuning range, which further decreases with the supply voltage. Furthermore, these designs also occupy a large chip area, regardless of scaling. In contrast, ring VCOs offer a wide tuning range and occupy a small chip area, and their power consumption substantially decreases with scaling. Owing to these attributes, ring VCOs are a popular candidate for implementation in scaled CMOS. Unfortunately, they exhibit poor phase noise performance. Thus, the phase noise of ring VCOs is the key issue compared to LC VCOs.

Extensive research has been carried out to analyze and improve the phase noise of ring oscillators [3]–[7]. From these works, it has been reported that the phase noise is degraded by the reduced output voltage swing and the increased channel thermal noise of the transistor in accordance with the development of CMOS technology [4]. The phase noise of the ring oscillator can be improved by maximizing the output voltage swing and minimizing the amount of noise injected during output voltage transitions [4]. The VCOs reported in [6] and [7] facilitate rail-to-rail voltage swings to achieve low phase noise. However, the noise performance of the design in [6] is limited by the delay cells, which inject a substantial amount of noise during the transition periods of the VCO. A ring VCO with good phase noise was reported in [7]. However, it suffers from an extremely narrow tuning range due to the reduced supply voltages of scaled-down CMOS technology [8]. In [8], this problem is mitigated by adopting a transmission gate. Despite an increased tuning range, the noise current injected by the transmission gate during the transition periods translates to a significant amount of phase noise. This brief focuses on reducing the amount of injected channel thermal noise of transistors during output voltage transitions while maintaining an acceptable frequency tuning range for low supply voltages.

This brief is organized as follows. Section II describes the phase noise of the ring oscillator. Section III presents the structure and the operation principles of the proposed VCO shown in Fig. 1. Section IV gives the measurement results. Section V discusses the performance of the proposed VCO in comparison with other ring VCOs in accordance with technology development. Finally, conclusions are provided in Section VI.

II. Phase Noise of Ring Oscillator

Hajimiri *et al.* [3], [4] reported that the phase noise of the ring oscillator is affected by the amount of noise injected during the transition period of the oscillator output signal, and the single-sideband phase noise spectrum due to a white-noise current source is given by

$$L\{f_{off}\} = \frac{\Gamma_{rms}^2}{8\pi^2 f_{off}^2} \cdot \frac{\bar{i_n}^2/\Delta f}{q_{max}^2} \tag{1}$$

where Γ_{rms}^2 is the rms value of the impulse sensitivity function (ISF); an approximate ISF for the ring oscillator is shown in Fig. 2 [4]. $\bar{i_n^2}/\Delta f$ is the single-sideband power spectral density of the noise current source and f_{off} is the frequency offset from the carrier. In the case of multiple noise sources injected into the same node of the delay cell, $\bar{i_n^2}/\Delta f$ represents the total current noise due to all sources and is given by the sum of individual

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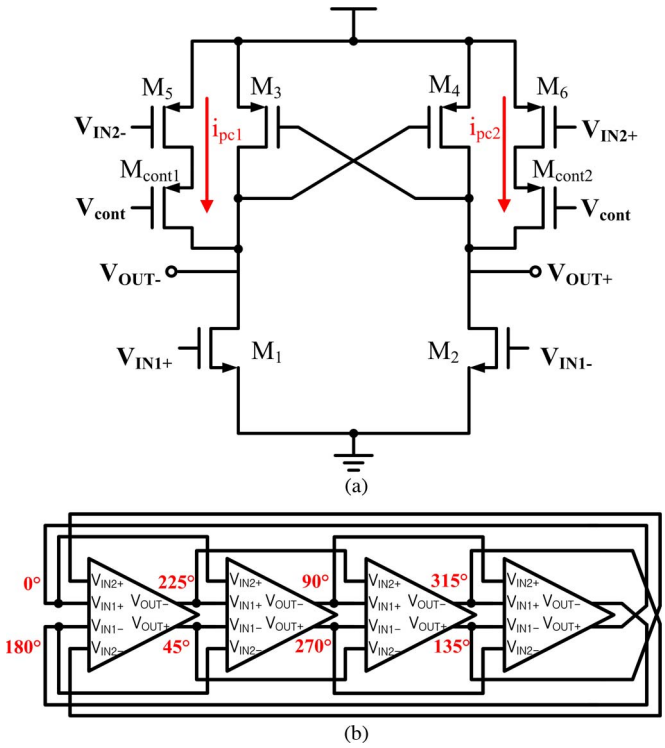

Fig. 1. Proposed (a) delay cell and (b) four-stage ring oscillator.

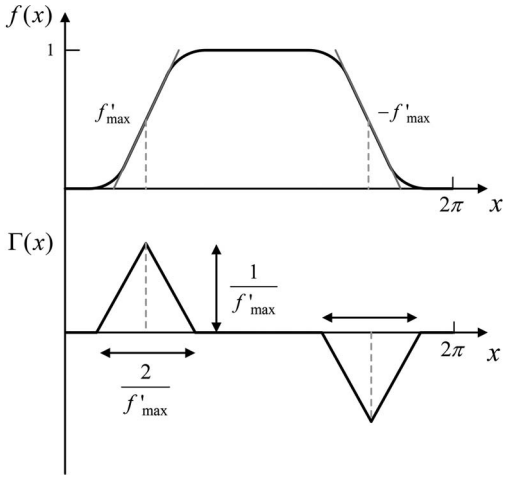

Fig. 2. Approximate waveform and ISF for ring oscillator.

noise power spectral densities [4]. According to (1), the phase noise can be improved by fast transition, increasing the output voltage swing, and reduction of the current noise sources during transitions. This brief focuses on the last approach, reducing the total current noise injected during the transition period in order to improve the phase noise.

III. Low-Noise Ring VCO Design

Fig. 1 shows the schematic of the proposed delay cell along with the corresponding four-stage ring oscillator. From Fig. 1(a), the delay cell consists of the NMOS input transistors (M_1, M_2), the cross-coupled PMOS transistors (M_3, M_4), the PMOS input transistors (M_5, M_6), and the PMOS control transistors (M_{cont1}, M_{cont2}) that are adopted to change the oscillation frequency by varying the control voltage V_{cont}. Fig. 1(b) shows the proposed four-stage ring VCO, which provides eight different phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). V_{IN1+} and V_{IN1-} represent the differential voltage that is applied to the NMOS input transistors M_1 and M_2, and V_{OUT-} and V_{OUT+} constitute the differential output voltage of the delay cell. Due to the oscillation condition of the four-stage structure, the phase difference between the input (V_{IN1+}, V_{IN1-}) and output (V_{OUT-}, V_{OUT+}) is 225°. V_{IN2-} and V_{IN2+} are applied to the PMOS input transistors M_5 and M_6, respectively. As V_{IN2-} and V_{IN2+} are taken from a delay cell that is two stages away from the corresponding delay cell,V_{IN2-} and V_{IN2+} come 45° earlier in phase than V_{IN1+} and V_{IN1-} [7]. The proposed VCO adopts the negative skewed delay scheme reported in [7] for fast transition as a method to improve the phase noise.

To illustrate how the phase noise is reduced in the proposed design, the time-domain operation of the proposed ring oscillator is now analyzed. Since each stage is identical, it is sufficient to examine a single delay cell over one oscillation period. The analysis is further simplified by only considering the half circuit of the proposed delay cell. This is easily justified since the goal of the analysis is to show the reduced conduction time during the transition periods of the oscillator, and both halves of the circuit ideally behave in the same manner.

Fig. 3 depicts the half-circuit waveforms of a single delay cell in the proposed design. Fig. 3(a) shows the input voltage V_{IN1+}, while V_{OUT-}, V_{IN2-}, and V_{OUT+} are given in Fig. 3(b). Fig. 3(c) shows the current i_{pc1} flowing through M_{cont1} in the proposed delay cell. Fig. 3(d) illustrates the behavior of the proposed delay cell through one oscillation period. Consequently, the delay circuit exhibits three regions of operation, which are now considered in detail.

In region I, V_{IN1+} and V_{OUT+} are low while V_{OUT-} remains high. This region of operation continues until a low–high transition of V_{IN2-} occurs, thereby changing V_{IN2-} to approximately $V_{DD-}|V_{th,p}|$. As illustrated in Fig. 3(d), M_1 is in the OFF state while all the PMOS transistors (M_3, M_5, M_{cont1}) are on. In this region, the device noise power spectral density is given by

$$\frac{\bar{i_n^2}}{\Delta f} = 4KT\gamma(g_{mp3} + g_{mpcont1}) \tag{2}$$

where g_{mp3} and $g_{mpcont1}$ are the transconductances of transistors M_3 and M_{cont1}, respectively. γ is the noise multiplication factor, which is more significant for a short-channel transistor. In this region, the phase noise is negligible since the output voltage remains near the supply rail [4].

In region II, V_{IN1+} and V_{OUT+} experience a low–high transition while V_{OUT-} undergoes a high–low transition. During the transition of V_{OUT-}, the phase noise is affected by the noise current of only two transistors, M_1 and M_3. In the proposed delay cell, i_{pc1} flowing through M_5 and M_{cont1} can be eliminated by turning off M_5 since V_{IN2-} is higher than $V_{DD-}|V_{th,p}|$ in this region. During the high–low transition of

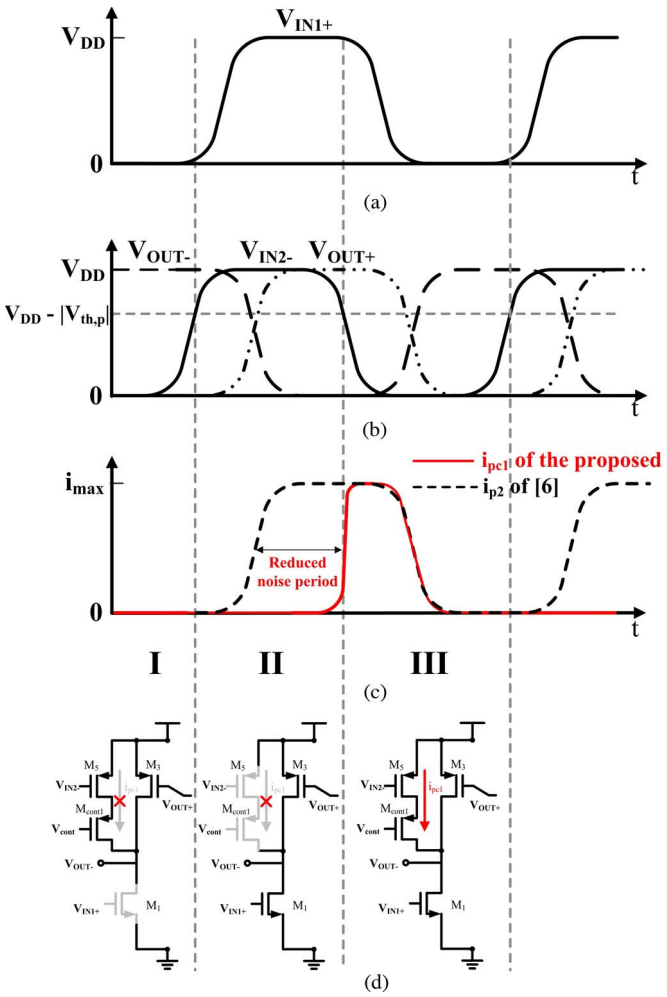

Fig. 3. Half-circuit waveforms of (a) V_{IN1+}, (b) V_{out-}, V_{IN2-}, (c) i_{pc1} and i_{p2}, and (d) half circuit of the proposed delay cell.

the output voltage V_{OUT-}, the device noise power spectral density is given by

$$\frac{\bar{i_n^2}}{\Delta f} = 4KT\gamma(g_{mp3} + g_{mn1}) \tag{3}$$

where g_{mn1} is the transconductance of transistor M_1. In (3), there is no noise current from M_{cont1} since the transistor is off during the high–low transition of V_{OUT-}. As a result, the phase noise does not suffer from noise current by M_{cont1} at the output in this region.

In region III, V_{IN1+} and V_{OUT+} change from high to low while V_{OUT-} undergoes a low–high transition. In this region, V_{IN2-} is at a lower voltage than $V_{DD-}|V_{th,p}|$, and thus, both M_5 and M_{cont1} turn on; hence, i_{pc1} and the accompanying channel noise are observed. However, i_{pc1} is terminated as soon as V_{OUT-} reaches V_{DD}. During the low–high transition of V_{OUT-}, the device noise power spectral density is given by

$$\frac{\bar{i_n^2}}{\Delta f} = 4KT\gamma(g_{mp3} + g_{mpcont1} + g_{mn1}). \tag{4}$$

Thus, the phase noise is dominantly affected during the low–high transition of V_{OUT-}, which occurs in region III,

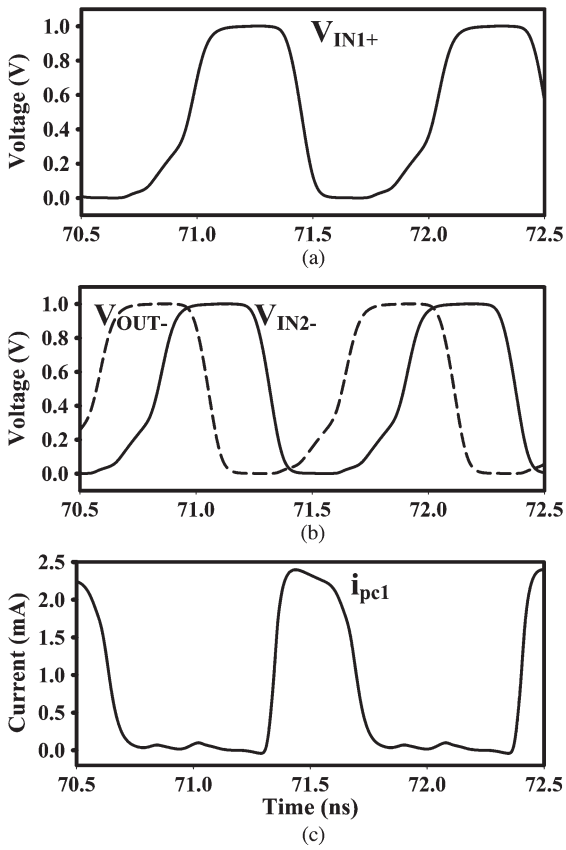

Fig. 4. Simulated waveforms. (a) V_{IN1+}, (b) V_{out-} and V_{IN2-}, and (c) i_{pc1}.

because all noise sources appear in this region. The same operation can be applied to the other half circuit.

In summary, the proposed ring oscillator can alleviate much of the phase noise contributed by the channel thermal noise of M_{cont1} by turning off M_5 and M_{cont1} in region II. Fig. 3(c) shows i_{p2}, which corresponds to the current through the frequency control transistors of the design reported in [6], plotted against i_{pc1} of the proposed oscillator. As can be seen in Fig. 3(c), i_{p2} of [6] appeared over the entire two transitions (low–high and high–low), but the frequency control current of the proposed delay cell (i_{pc1}) only appeared during one transition period (low–high). As a result, the phase noise performance is improved in the proposed architecture. Fig. 4 represents the simulation results of the proposed structure to verify the discussed waveforms (V_{IN1+}, V_{out-}, V_{IN2-}, and i_{pc1}) in Fig. 3. The simulation results shown in Fig. 4 are similar to that in Fig. 3, and i_{pc1} is eliminated during the high–low transition of the output voltage. Thus, the phase noise of the proposed VCO is improved by eliminating the noise current of $M_{cont1,2}$ during the high–low transition as well as by achieving the fast transition by a negative skewed delay scheme [7] and PMOS latch.

Fig. 5 shows the simulated phase noise performance in comparison with other ring VCO architectures reported in [6], [7], and [10] for the same process, supply voltage, center frequency (645 MHz), and power dissipation (11 mW). The proposed VCO achieves the lowest phase noise performance among the simulated VCOs; the phase noise of the proposed VCO is 6.6,

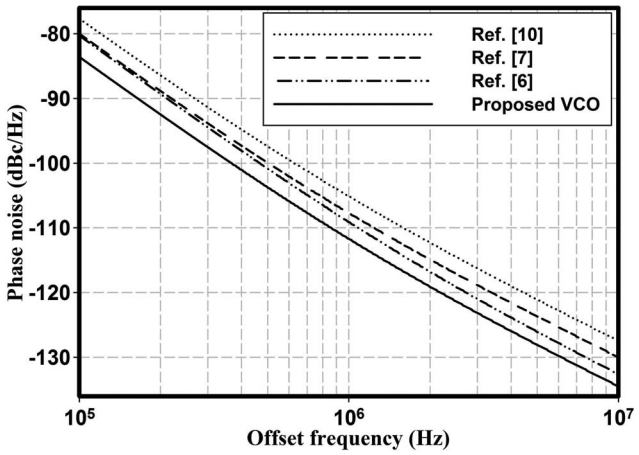

Fig. 5. Simulated phase noise performance in comparison with other ring VCOs.

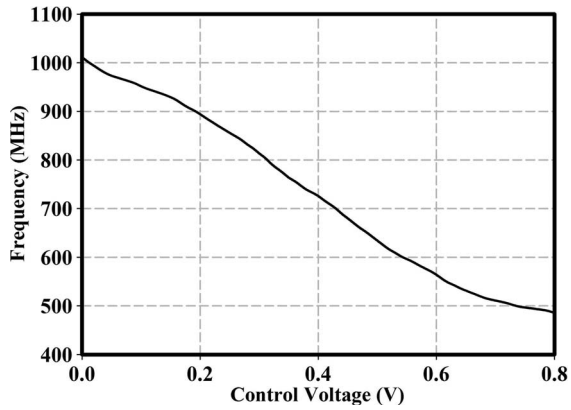

Fig. 6. Measured oscillation frequency of the proposed VCO versus the control voltage.

4, and 2.6 dB lower at a 1-MHz offset frequency than those of [6], [7], and [10], respectively.

The oscillation frequency is tuned by i_{pc1}, which is changed according to the control voltage (V_{cont}), because the charging time of the output capacitor is affected by i_{pc1}. If the gate voltage V_{cont} of M_{cont1} is increased, the current i_{pc1} is decreased, and the output capacitor is charged slowly. Thus, the charging time is increased, and the oscillation frequency is decreased. Therefore, the oscillation frequency can be changed by V_{cont}. Furthermore, the proposed VCO achieves a wider frequency tuning range than [6] because higher oscillation frequency is achieved by adopting the dual-delay scheme of [7]. The proposed ring oscillator is limited by the characteristic that the delay cell can be used as a four-stage oscillator in order to maximize the effect of the phase noise improvement. This may not, however, be a critical issue, as a four-stage ring oscillator has been widely used.

IV. Measurement Results

The proposed ring VCO is fabricated in a 65-nm CMOS technology. The oscillation frequency range is measured from 485.7 to 1011.6 MHz over a control voltage from 0.8 to 0 V, as shown in Fig. 6. Fig. 7 shows the measured phase noise and the

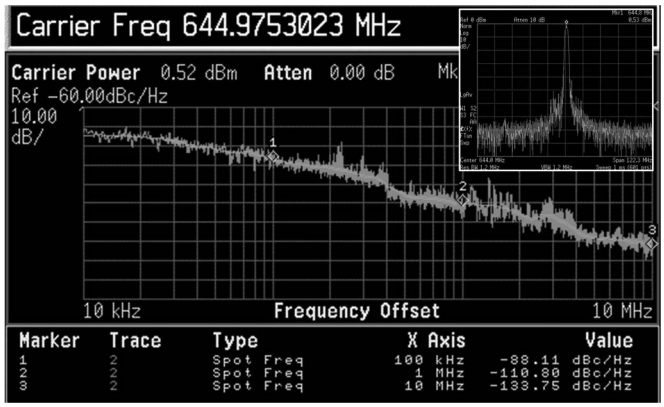

Fig. 7. Measured phase noise and output spectrum.

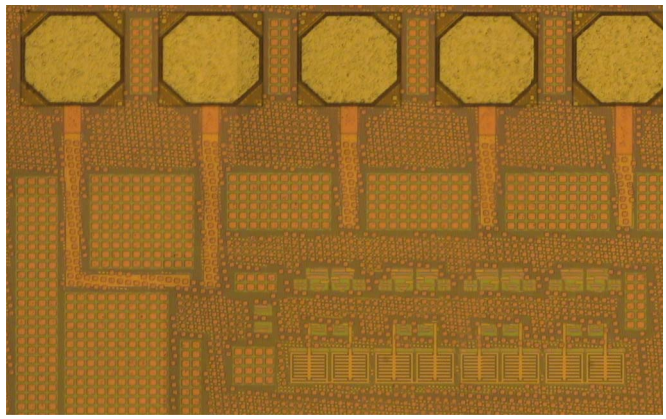

Fig. 8. Microphotograph of the proposed VCO.

output spectrum. The measured phase noise is -110.8 dBc/Hz at a 1-MHz offset while oscillating at 645 MHz and dissipating 10 mA at a 1-V supply. An approximately 0-dBm output power is measured at the buffer output. The open-drain common-source topology using the off-chip inductor is adopted as the output buffer of the proposed ring VCO. Fig. 8 shows a microphotograph of the fabricated VCO. The chip area without the pads is $230 \times 98\ \mu m^2$.

Table I summarizes the measurement results of the proposed VCO and prior works. In order to provide a fair comparison with other reported works at different center frequencies and power consumptions, a Figure-of-Merit (FoM), as defined hereinafter, is used:

$$FoM = L\{f_{off}\} - 20\log\left(\frac{f_{osc}}{f_{off}}\right) + 10\log\left(\frac{P_{diss}}{1\,\mathrm{mW}}\right) \quad (5)$$

where $L\{f_{off}\}$ is the phase noise from the oscillation frequency (f_{osc}) at the offset of f_{off} and P_{diss} is the power consumption of the VCO.

V. Discussion

As shown in Table I, [6]–[9] and [11] were implemented in 500-, 600-, 180-, 180-, and 180-nm CMOS technologies, respectively. The delay cells of [7] was used in [9] and [11] as well. Eken and Uyemura [11] report a high oscillation frequency of 5.9 GHz with good phase noise performance. However, the FoM cannot be estimated to compare with other

TABLE I
PERFORMANCE COMPARISON WITH OTHER VCOs

Ref.	Process (nm)	Supply (V)	P_{diss} (mW)	f_{osc} (MHz)	Phase Noise@1MHz (dBc/Hz)	FoM (dBc/Hz)
[6]	500	2.5	15.4	900	-105.5@600KHz	-157.1
[7]	600	3	30	900	-117@600KHz	-165.7
[8]	180	2	22	630	-108	-150.6
[9]	180	1.8	13	1861	-102	-156.3
[11]	180	1.8	N.A	1810 / 5790	-105.5(by measurement) / -99.5(by simulation)	-
This Work	65	1	10	645	-110.8	-157

ring VCOs in Table I because the power dissipation was not reported. In Table I, it can be seen that the FoMs of [6] and [7] are better than those of [8] and [9] because the phase noise of the short-channel oscillator is larger than that of the long-channel case at the same center frequency and power consumption due to the larger γ of the short-channel transistor as reported in [4]. Although the channel lengths of [8] and [9] are the same, the FoM of [9] is better than that of [8] because the delay cell of [9] was used with the low-noise delay cell of [7]. As discussed in Section I, however, the delay cell of [7] suffers from a narrow tuning range at a low supply voltage. In the case of [9], the frequency tuning range is only 8.13% under a tuning voltage of 1.6 V. If the supply voltage continues to be reduced with the development of CMOS technology, the frequency tuning range would be narrower, and the delay cell of [7] will be difficult to be used in wideband applications. Thus, new low-noise delay cells are required for an acceptable frequency tuning range at a low supply voltage. In spite of the low supply voltage and the short-channel technology whose phase noise performance is inferior, the proposed VCO shows a frequency tuning range of about 70% with a tuning voltage of 0.8 V and a FoM of -157 dBc/Hz, which is similar to that of [6] and is 6.4 and 0.7 dB better than those of [8] and [9], respectively. Therefore, the proposed VCO can be used as a low-noise ring VCO for low supply voltage and scaled-down technology.

VI. CONCLUSION

A low-noise ring VCO is proposed as a suitable structure in deep-submicrometer CMOS technology. The phase noise is improved by eliminating the noise currents that are added for frequency tuning during the output high–low transition. The VCO is implemented in a 65-nm CMOS technology. The measured frequency tuning range is from 485.7 to 1011.6 MHz (about 70%). At 645 MHz, the measured phase noise is -110.8 dBc/Hz at a 1-MHz offset frequency while dissipating 10 mA at a 1-V supply. The FoM of the proposed VCO is -157 dBc/Hz. The proposed VCO can be used as a low-noise ring VCO for low supply voltage and scaled-down technology.

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