A CMOS Wideband Highly Linear Low-Noise Amplifier for Digital TV Applications

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***Abstract*—This paper presents a highly linear wideband differential low-noise amplifier (LNA) for digital TV applications. The proposed LNA is a modified version of the wideband LNA reported by Bruccoleri *et al.* in 2004. In order to increase the linearity of Bruccoleri *et al.*'s LNA, the Volterra series is adopted to identify the nonlinear components and the noise-cancelling circuit is modified to eliminate the whole nonlinear components. Implemented in 0.13-μm CMOS technology, the proposed wideband LNA has a gain of 12.4 dB and a noise figure of 1.6 dB, as determined from measurements, while drawing 18.45 mA from a 1.2-V supply. The proposed LNA has an IIP_3 of 16.6 dBm with 6-MHz frequency offset at 100 MHz, far exceeding the values of existing wideband LNAs.**

***Index Terms*—Common source (CS), distortion cancellation, low-noise amplifier (LNA), noise cancelling, resistive shunt feedback, third-order input-referred intercept point (IIP_3), Volterra series analysis, wideband.**

I. Introduction

THE DIGITAL TV (D-TV) market has recently experienced substantial growth due to the rapid transition from analog to digital television broadcasting. In step with this change, there has been much effort to fully integrate D-TV receivers into a single CMOS chip that can cover the entire D-TV band for both terrestrial and cable TV broadcasting. However, stringent specifications of the D-TV standard present a number of design challenges. A D-TV receiver for both terrestrial and cable broadcasting should cover a wide frequency band from 50 to 860 MHz. Terrestrial broadcasting experiences large variations of the input signal power, and cable TVs should accommodate about 130 closely spaced channels. As a result, a D-TV receiver requires high sensitivity and linearity, a wide dynamic range, and good adjacent channel rejection characteristics [2]–[4].

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The performance of a D-TV receiver is sensitive to the low-noise amplifier (LNA) characteristics. A wideband LNA should simultaneously have high linearity, a low noise figure (NF), and a wide dynamic range, thus presenting a significant design challenge. Bruccoleri *et al.* [1] proposed a wideband LNA (referred to as Bruccoleri's LNA hereafter) that reduces the NF by adopting a noise-cancelling technique, which is shown to be quite effective. Bruccoleri's LNA achieves a low NF of 2 dB and a moderate gain of 13.7 dB over a frequency range from 2 to 1600 MHz. The major shortcomings of Bruccoleri's LNA are poor linearity and high power consumption. Since the introduction of the noise-cancelling technique for Bruccoleri's LNA, most wideband LNAs have adopted variations of this technique [5]–[13].

The linearity characteristic of an LNA is an important design consideration for D-TV applications and is expressed in terms of the input second- and third-order intercept points (IIP_2 and IIP_3). Since, a differential architecture ensures high IIP_2, IIP_2 is typically not a major design concern. A commonly adopted approach to improve IIP_3 in narrowband LNAs is cancelling of the third-order nonlinear components of the amplifying transistor(s) [14]–[22]. Ding and Harjani proposed a third-order component-cancelling technique wherein an auxiliary transistor that operates in weak inversion is adopted, and the drain current is combined with the main amplifying transistor [14]. Ding and Harjani reported a narrowband IIP_3 of 18 dBm at the cost of a slightly increased NF. Other LNA designs reported in [15]–[22] took the same approach, in principle, although the actual circuits are different.

Ding and Harjani's approach is effective for narrowband applications, but insufficient for wideband LNAs, which are typically composed of two amplifying stages to satisfy wideband input matching and noise cancellation. To achieve a high IIP_3 and low NF at the same time, it is necessary to cancel out the nonlinear components of both the input matching and the noise-cancellation stages. The cancellation mandates the identification of all sources of third-order intermodulation (IM3) products at the output node, and a scheme should then be adopted to cancel the nonlinear components.

Chen *et al.* [7] (referred to as Chen's LNA hereafter) applied a Volterra series to analyze the nonlinear components of their wideband LNA. Based on a Volterra-series analysis, they adopted a complementary common-gate topology, where the nMOS and pMOS transistor outputs are combined through a capacitor to cancel out the second-order nonlinear components, the dominant components that determine the IIP_3 of their topology. Chen's LNA achieves a far better IIP_3 of around

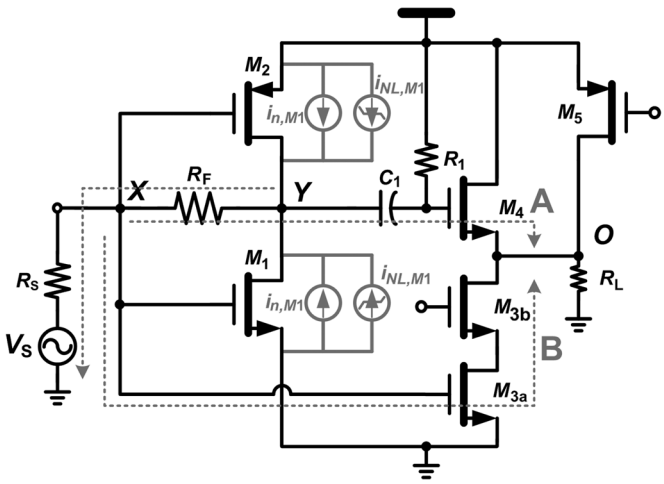

Fig. 1. Bruccoleri's LNA with noise-cancelling technique [1].

16 dBm compared to other wideband LNAs, with similar gain and NF. However, the IIP_3 of Chen's LNA decreases to around 0 dBm for a two-tone frequency offset of 10 MHz or narrower, as the size of the coupling capacitance determines the amount of low-frequency second-order nonlinear components. A larger capacitor can be more effective for a smaller spacing of the two tones, but the size of the capacitor becomes impractical. As a compromise, they adopted a 15-pF coupling capacitor, which makes the proposed linearization technique ineffective for the required two-tone spacing of 6 MHz in D-TV systems.

As noted earlier, Bruccoleri's LNA achieves low noise over a wide range of frequency, and hence, is suitable for D-TV applications. The key shortcoming of Bruccoleri's LNA is poor linearity. While Chen's LNA has a rather high IIP_3, it varies over the two-tone spacing. This paper reports the design details of a wideband LNA that resolves the linearity problem of Bruccoleri's LNA based on a Volterra-series analysis.

The remainder of this paper is organized as follows. Section II briefly overviews two relevant existing noise and nonlinear components cancellation methods presented in [1] and their respective limitations. Section III describes the behavior of the proposed fully differential wideband LNA through theoretical analysis and simulation studies. Section III also introduces the LNA design including the effect of bond wires and PVT variations for robustness. Section IV introduces measurement results of the proposed LNA, and Section V concludes.

II. Background of Bruccoleri's LNA

Fig. 1 shows the circuit schematic of Bruccoleri's LNA [1]. In Fig. 1, the matching stage (M_1, M_2, and R_F) of the LNA adopts a complementary resistive shunt feedback amplifier for higher transconductance and wideband input matching. The noise-cancelling stage (M_{3a}, M_{3b}, and M_4) is configured to cancel the noise signals of M_1 and M_2 while amplifying the wanted signal. pMOS M_5 is adopted parallel with nMOS M_4 for supplying the current to increase dc bias of output node.

The noise signal induced by the transistors M_1 and M_2, $i_{n,M1}$ and $i_{n,M2}$, flows from nodes Y to X and the noise voltages at both nodes can be given by

$$V_{X,n} = R_S \cdot (i_{n,M1} + i_{n,M2}) \tag{1}$$

$$V_{Y,n} = (R_F + R_S) \cdot (i_{n,M1} + i_{n,M2}). \tag{2}$$

These noise voltages are transferred to output node through M_3 and M_4, and can be cancelled out upon satisfaction of the following condition [1]:

$$\frac{R_F + R_S}{R_S} = \frac{g_{m3a}}{g_{m4}} \tag{3}$$

where R_F is the feedback resistance, R_S is the input signal source resistance, and g_{m3} and g_{m4} are the transconductances of M_3 and M_4, respectively.

Similarly, the nonlinear components of the matching stage can also be cancelled [1]. In Fig. 1, the nonlinear currents of M_1 and M_2, $i_{\mathrm{NL},M1}$ and $i_{\mathrm{NL},M2}$, flows from nodes Y to X like the noise currents and induce nonlinear voltages, which can be given by

$$V_{X,\mathrm{NL}} = R_S \cdot (i_{\mathrm{NL},M1} + i_{\mathrm{NL},M2}) \tag{4}$$

$$V_{Y,\mathrm{NL}} = (R_F + R_S) \cdot (i_{\mathrm{NL},M1} + i_{\mathrm{NL},M2}) \tag{5}$$

where $i_{\mathrm{NL},M1}$ and $i_{\mathrm{NL},M2}$ represent the nonlinear currents of M_1 and M_2. These nonlinear voltages are also expected to be cancelled out at the output node of the LNA upon satisfaction of (3) [1]. However, the measured IIP_3 of Bruccoleri's LNA is 0 dBm and it can be explained below.

In Fig. 1, the input signal travels through two different paths (paths A and B) to be combined at the output node. Path A involves M_1, M_2, and M_4, while path B involves M_{3a} and M_{3b}. Therefore, the nonlinear terms of g_m of M_1, M_2, M_{3a} and M_4 are expected to contribute to the linearity of the given circuit. However, Bruccoleri's LNA is designed to cancel the noise signal and the nonlinear components of M_1 and M_2 only.

In Fig. 1, the ratio of R_F/R_S should be large enough to achieve a high gain so that the noise contribution of the second stage will be small. To satisfy a large value of R_F/R_S and the noise-cancelling condition given in (3), a large ratio of $(W/L)_{M3a}/(W/L)_{M4}$ is required. In Fig. 1, M_1 and M_{3a} share the same gate–source voltage. Considering the limited amount of drain current in M_{3a}, the size of M_4 has to be quite small. This can mandate a large value of $V_{\mathrm{gs},M4}$, which tends to drive M_{3a} into triode region operation. For compensation, current source M_5 is connected with M_4 in parallel for supplying the current.

III. Proposed Low-Noise Highly Linear Wideband LNA

Fig. 2(a) and (b) shows the circuit schematic of the proposed LNA single-ended half-circuit and differential full-circuit, respectively. In Fig. 2(a), the circuit schematic is the same as that of Bruccoleri's LNA, except for removing cascode transistor M_{3b} for low supply voltage and connecting the gate of M_3 to

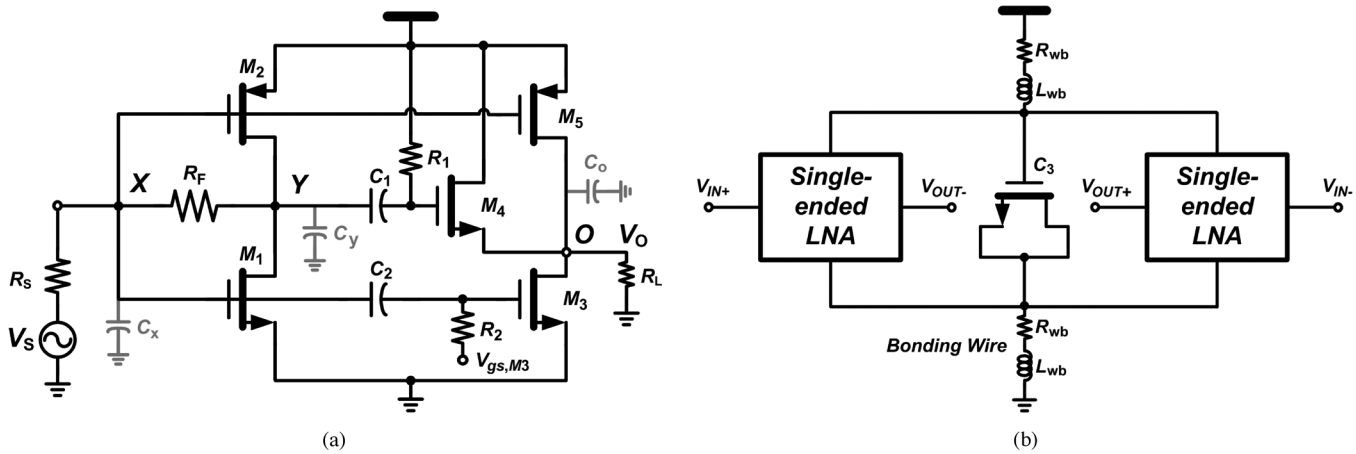

Fig. 2. Circuit schematic of the proposed LNA. (a) Single-ended half-circuit. (b) Differential full-circuit.

the input with a blocking capacitor C_2, where the gate of M_5 is also connected at the input.

The input impedance of the proposed differential LNA, shown Fig. 2(b), is given by [1]

$$Z_{\text{in}} = 2 \cdot \frac{R_F + (r_{o1} \| r_{o2})}{1 + (g_{m1} + g_{m2}) \cdot (r_{o1} \| r_{o2})} \tag{6}$$

where r_{o1} and r_{o2} are the intrinsic output resistances of M_1 and M_2, respectively. As R_F is much smaller than r_o, the input impedance is approximately equal to $2/(g_{m1} + g_{m2})$.

In Fig. 2(a), M_5 and M_3 together form a complementary common source amplifier, which leads to higher transconductance compared to that of Bruccoleri's LNA. In Fig. 2(a), the noise-cancelling condition for M_1 and M_2 can still be achieved by satisfying

$$\frac{R_F + R_S}{R_S} = \frac{g_{m3} + g_{m5}}{g_{m4}}. \tag{7}$$

By the addition of g_{m5} in (7), the required ratio of $((W/L)_{M_3}/(W/L)_{M_4})$ in Fig. 2(a) can be reduced compared to that of Bruccoleri's LNA. Therefore, power consumption of the noise-cancelling stage could be reduced and output dc bias will be increased. With removing cascode transistor (M_{3b}), this allows M_3 to operate in a deeper saturation region compared to the case of Bruccoleri's LNA, which would improve the linearity.

A. Noise Analysis

The noise characteristic of the proposed LNA is similar to that of Bruccoleri's LNA [1], except that M_3 is replaced with $M_3 + M_5$ as a complementary transistor. The noise factor of the proposed LNA can be given by

$$F = 1 + \frac{\frac{\gamma}{\alpha}(g_{m3}+g_{m4}+g_{m5})}{R_S G^2} + \frac{R_F g_{m4}^2}{R_S G^2} + \frac{\frac{\gamma}{\alpha}(g_{m1}+g_{m2})}{R_S G^2}\left((R_F+R_S)g_{m4} - R_S(g_{m3}+g_{m5})\right)^2 \tag{8}$$

where γ is the noise parameter of the MOSFET, $\alpha = g_m/g_{d0}$ and the total transconductance gain G of the proposed LNA is given by

$$G = g_{m4}\left(1 - (g_{m1} + g_{m2})R_F\right) - (g_{m3} + g_{m5}). \tag{9}$$

Under the noise-cancelling condition that satisfies (7) and the matching condition of $(g_{m1} + g_{m2} = 1/R_S)$, (8) becomes

$$F = 1 + \frac{\frac{\gamma}{\alpha}}{(g_{m3} + g_{m5})}\left(\frac{1}{R_S} + \frac{3}{R_F} + \frac{2R_S}{R_F^2}\right) + \frac{R_S}{R_F}. \tag{10}$$

The noise factor shown in (10) is almost the same as that of Bruccoleri's LNA, except that g_{m3} is replaced with $g_{m3} + g_{m5}$. In (10), for the given values of R_F and R_S, higher values of $g_{m3} + g_{m5}$ lead to lower values of NF. Compare to Bruccoleri's LNA, for the given amount of power dissipation, g_{m5} is obtained with no additional power dissipation in the proposed LNA. In addition, the noise contribution of M_5 as a current source is not included in the NF expression in [1]. Therefore, the NF of the proposed LNA is expected to be better than that of the Bruccoleri's LNA.

B. Nonlinear Analysis

In general, the nonlinear characteristics of a MOSFET are mainly caused by the nonlinearities in transconductance g_m and drain conductance g_{ds}. Usually, the nonlinearities of drain conductance are relatively insignificant and can be ignored. For a small-signal operation, the drain current of a NMOSFET considering the nonlinearities can be expressed as

$$i_{\text{ds}} = g_m v_{\text{gs}} + \frac{g'_m}{2!} v_{\text{gs}}^2 + \frac{g''_m}{3!} v_{\text{gs}}^3 + \cdots \tag{11}$$

where g_m represents the small-signal transconductance as a first-order term, and g'_m and g''_m as second- and third-order nonlinear terms. The same can be applied for a PMOSFET, except that the gate–source voltage is given by v_{sg}.

Fig. 3 shows a schematic and mathematical model of how the IM3 components at the LNA output are determined by the combinations of the first-, second-, and third-order current components of active devices following the signal flow. Fig. 3(b)

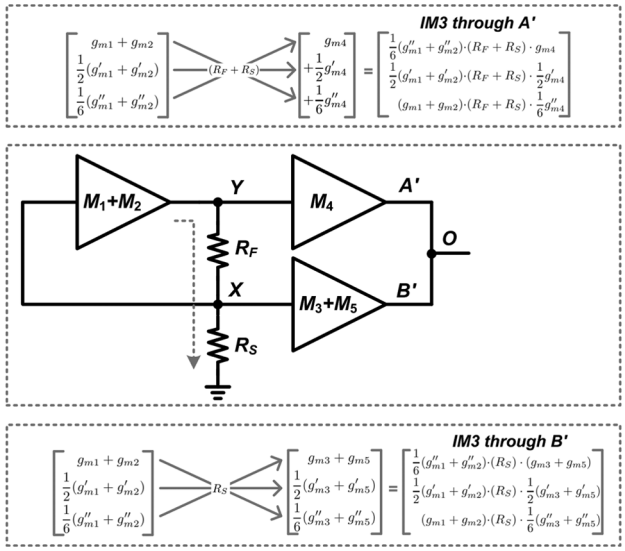

Fig. 3. Schematic and mathematical model of how the IM3 components at the LNA output are determined by the combinations of the first-, second-, and third-order current components of active devices following the signal flow.

shows the equivalent circuit model of the proposed LNA to analyze the nonlinear characteristic. Fig. 3(a) shows how the final IM3 current components appear at the A' branch, where the first-, second-, and third-order current components of M_1 and M_2 convert into a voltage signal by meeting $R_F + R_S$, and are then multiplied with the third-, second-, and first-order current components of M_4, respectively. Similarly, Fig. 3(c) shows how the final IM3 current components appear at the B' branch, where the first-, second-, and third-order current components of M_1 and M_2 convert into a voltage signal by meeting R_S, and are then multiplied with the third-, second-, and first-order current components of $M_3 + M_5$, respectively. Fig. 3 demonstrates that the IM3 components of the proposed LNA are determined by the combinations of the first-, second-, and third-order current components of the transistors in matching and noise-cancelling stages.

For more detailed analysis in this work, a Volterra series is applied to identify the nonlinear component combinations of all transistors at nodes X, Y, and O of the LNA shown in Fig. 2(a) since the Volterra series is more suitable than the Taylor series to figure out the nonlinear components combinations at a glance. The Volterra series considering up to the third-order nonlinear components at each node can be expressed as

$$V_x = A_1(s_1) \circ V_S + A_2(s_1, s_2) \circ V_S^2 + A_3(s_1, s_2, s_3) \circ V_S^3 \quad (12)$$

$$V_y = B_1(s_1) \circ V_S + B_2(s_1, s_2) \circ V_S^2 + B_3(s_1, s_2, s_3) \circ V_S^3 \quad (13)$$

$$V_o = C_1(s_1) \circ V_S + C_2(s_1, s_2) \circ V_S^2 + C_3(s_1, s_2, s_3) \circ V_S^3 \quad (14)$$

where V_S is the input voltage and $A_i(s_i)$, $B_i(s_i)$, and $C_i(s_i)$ denote Volterra kernels (coefficients) at V_x, V_y, and V_o, respectively, and $s_i = 1, 2, 3$ represents the operating frequency. All the Volterra kernels in (12)–(14) can be obtained by applying Kirchhoff's circuit law (KCL) at nodes X, Y, and O, respectively (see the Appendix).

Among the Volterra kernels, the nonlinear factors contained in the third-order nonlinear term leads to IIP_3 degradation. The third-order kernel of the output node, $C_3(s_1, s_2, s_3)$, can be given by

$$\begin{aligned} C_3(s_1, s_2, s_3) &= \Big(-(g_{m3} + g_{m5}) A_3(s_1, s_2, s_3) + g_{m4} B_3(s_1, s_2, s_3) \\ &\quad + \frac{1}{2}\left(g'_{m3} + g'_{m5}\right) A_1(s_1) \overline{A_2(s_2, s_3)} \\ &\quad + \frac{1}{2} g'_{m4} B_1(s_1) \overline{B_2(s_2, s_3)} \\ &\quad - \frac{1}{6}\left(g''_{m3} + g''_{m5}\right) A_1(s_1) A_1(s_2) A_1(s_3) \\ &\quad + \frac{1}{6} g''_{m4} B_1(s_1) B_1(s_2) B_1(s_3) \Big) \\ &\quad \times \left(r_{o3} \| r_{o4} \| r_{o5} \| Z_L(s_1 + s_2 + s_3)\right) \end{aligned} \quad (15)$$

where the details of derivatives are described in the Appendix. A smaller value of $C_3(s_1, s_2, s_3)$ would lead to smaller IM3 products, and hence, a higher IIP_3. In (15), the Volterra kernel $C_3(s_1, s_2, s_3)$ contains six terms inside the brackets, and the sum of the six terms should be minimized to maximize the IIP_3. The first two terms include g_{m3}, g_{m4} and g_{m5}, and the third-order nonlinear components of M_1 and M_2 embedded within $A_3(s_1, s_2, s_3)$ and $B_3(s_1, s_2, s_3)$, respectively. [Refer to the Appendix for the expression of $A_3(s_1, s_2, s_3)$ and $B_3(s_1, s_2, s_3)$.] As explained in Section II, the nonlinear components associated with M_1 and M_2 of the proposed LNA are cancelled upon meeting condition (7). Therefore, the first and second terms in (15) can be negligible. In (15), the fourth and sixth terms, terms multiplied by g'_{m4} and g''_{m4}, respectively, contain the nonlinear component of M_4. However, considering the buffer role of M_4 with high dc gate–source voltage, these two terms can be neglected, as g'_{m4} and g''_{m4} are expected to be small. Now, the remaining two terms, the third and the fifth terms, will be small if the nonlinear terms of M_3 and M_5 can cancel out each other; i.e., $g'_{m3} + g'_{m5} = 0$ and $g''_{m3} + g''_{m5} = 0$. Since M_3 is nMOS and M_5 pMOS, the signs of $g'_{m3} + g'_{m5}$ and $g''_{m3} + g''_{m5}$ are opposite, respectively, opening the possibility of cancellation. However, both $g'_{m3} + g'_{m5} = 0$ and $g''_{m3} + g''_{m5} = 0$ cannot be satisfied simultaneously [21]. Fortunately, in (15), $g'_{m3} + g'_{m5}$ is multiplied with $A_2(s_2, s_3)$, which is given by

$$A_2(s_2, s_3) = \frac{B_2(s_2, s_3)}{\left(1 + \frac{Z_F(s_1+s_2)}{Z_S(s_1+s_2)}\right)}. \quad (16)$$

From (16), the amplitude of $A_2(s_2, s_3)$ is expected to be much smaller than that of $B_2(s_2, s_3)$ since usually the feedback impedance $Z_F(s_1 + s_2)$ is expected be much larger than the source impedance $Z_S(s_1+s_2)$ at the frequency range of interest, making the third term in (15) negligible. The remaining fifth term can be removed by making $g''_{m3} + g''_{m5} = 0$. Fig. 4 shows the plot of IIP_3 and $g''_{m3} + g''_{m5}$ versus $V_{\mathrm{gs},M3}$ of the proposed LNA at 400 MHz. In Fig. 4, it can be seen that IIP_3 reaches its maximum of +13.5 dBm at the point where $g''_{m3} + g''_{m5}$ approaches zero. In Fig. 4, the sharp reduction in IIP_3 for $V_{\mathrm{gs},M3}$ smaller than 0.43 V can be explained by the collapsing of the noise-cancelling condition as M_4 starts to turn off by the reduction in the drain current of M_3. Hence, the proposed LNA is

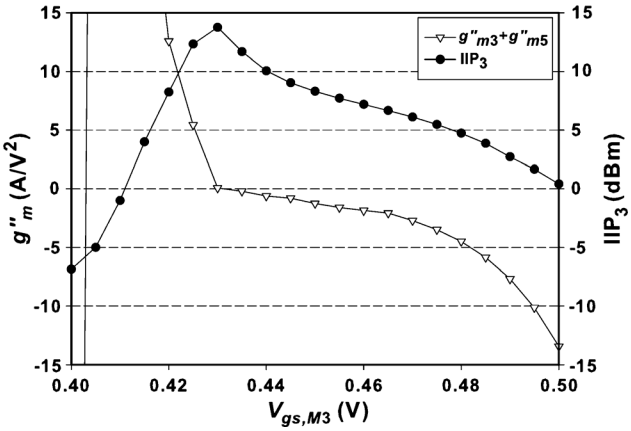

Fig. 4. Plot of IIP_3 and $g''_{m3} + g''_{m5}$ versus $V_{\mathrm{gs},M3}$ of the proposed LNA at 400 MHz.

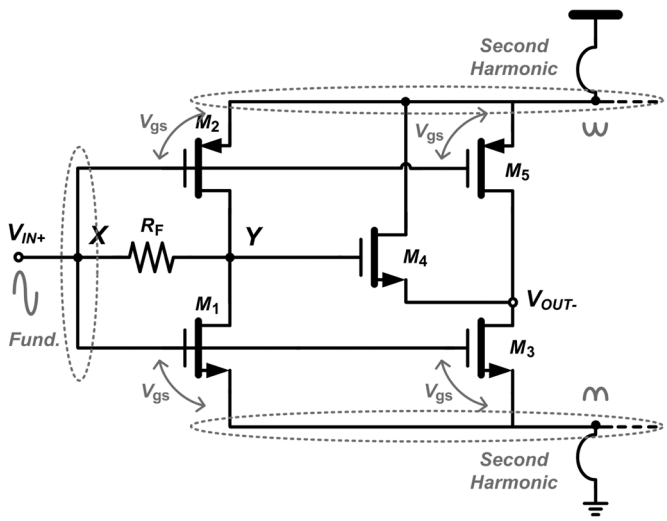

Fig. 5. Half circuit of the proposed LNA to explain how the bond wires can affect IM3.

expected to have better linearity performance than Bruccoleri's LNA.

It is a well-known characteristic that the MOSFET has higher linearity at higher values of V_{gs}. However, in general, higher V_{gs} means a higher amount of power dissipation to reach a certain g_m since g_m/I_D of a transistor is low [23]. In [23], the complementary stage is adopted in an effort to reduce the power dissipation while maintaining high values of V_{gs} for a certain g_m. Another noticeable aspect of the high V_{gs} approach is that it reduces the nonlinear components, but does not eliminate them like the cancelling approach with low V_{gs} introduced in this work.

C. Bond-Wire Effects

In Fig. 2(b), the bond wires are modeled as a series of an inductor and a resistor. The inductance $L_{\omega b}$ and resistance $R_{\omega b}$ of the bond wires are obtained empirically and set to 0.7 nH and 0.7 Ω. Fig. 5 shows the half circuit of the proposed LNA to explain how the bond wire affects IM3. As shown in Fig. 5, second-order harmonics of the input signal can appear at the supply and ground nodes due to the bond-wire impedances. These second-order harmonic signals in combination with the

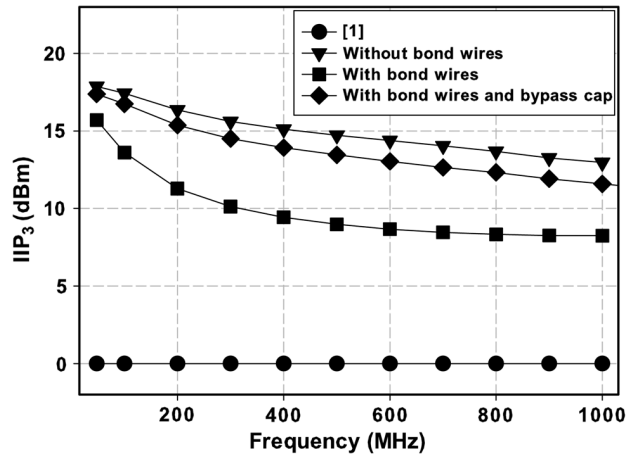

Fig. 6. Simulated IIP_3 of the proposed LNA for comparison with [1], without bond wires, with bond wires, and with bond wires and bypass capacitor.

fundamental input signal can generate other IM3 currents at the drain terminals of M_1, M_2, M_3, and M_5 as these signals induce additional V_{gs} in (11). Therefore, second- and third-order nonlinear components from the presence of bond wires may be present at the output.

There are two different approaches to reduce the adverse impact of bond wires. The bond-wire parasitic can be reduced by increasing the number of pads. However, this is ineffective due to the inductive coupling between bond wires. Furthermore, the additional pads lead to greater chip size. An effective solution to nullify the bond-wire parasitic is the adoption of an on-chip capacitor, C_3, as shown in Fig. 2(b). In Fig. 2(b), the MOS capacitor C_3 is set to around 200 pF as a compromise between the shunt impedance and the die area, and the impedance is around 8 Ω at 100 MHz.

The key idea of the proposed LNA, to improve IIP_3 from Bruccoleri's LNA, is the connection of the gate of M_5 to the input node for the cancellation of g''_{m3} and removing the cascode M_{3b}. We have evaluated the performance of the proposed differential LNA shown in Fig. 2(b) by simulation comparison with [1]. Fig. 6 shows the simulated IIP_3 versus frequency for an offset frequency of 6 MHz. In Fig. 6, by the simple modification of the LNA in [1], the IIP_3 of the proposed LNA is increased by 17.9 and 13 dB at 100 MHz and 1 GHz, respectively. The large improvement in IIP_3 verifies the effectiveness of the proposed scheme in cancelling the nonlinear components of M_3 based on the Volterra analysis. The improvement of IIP_3 is smaller at higher frequencies due to the capacitive parasitic of the transistors.

The impact of bond-wire impedance on the IIP_3 and the effectiveness of the bypass capacitor C_3 in the proposed differential LNA are investigated by simulation. Fig. 6 also shows the simulated IIP_3 versus frequency of the proposed LNA with 6-MHz offset for three different cases; with and without bond wires, and with bond wires and an on-chip bypass capacitor C_3. As can be seen from Fig. 6, the bond-wire impedance degrades the IIP_3 rapidly with increased operating frequency and IIP_3 levels off as the frequency approaches 1 GHz. The maximum difference in IIP_3 between the cases of with and without bond wires is 6 dBm at 600 MHz. It can also be seen that the on-chip

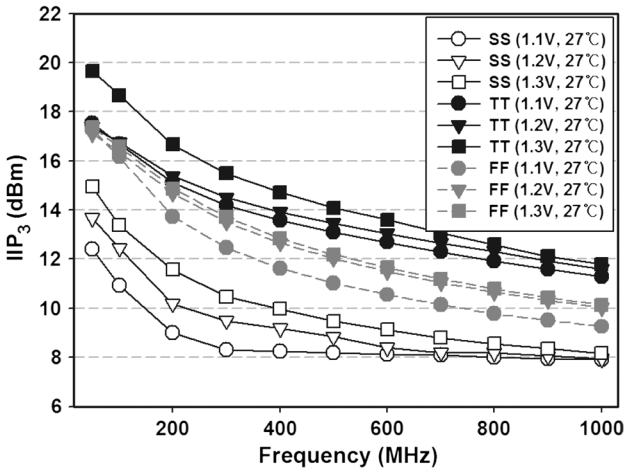

Fig. 7. Simulated IIP_3 of the proposed LNA over the SS, TT, and FF corners of process variations, as well as the supply variations of 1.2 ± 0.1 V at 27 °C.

capacitive bypassing is an effective way to stop the IIP_3 degradation, as IIP_3 degrades less than 2 dB over the entire frequency range.

In order to verify the effect of the second-order harmonics generated by the bond wires, a −20-dBm signal at 400 MHz is applied to the input of LNA. From the simulation, the second-order harmonics of 800 MHz appear at the common nodes of supply and ground with values of −69 and −61 dBm, respectively, while, with adoption of the on-chip bypass capacitor, the harmonics reduce to −80 dBm. For these two cases, the IIP_3 of the LNA changes from 9.43 to 13.92 dBm, an improvement of 4.5 dB.

D. Design Robustness

To demonstrate robustness of the proposed scheme to improve the linearity of the LNA, the performances over the process and voltage variations are investigated. Fig. 7 shows the simulated IIP_3 of the proposed LNA over the slow–slow (SS), typical–typical (TT), and fast–fast (FF) corners of process variations as well as the supply variations of 1.2 ± 0.1 V at 27 °C. In Fig. 7, the IIP_3 shows up to +2.5 and −5.2 dB of variations compare to the value of typical condition (TT, 1.2 V) over the process and supply voltage variations for the whole frequency ranges. Fig. 8(a) and (b) shows the simulated IIP_3 over the process and temperature variations at 500 and 900 MHz. In Fig. 8(a) and (b), IIP_3 varies from 8.1 to 14.2 dBm and from 7.6 to 13.3 dBm at 500 and 900 MHz, respectively.

Fig. 9 shows the IIP_3 versus frequency of the proposed LNA in comparison with that of the same LNA where M_5 is being used as a current source only, as well as the Monte Carlo simulations of the process and mismatch variations. In Fig. 9, by changing of the role of M_5, IIP_3 increases by 14 and 7.6 dB at 50 MHz and 1 GHz, respectively. In Fig. 9, the IIP_3 shows larger variations at the higher values since it is more susceptible to the same variations under the more accurate cancelling conditions, especially in the proposed LNA.

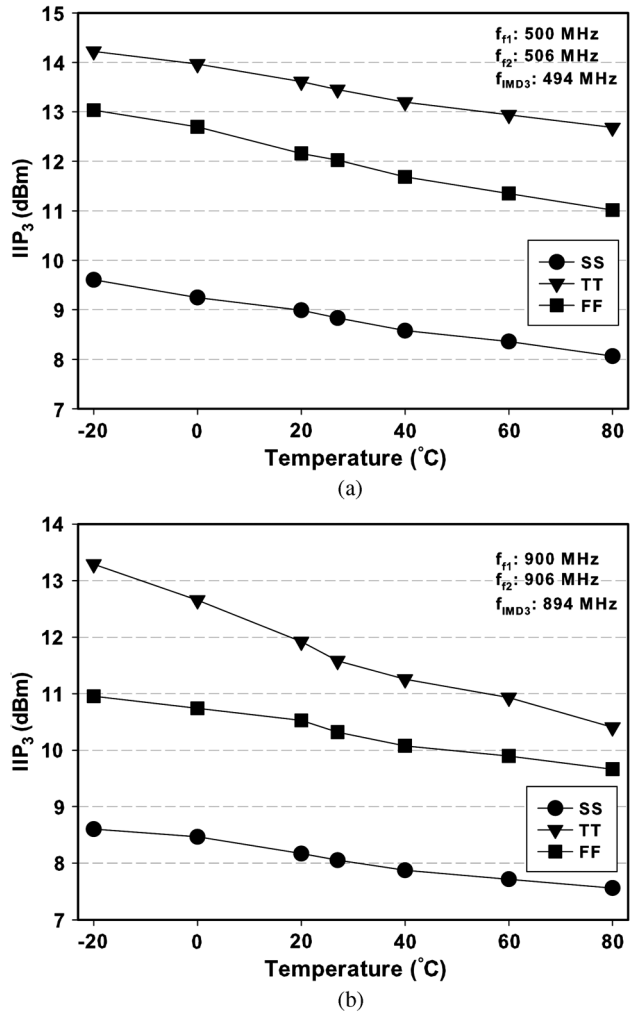

Fig. 8. Simulated IIP_3 of the proposed LNA over process and temperature variations at: (a) 500 MHz and (b) 900 MHz.

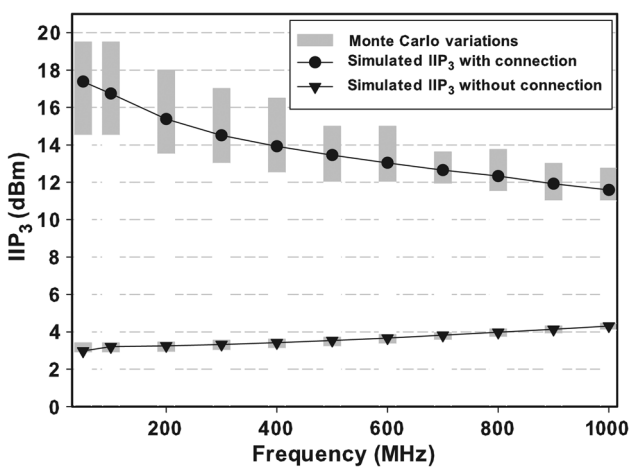

Fig. 9. IIP_3 versus frequencies of the proposed LNA in comparison with that of the same LNA where M_5 being used as a current source only, including Monte Carlo simulations.

In principle, it is a fundamental characteristic of linearity improvement techniques that adopts cancelling to be more susceptible to PVT variations at higher values of IIP_3. Nevertheless, as can be seen from Figs. 7–9, the worst case IIP_3 of the

TABLE I
DIMENSIONS OF DEVICES AND COMPONENT VALUES OF THE PROPOSED LNA

M_1	(17.5μm/0.2μm)×2	R_F	300 Ω
M_2	(15μm/0.2μm)×8	C_1	3.8 pF
M_3	(80μm/0.2μm)×8	C_2	15 pF
M_4	(20μm/0.2μm)×2	C_3	200 pF
M_5	(68μm/0.13μm)×2		

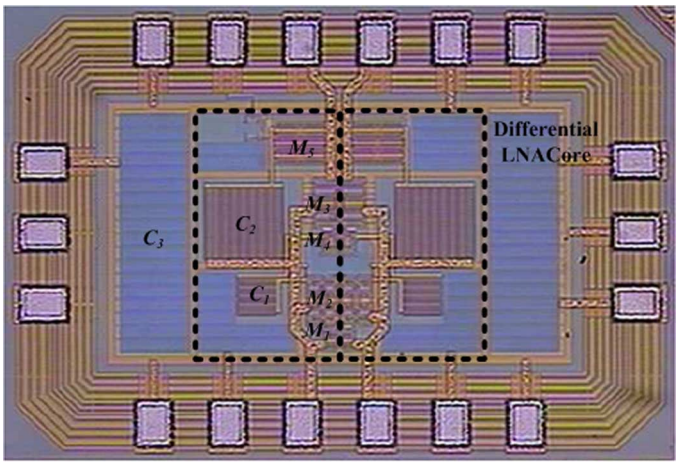

Fig. 10. Die microphotograph.

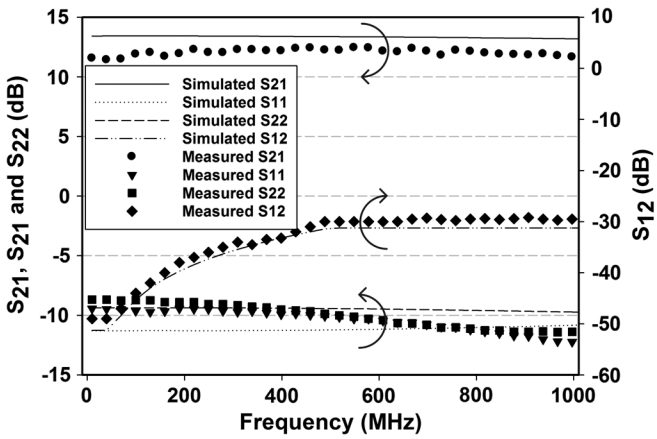

Fig. 11. Measured S-parameters of the proposed LNA in comparison with simulation.

proposed LNA is higher than the typical IIP_3 of [1] by more than 8 dB. Therefore, it can be said that the proposed LNA is a topology that can significantly and reproducibly improve the linearity compared to that of [1].

IV. MEASUREMENT RESULTS

The proposed differential LNA shown in Fig. 2(b) is designed to cover frequency bands from 50 to 860 MHz and is fabricated in 0.13-μm CMOS technology. The LNA dissipates 18.45 mA from a 1.2-V supply. The die size is 0.88 × 0.62 mm^2 and the individual device sizes and major component values are summarized in Table I. A die microphotograph is shown in Fig. 10. The LNA is measured with one supply and ground wire bonding on the printed circuit board (PCB) for proving the role of C_3 and an off-chip balun is used for changing single to differential.

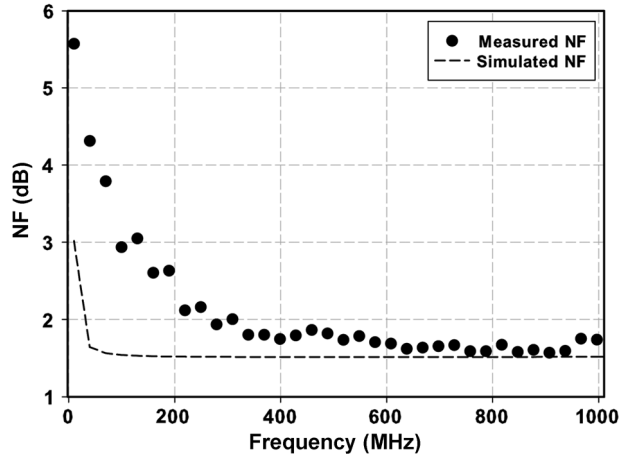

Fig. 12. Measured and simulated NF of the proposed LNA.

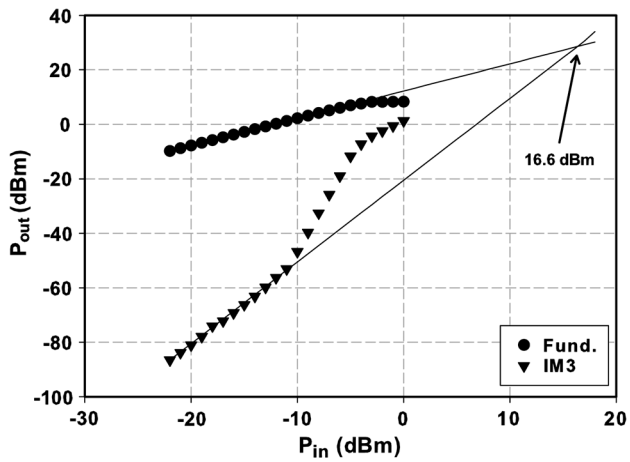

Fig. 13. Measured IIP_3 of the proposed LNA at 100 MHz.

Fig. 11 shows the measured S-parameters up to 1 GHz in comparison with simulation. In Fig. 11, S_{21} has a maximum value of 12.4 dB at 400 MHz. S_{11} and S_{22} remains below −8 dB over the entire frequency band of the measurements. Fig. 12 shows the measured and simulated NF of the proposed LNA. In Figs. 11 and 12, the simulated and measured results are in reasonably good agreement. In Fig. 12, the measured NF is less than 2 dB over most of the target frequency range, which is comparable to that of Bruccoleri's LNA. At low frequencies, NF rises due to the high-pass filtering characteristics of C_1 and R_1 at the gate of M_4 in Fig. 2(a).

Fig. 13 shows the measured IIP_3 of 16.6 dBm at 100 MHz (97 and 103 MHz), which is more than 16.6 dB higher than that of Bruccoleri's and Chen's LNAs. The IM3 cancellation scheme holds effective for blocker power level as large as −11 dBm. Fig. 14 shows the simulated and measured IIP_3 versus $V_{\mathrm{gs},M3}$ at 400 MHz and the both show similar results. An IIP_3 greater than +5 dBm was achieved within a $V_{\mathrm{gs},M3}$ bias window of 90 mV even though it is strong dependence on the value of $V_{\mathrm{gs},M3}$ since $V_{\mathrm{gs},M3}$ control the current of M_4. However, as shown in Fig. 14, if the gate–source voltage of M_5 is separately controlled with each value of $V_{\mathrm{gs},M3}$ for control of the current of M_4, like in [7], the IIP_3 shows less dependent on the value of $V_{\mathrm{gs},M3}$ and

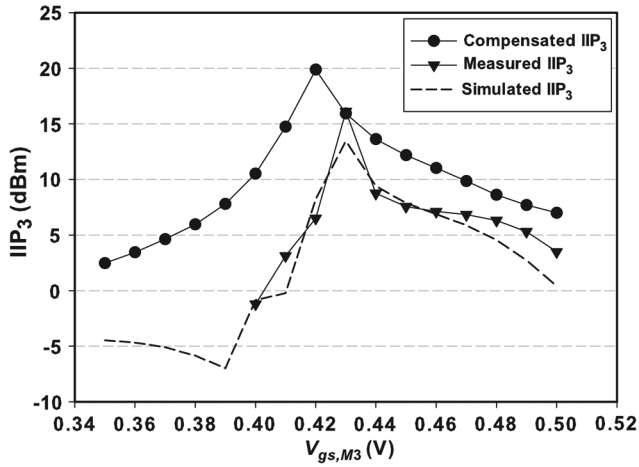

Fig. 14. Simulated and measured IIP_3 versus $V_{\mathrm{gs},M3}$ at 400 MHz.

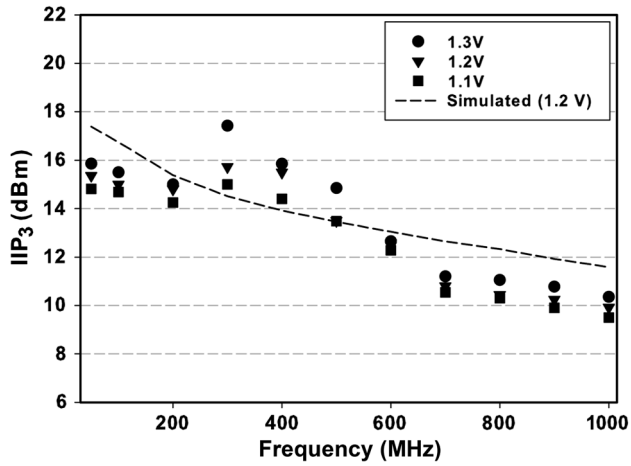

Fig. 16. Measured IIP_3 over the supply voltage variations from 1.1 to 1.3 V.

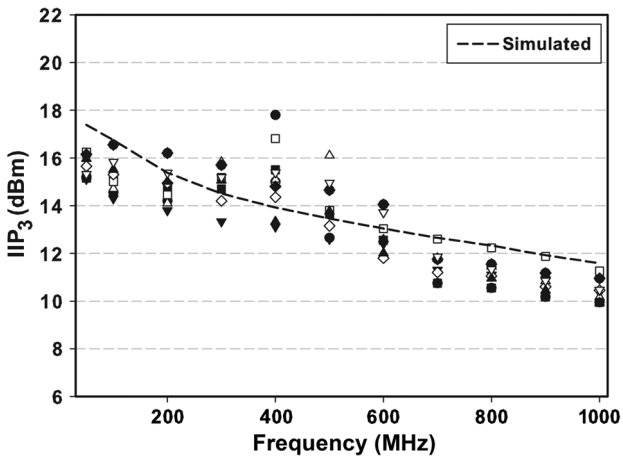

Fig. 15. Measured IIP_3 of ten chips over the frequency range from 50 to 1000 MHz with 6-MHz offset in comparison with simulations results.

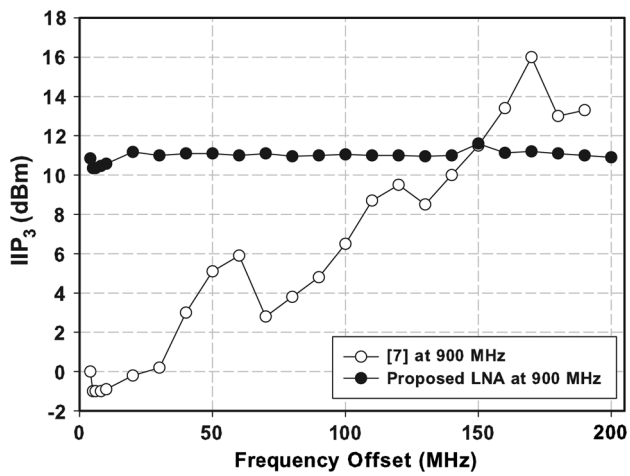

Fig. 17. Measured IIP_3 versus the offset frequency at 900 MHz for the proposed LNA and [7].

high values. From Fig. 14, an IIP_3 greater than $+10$ dBm was achieved within a $V_{\mathrm{gs},M3}$ bias window of 80 mV and it shows better results than that of [7]. All measurements, S-parameter, NF, and IIP_3, are done when $V_{\mathrm{gs},M3}$ is at the optimum point, 0.43 V.

Fig. 15 shows the measured IIP_3 of ten chips over the frequency range from 50 to 1000 MHz with 6-MHz offset in comparison with simulations results. Overall, the measurement results are in good agreement with the simulation. In Fig. 15, the minimum measured IIP_3 is 9.5 dBm at 1 GHz, which is comparable to that of narrowband LNAs that adopt linearity improvement techniques [14]–[22]. Fig. 16 shows the measured IIP_3 over the supply voltage variations from 1.1 to 1.3 V. In Fig. 16, overall, the measurement results show reasonably good agreement with that of simulation results shown in Fig. 9.

Fig. 17 shows the IIP_3 of the proposed LNA measured at 900 MHz, while the offset frequency is varied from 1 to 200 MHz. Fig. 17 also shows the measured IIP_3 of Chen's LNA [7] for comparison. The IIP_3 of the proposed LNA remains nearly constant with less than 2-dB variation over the entire range of offset frequencies at operating frequencies of 900 MHz. In contrast to Chen's LNA [7], the proposed LNA (and Bruccoleri's LNA) does not require a coupling capacitor at the output node, and thereby a uniform IIP_3 over a wide range of offset frequencies is obtained. As expected, Chen's LNA has more than 14-dB IIP_3 variations at operating frequencies of 900 MHz.

In cases of [7] and [24], even though the circuits are designed for wideband operation, it is used for narrowband desired signals. In these wideband circuits, the in-band means the frequency band where the desired signal is present (e.g., 2.1 GHz of WCDMA), while the out-of-band means the frequency band where the blocker signal is present (e.g., 1.76 and 1.95 GHz). Therefore, the out-of-band IIP_3 in [7] and [24] does not represent IIP_3 of the wideband circuits outside the 3-dB bandwidth. However, in the proposed wideband LNA, which is designed for a D-TV tuner, the entire 3-dB bandwidth (48–860 MHz) corresponds to in-band in which all other channel signals work as a blocker signal to the desired signal. Therefore, in this work, the out-of-band IIP_3 described in [7] and [24] is being called the in-band IIP_3.

Fig. 18 shows the measured P1 dB and IIP_2 of the proposed LNA as a function of frequency. In Fig. 18, the measured P1 dBs are lower than the expectation considering the high IIP_3. The 20-dB difference between IIP_3 and P1 dB deviating from the

TABLE II
PERFORMANCE SUMMARY IN COMPARISON WITH RECENTLY PUBLISHED WORKS

	Tech. (nm)	BW (MHz)	S_{11} (dB)	Gain (dB)	NF (dB)	IIP_3 (dBm)	IIP_2 (dBm)	P1dB (dBm)	Freq. Offset[1] (MHz)	Supply (V)	Power (mW)	Area (mm^2)	Type	EFOM (GHz)
[1]	250	2-1600	<-8	13.7	2.5	0	+12	-9	4	2.5	35	0.075	S[2]	1.07
[5]	180	1200-11900	<-11	9.7	4.5	-6.2	+20	-15	1	1.8	20	0.59	S	1.12
[6]	130	1950-2300	<-10	5.2	3.0	+10.5	-	-	7	1.2	12.6	0.66	D[3]	1.03
[7]	130	800-2100	<-15	14.5	2.6	+16(-1)	-	-12	170(6)	1.5	17.4	0.66	S	83.8(1.67)
[9]	180	20-1175	<-10	20.5	3.3	+2.7	+43	-	5	1.8	32.4	0.12	D	7.45
[10]	180	48-1200	<-9	14	3	+3	+44	-	5	2.2	15.8	0.16	S	3.65
[11]	180	48-1000	<-10	16	2.4	-1	+40	-15	5	1.8	30.6	0.25	D	0.98
[12]	130	50-860	<-10	14.5	3.6	+2.5	+38	-	5	1.2	9.6	0.08[4]	D	4.23
[26]	180	470-860	<-10	10	5.7	+10	-	-	7	1.8	5.2	0.52[4]	D	7.5
[27]	120	48-860	<-8	15	3	+5.5	-	-	6	2.5	57.5	-	D	1.58
[28]	180	48-860	<-10	5	8.2	+12	-	-	6	3.3	92.4	0.075[4]	S	0.44
[29]	90	2-1100	<-15	20	1.43	-1.5	-	-	1	1.8	18	0.06	D	4.33
[34]	180	320-1000	<-10	23.5	2.2	0	-	-	-	1.8	15.3	0.1	S	9.95
[36]	180	300-920	<-10	21	2	-3.2	-	-	1	1.8	3.6	0.33	D	10.4
This Work	**130**	**50-1000**	**<-8**	**12.4**	**1.6**	**+16.6**	**+35**	**-3**	**6**	**1.2**	**22.1**	**0.54**	**D**	**34.1**

[1] Frequency offset: for comparisons with [7] since IIP_3 of [7] varies strongly as a function of frequency offset.
[2] Single-ended topology.
[3] Differential topology.
[4] Core only excluding PADs.

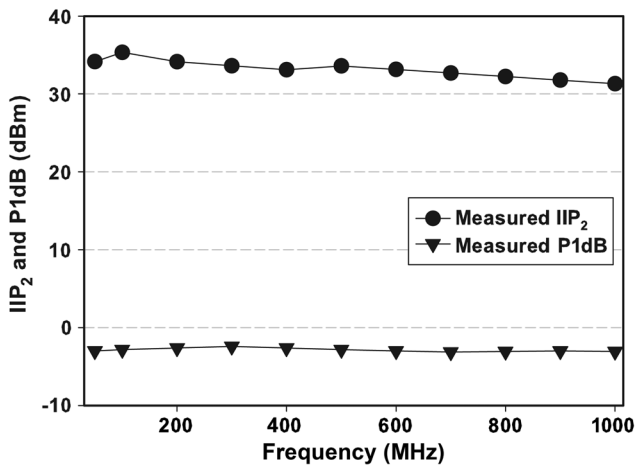

Fig. 18. Measured IIP_2 and P1 dB.

theoretical value of 9.6 dB can be simply explained by the higher order (e.g., fifth) nonlinearity, if the third-order terms have been cancelled. The theoretical value of 9.6 dB is valid only when the third-order terms dominate. However, the proposed LNA still shows more than 5 dB higher P1 dB than that of Bruccoleri's LNA. In Fig. 18, by being a differential amplifier, IIP_2 shows more than 30 dBm over the entire frequency range of interest.

Table II summarizes the measured performance of the proposed LNA in comparison with the state-of-the-art wideband LNAs. It is difficult to make a fair comparison due to the differences in technology, frequency band, supply voltage, frequency offset, etc., but the proposed LNA has the highest IIP_3 and the lowest NF among them. For the quantitative comparison, an effective figure of merit (EFOM) is defined and included in Table II, which is given by

$$\mathrm{EFOM} = \frac{f_m \cdot G_m \cdot \mathrm{IIP}_{3m}}{P_m} \tag{17}$$

where f_m is the power limiting bandwidth, P_m is the power dissipation, G_m is the available power gain, and IIP_{3m} is the third-order intercept point. In Table II, the proposed LNA has overwhelmingly high values of EFOM after [7] even as a differential amplifier. However, for the same frequency offset of 6 MHz, as shown in parentheses, [7] shows far inferior value of EFOM compared to that of the proposed LNA. The IIP_3 of the proposed LNA is higher than that of other LNAs by more than 4–10 dB when the offset frequency is 6 MHz or lower. Note that the proposed LNA, a modification of Bruccoleri's LNA, has not only a much higher IIP_3, but also a lower NF relative to that of Bruccoleri's LNA. The NF of [29] can be compared with the one of this work, however, it comes from high gain. The power consumption of the proposed LNA is comparable to that of Chen's LNA, but lower than that of Bruccoleri's LNA even though the proposed LNA adopts a differential amplifier.

V. CONCLUSION

This paper has presented a new method to increase the linearity in wideband LNAs. Bruccoleri's wideband noise-cancelling LNA [1] is analyzed to identify the source of poor linearity using Volterra series. From the analysis, a modified low-noise high-linearity wideband LNA topology, by connecting the gate of the pMOS transistor to input instead of a bias and adding a decoupling capacitor, is proposed, and achieves high IIP_3 immune to the offset frequency of two-tone signals. Furthermore, this paper identifies linearity degradation due to the bond wires in wideband LNAs, and proposes a scheme to mitigate the effect. The effectiveness of the proposed techniques is demonstrated by comparative simulations.

The proposed LNA is realized in a 0.13-μm standard CMOS process. Measurement results show a high IIP_3 more than +10 dBm for an offset frequency of 6 MHz over the target frequency band from 50 to 860 MHz. The lowest measured NF is 1.6 dB, while drawing 18.45 mA from a 1.2-V supply. The

proposed LNA shows a high enough IIP_3 to be applicable as a wideband amplifier for D-TV tuners.

APPENDIX

VOLTERRA-SERIES ANALYSIS OF THE PROPOSED SINGLE-ENDED LNA SHOWN IN FIG. 2(a)

With the Volterra-series equations (12)–(14), the KCL can be applied to each node to calculate the Volterra-series kernels, given by

$$i_{m1}+\frac{V_y}{r_{o1}}+i_{m2}+\frac{V_y}{r_{o2}}=\frac{V_x-V_y}{Z_F(s)} \tag{A.1}$$

$$\frac{V_x-V_s}{Z_S(s)}=\frac{V_y-V_x}{Z_F(s)} \tag{A.2}$$

$$i_{m4}-\frac{V_o}{r_{o4}}=i_{m3}+\frac{V_o}{r_{o3}}+i_{m5}+\frac{V_o}{r_{o5}}+\frac{V_o}{Z_L(s)} \tag{A.3}$$

where $Z_S(s)=R_S\|1/sC_x$, $Z_F(s)=(R_F+Z_S(s))\|1/sC_y$, and $Z_L(s)=R_L\|1/sC_o$, and i_{m1}, i_{m2}, i_{m3}, i_{m4}, and i_{m5} denote the small-signal current flowing into the source of the five transistors (M_1, M_2, M_3, M_4, and M_5), and are given by

$$i_{mj}=g_{mj}V_x+\frac{g'_{mj}}{2!}V_x^2+\frac{g''_{mj}}{3!}V_x^3 \tag{A.4}$$

$$i_{m4}=g_{m4}V_y+\frac{g'_{m4}}{2!}V_y^2+\frac{g''_{m4}}{3!}V_y^3 \tag{A.5}$$

where $j=1,2,3$, and 5. To find the first-, second-, and third-order Volterra kernels, i_{mi}'s in (A.1)–(A-3) are substituted by the first-, second-, and third-order components of g_m polynomials in (A.4) and (A.5). The first-order Volterra kernels can then be expressed as follows:

$$A_1(s)=\frac{\left(\frac{1}{r_{o1}}+\frac{1}{r_{o2}}+\frac{1}{Z_F(s)}\right)\frac{Z_F(s)}{Z_S(s)}}{(g_{m1}+g_{m2})+\left(\frac{1}{r_{o1}}+\frac{1}{r_{o2}}\right)\left(1+\frac{Z_F(s)}{Z_S(s)}\right)+\frac{1}{Z_S(s)}} \tag{A.6}$$

$$B_1(s)=A_1(s_1)\cdot\left(1+\frac{Z_F(s)}{Z_S(s)}\right)-\frac{Z_F(s)}{Z_S(s)} \tag{A.7}$$

$$C_1(s)=((-g_{m3}+g_{m5})A_1(s_1)+g_{m4}B_1(s_1))\times(r_{o3}\|r_{o4}\|r_{o5}\|Z_L(s))\,. \tag{A.8}$$

The second-order Volterra kernels can be express as

$$A_2(s_1,s_2)=\frac{-\frac{1}{2}A_1(s_1)A_1(s_2)(g'_{m1}-g'_{m2})}{(g_{m1}+g_{m2})+\left(\frac{1}{r_{o1}}+\frac{1}{r_{o2}}\right)\left(1+\frac{Z_F(s_{i2})}{Z_S(s_{i2})}\right)+\frac{1}{Z_S(s_{i2})}} \tag{A.9}$$

$$B_2(s_1,s_2)=A_2(s_1,s_2)\left(1+\frac{Z_F(s_{i2})}{Z_S(s_{i2})}\right) \tag{A.10}$$

$$C_2(s_1,s_2)=\Bigg(-(g_{m3}+g_{m5})A_2(s_1,s_2)+g_{m4}B_2(s_1,s_2)-\frac{g'_{m3}+g'_{m5}}{2}A_1(s_1)A_1(s_2)+\frac{g'_{m4}}{2}B_1(s_1)B_1(s_2)\Bigg)\times(r_{o3}\|r_{o4}\|r_{o5}\|Z_L(s_{i2})) \tag{A.11}$$

where $S_{i2}=(s_1+s_2)$.

The third-order Volterra kernels can be express as

$$A_3(s_1,s_2,s_3)=\Bigg(-\frac{(g'_{m1}+g'_{m2})}{2}\overline{A_1(s_1)A_2(s_2,s_3)}-\frac{(g''_{m1}+g''_{m2})}{6}A_1(s_1)A_1(s_2)A_1(s_3)\Bigg)\times\frac{1}{(g_{m1}+g_{m2})+\left(\frac{1}{r_{o1}}+\frac{1}{r_{o2}}\right)\left(1+\frac{Z_F(s_{i3})}{Z_S(s_{i3})}\right)+Z_S(s_{i3})} \tag{A.12}$$

$$B_3(s_1,s_2,s_3)=A_3(s_1,s_2,s_3)\left(1+\frac{Z_F(s_{i3})}{Z_S(s_{i3})}\right)$$

$$C_3(s_1,s_2,s_3)=\Bigg(-(g_{m3}+g_{m5})A_3(s_1,s_2,s_3)+g_{m4}B_3(s_1,s_2,s_3)+\frac{1}{2}(g'_{m3}+g'_{m5})\,\overline{A_1(s_1)A_2(s_2,s_3)}+\frac{1}{2}g'_{m4}\overline{B_1(s_1)B_2(s_2,s_3)}-\frac{1}{6}(g''_{m3}+g''_{m5})\,A_1(s_1)A_1(s_2)A_1(s_3)+\frac{1}{6}g''_{m4}B_1(s_1)B_1(s_2)B_1(s_3)\Bigg)\times(r_{o3}\|r_{o4}\|Z_L(s_1+s_2+s_3)) \tag{A.13}$$

where $s_{i3}=(s_1+s_2+s_3)$.

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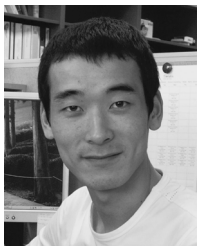

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