0.7–2.7 GHz wideband CMOS low-noise amplifier for LTE application

O.A. Hidayov, N.H. Nam, G. Yoon, S.K. Han and S.G. Lee

A wideband low-noise amplifier (LNA) for long-term evolution applications is presented. A capacitive cross-coupled common-gate in combination with current-bleeding common-source topologies is adopted for wideband input matching, high gain and low noise figure (NF). Inter-cascade inductors are adopted to cancel the inter-stage parasitics, which extend input matching and operational bandwidth to higher frequency with additional NF reduction. Implemented in a 0.18 μm CMOS technology, the proposed wideband LNA shows a voltage gain of 17 dB, a NF of <2.5 dB, $|S_{11}|$ of higher than 10 dB and a maximum IIP3 of $+1.52$ dBm over the frequency range of 0.7–2.7 GHz while consuming 7.5 mA from a 1.8 V supply.

Introduction: The long-term evolution (LTE) technology [1, 2] has been deployed successfully by meeting the requirements of the third-generation mobile communication standards. The LTE standard utilises the frequency span of 0.7–2.7 GHz. Designing the receivers for LTE applications involves many challenges. The low-noise amplifier (LNA) is an important block as the first block of the receiver. Compared with the multiple narrow-band LNAs, which can experience noise figure (NF) degradation by the adoption of switches, a single wideband LNA for LTE application can reduce the die area and the number of pins, reducing the cost. However, the wide-band LNA design involves several challenges in meeting the requirements of high linearity, reasonably flat gain, relatively low NF of <3 dB while satisfying the minimum return loss of more than 10 dB over the frequency band of interest.

Circuit design: Fig. 1 shows the proposed LNA schematic. In Fig. 1, $M_1 - M_2$ constitutes a capacitive cross-coupled common-gate (CCC-CG) topology which provides wideband input matching and a higher value of transconductance. The off- and on-chip inductors L_S and L_{int} are adopted as choke and for the input matching purposes, respectively, and $M_3 - M_4$ are the cascode transistors. The PMOS transistors $M_5 - M_6$ work as current-bleeding devices as well as providing additional transconductance to the CCC-CG topology. The PMOS transistors reduce the bias currents in the load resistors, which allows a larger value of load resistor and therefore larger gain. Since their gates are coupled with the gates of M_1–M_2, the overall voltage gain of the proposed LNA is given by

$$A_V = (2g_{m1,2} + g_{m5,6})R_L \tag{1}$$

where $g_{m1,2}$ and $g_{m5,6}$ represent the transconductances of M_1–M_2 and M_5–M_6, respectively, and R_L is the loading resistor.
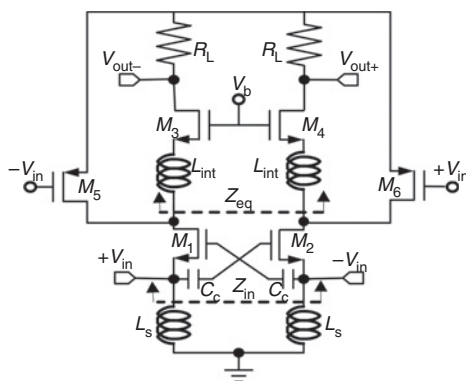

Fig. 1 *Schematic of proposed LNA*

Fig. 2 shows the mechanisms of noise cancelling that occurs for the channel thermal noise of M_1–M_2 in the CCC-CG and the proposed topology shown in Fig. 1. In Fig. 2a, the channel thermal noise of M_1 appears as a common-mode noise at the output, but the amount of noise current at the drain terminal of M_1 is larger than that of M_2 by two times, so that only half of the noise current is being cancelled [3]. In Fig. 2b, $M_5 - M_6$ participate in noise cancelling, and the noise amplified by M_6 is twice the amount of the noise amplified by M_5, bringing

the common-mode noises at the drain terminals of $M_1 - M_2$ closer to each other, meaning a larger amount of noise cancelling. However, because of the additional noise contributed by $M_5 - M_6$, the net effect leads to a higher amount of NF for the whole LNA. Therefore, in this Letter, the size of the PMOS transistors is minimised.
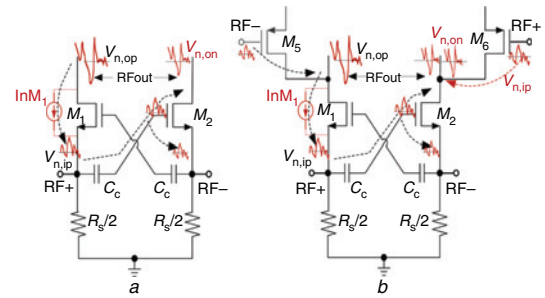

Fig. 2 *Mechanisms of noise cancelling for channel thermal noise of M_1–M_2 in conventional CCC-CG and proposed topology*

a Conventional CCC-CG
b Proposed topology

In Fig. 1, as described in [4], with technology scaling, the input impedance of the CCC-CG deviates from $1/g_{m1,2}$ [5] and becomes a non-negligible function of impedance presented at the drain terminals of M_1–M_2, Z_{eq}. Therefore, due to the parasitic capacitances at the drain terminals of $M_1 - M_2$, it is difficult to achieve wideband matching by making $1/g_{m1,2}$ equal to R_S. From [4], the input impedance of the LNA shown in Fig. 1 is given by

$$Z_{in} = \frac{1}{g_{m1,2}}\left(1 + \frac{Z_{eq}}{r_{ds1,2}}\right) \simeq R_S \tag{2}$$

where $r_{ds1,2}$ is the drain–source resistance of $M_1 - M_2$, $Z_{eq} = [(1/g_{m3,4}) + j\omega L_{int})]\|(1/j\omega C_{par})$, where $g_{m3,4}$ is the transconductance of $M_3 - M_4$ and C_{par} represents the parasitic capacitances at the drain terminals of $M_1 - M_2$. In the proposed LNA, Z_{in} is designed to be equal to R_S. In (2), L_{int} compensates for the reduction in the value of Z_{eq} at high frequencies caused by C_{par}, so that Z_{in} stays nearly equal to R_S. Note that the additional parasitic capacitances provided by $M_5 - M_6$ help reduce the size of L_{int}, allowing smaller chip size.

From (2), if we neglect the contributions of $M_5 - M_6$ considering their small size, then the NF of the proposed LNA can be given by

$$F \simeq 1 + \frac{\gamma}{2}\frac{1}{1 + (Z_{eq}/r_{ds})} \tag{3}$$

where γ represents the transistor's thermal noise parameter. From (3), we can see that the adoption of L_{int} leads to lower NF compared with the case of the conventional CCC-CG. The adoption of L_{int} also helps to extend the bandwidth of the proposed LNA.

Experimental results: The proposed wideband LNA shown in Fig. 1 is optimised for the frequency range of 0.7–2.7 GHz while dissipating 7.5 mA from a 1.5 V supply, and implemented in a 0.18 μm CMOS technology. Fig. 3 shows the chip microphotograph with a size of 1270×700 μm^2 including pads and a buffer that has been included for measurement purpose only.

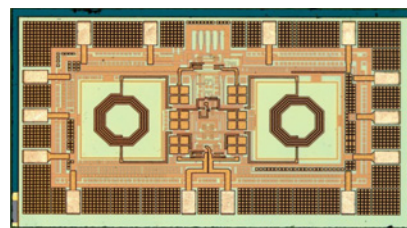**Fig. 3** *Chip microphotograph of proposed LNA with core size of 1270 × 700 μm^2*

Fig. 4a shows the measured S_{11}, S_{21} and NF of the proposed LNA. In Fig. 4a, the measured S_{11} is below -10 dB over the frequency range of 0.5–3.2 GHz, and the voltage gain stays at 17 dB with 1 dB flatness

from 0.5 to 3 GHz with a 3 dB bandwidth of 3.3 GHz. In Fig. 4a, the measured NF stays below 2.5 dB over most of the frequency range of interest. The increase in the NF at frequencies below 1 GHz can be referred to the loss of the transformer that has been adopted for measurement purposes. Fig. 4b shows the IIP3 against frequency measured with 5 MHz spacing two tone signals, where the maximum of 1.5 dBm is obtained at 0.7 GHz.
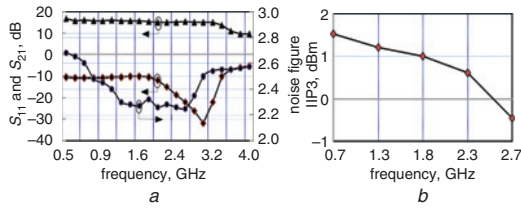

Fig. 4 *Measured results*

a S_{11}, S_{21} and NF against frequency
b IIP3 against frequency

Table 1 summarises the measured performances of the proposed LNA in comparison with other recently reported wideband LNAs. Overall, the proposed LNA shows significant improvements in NF and linearity compared with prior works.

Table 1: Performance summary in comparison with prior works

Refs.	[4]	[5]	[6]	[7]	This work
CMOS	0.18 μm	0.13 μm	0.25 μm	0.18 μm	0.18 μm
BW (GHz)	2.9–11	0.2–3.8	0.02–1.6	3.1–10.6	0.7–2.7
Gain (dB)	16	11.2	13.7	9.7	17
NF (dB)	4	2.85	< 2.4	4.5–5.1	< 2.5
IIP3 (dBm)	N/A	− 2.7	0	− 6.2	1.5
Power (mW)	9.54	1.9	35	20	13.5

Conclusion: A LNA for the LTE system is reported where a capacitive CCC-CG in combination with current-bleeding common-source topologies is adopted for higher gain and lower NF. Inter-cascade inductors are adopted for wideband matching, wider bandwidth and lower NF. The principles and advantages of the proposed design are described. The proposed LNA is implemented in a 0.18 μm CMOS technology. Measurement shows larger than 10 dB input matching, 17 dB voltage gain, 1.5 dBm maximum IIP3 and a below 2.5 dB NF while dissipating 7.5 mA from a 1.8 V supply.

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