A High-Sensitivity and Low-Walk Error LADAR Receiver for Military Application

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***Abstract*—An integrated receiver with high sensitivity and low walk error for a military purpose pulsed time-of-flight (TOF) LADAR system is proposed. The proposed receiver adopts a dual-gain capacitive-feedback TIA (C-TIA) instead of widely used resistive-feedback TIA (R-TIA) to increase the sensitivity. In addition, a new walk-error improvement circuit based on a constant-delay detection method is proposed. Implemented in 0.35 μm CMOS technology, the receiver achieves an input-referred noise current of 1.36 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ with bandwidth of 140 MHz and minimum detectable signal (MDS) of 10 nW with a 5 ns pulse at $\mathrm{SNR} = 3.3$, maximum walk-error of 2.8 ns, and a dynamic range of 1:12,000 over the operating temperature range of $-40\ ^{\circ}\mathrm{C}$ to $+85\ ^{\circ}\mathrm{C}$.**

***Index Terms*—LADAR, laser detection and ranging, laser radar, optical receiver, rangefinder.**

I. Introduction

LASER detection and ranging (LADAR) system is an optical remote sensing technology that can measure the distances to targets by emitting and detecting laser pulses. LADAR systems have been developed with growing interests in recent years [1], [2]. Since the use of optical signals for measuring distances removes the need for physical contact with the target, LADAR technology has been applied in many fields, including the automotive, military or robotics for target identification and range determination [3]–[6], or 2D and 3D imaging systems [7]. Pulsed time-of-flight (TOF) LADAR is widely used to measure distances due to its unique advantage of high precision compare to other measurement methods such as the continuous-wave optical phase method [8], [9].

A block diagram of a typical pulsed LADAR system is shown in Fig. 1. As shown in the figure, pulsed LADAR consists of a laser transmitter and an optical receiver module. Pulsed LADAR measures distances based on the time it takes between a transmitted and reflected optical pulse to be detected by the receiver. Using suitable optical devices, the laser output is focused on the target and a fraction of the transmitted optical pulse is reflected back from the target to the receiver. The receiver, on which this work focuses, converts the detected optical signal into an electrical current pulse using a photodetector, converts the current into voltage with amplification

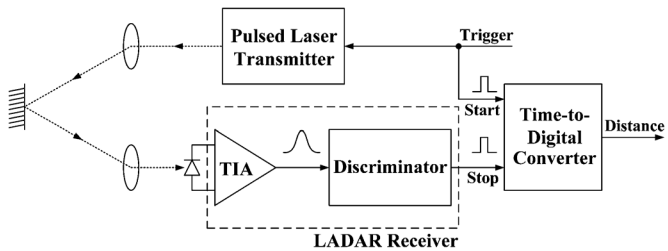

Fig. 1. Block diagram of typical pulsed TOF LADAR.

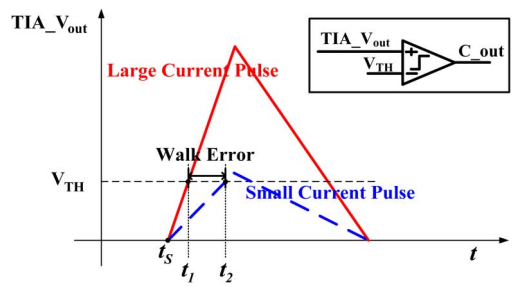

Fig. 2. Timing detection diagram that explains the cause of walk error.

using transimpedance amplifier (TIA), and finally the timing detection block produces a timed logic pulse that indicates the arrival of the optical signal.

In the case of pulsed LADAR for the military purposes, which this work is focused on, the target identification of a few kilometers range is necessary. Since the transmit power and repeatability of a pulse laser are limited, the sensitivity of the LADAR receiver becomes a critical issue. The accuracy of the LADAR is also important. In fact, timing errors of less than mm-level is preferred; however, for military purposes, this is not mandatory, and the accuracy of a few cm-level is sufficient [10].

For the timing detection in pulsed LADAR receiver, a TIA with a leading edge timing discriminator, which uses only a comparator to sense the moment when the output signal of the amplifier block exceeds a certain threshold, is generally used owing to its simplicity. In addition, since the timing event occurs only during the rising edge of the pulse, where no wide linearity range is needed during the timing detection, this approach has the advantages of wide dynamic range and high speed. However, there is a performance limitation in the form of a large timing error caused by the variation in the amplitude of the input current which is induced by the difference in reflectivity or orientation of the target. As shown in Fig. 2, the timing detection by a single comparator with a threshold generates a timing error which is known as a walk error depending on the input amplitude for an object located at the same distance.

This work proposes a high-sensitivity and low-walk error pulsed LADAR receiver architecture for the military purposes. With a capacitive feedback TIA (C-TIA), instead of the widely

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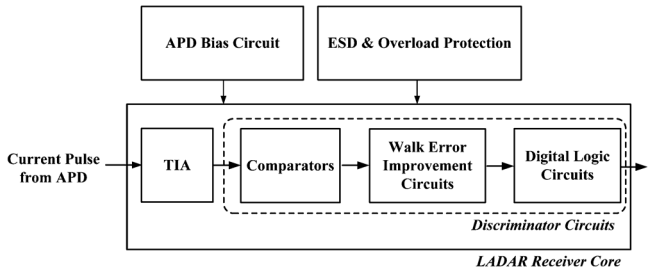


Fig. 3. Block diagram of proposed LADAR receiver.

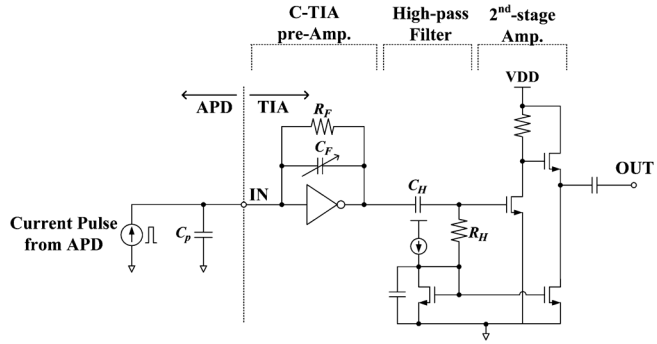


Fig. 4. Schematic of the TIA.

used resistive TIA (R-TIA), the TIA noise can be reduced and facilitates high sensitivity in the receiver, which allows range detection of a few km. Moreover, a new walk-error improvement scheme based on a constant-delay detection method is adopted. In contrast to other commercially available analog LADAR receivers which have been realized as a hybrid circuits or in a BiCMOS technology to provide high-gain and low-noise properties of the bipolar transistor, the receiver is implemented in CMOS technology for good cost efficiency.

The rest of this paper is organized as follows. Section II describes the operational principle, architecture and circuit implementation details of the proposed LADAR receiver. The measurement results of the proposed receiver are shown in Section III, and Section IV presents the conclusion.

II. Proposed LADAR Receiver

The main function of the LADAR receiver is to detect the time moment of the weak optical echo that is reflected from the object. From the well-known radar principle, to increase the detectable range, the minimum detectable power of the receiver should be inversely proportional to the square of the distance [1]. Moreover, since the signal current from the photo detector into the receiver is given by $i_{\mathrm{R}} = P_{\mathrm{R}} \cdot R_0$, where R_0 is the responsivity of the PD (photo detector) and P_{R} the optical power at the receiver, the responsivity of the PD also should be considered.

The photodetector used here is APD (avalanche PD). In general, the gain of photodetector is defined by the multiplication of responsivity and multiplication factor (MR). The gain of a Si APD can be 50 A/W, however, it is not applicable for the eye-safe laser which has wavelength of over 1000 nm [11], [12]. The InGaAs APD can be an alternative to resolve the problem, however, it has the typical gain of only 5 A/W. Therefore, the minimum detectable signal current for the receiver should be under few tens of nA to use InGaAs APD.

The signal-to-noise ratio (SNR) can also be estimated by the basic radar equation [13]. With the detection probability (P_{d}) and false alarm probability (P_{fa}) of 0.5 and 10^{-3}, respectively, which is enough for the military application, the required SNR of LADAR is around 3.3 which is different from that of the general tens of meter detection LADAR system. The SNR of $\sim$10 would be advantageous for mm-level accuracy.

Fig. 3 shows the block diagram of the proposed LADAR receiver. In Fig. 3, the receiver consists of four parts, the transimpedance amplifier (TIA), discriminator circuit, protection circuit (not shown here) and the APD bias circuit. The TIA is an analog circuit which converts the input current pulse from the APD into voltage. The discriminator circuits consist of several comparators, walk error improvement circuits, and digital logic circuits. The comparators play an important role of distinguishing signal versus noise by comparing the output voltage of TIA with the pre-determined threshold voltages. Since the conventional discriminator with simple threshold based discrimination introduces significant walk error, in the proposed LADAR receiver, a novel walk-error improvement circuit based on a constant delay detection method is adopted. The digital logic circuit generates digital output lasting 20 ns if it detects signal. In addition, it generates a reset signal through some logical process. The APD bias circuit provides temperature compensated bias for the APD. Finally, the protection circuits include over current protection and ESD protection circuits.

A. TIA

The TIA converts the current pulse created from the APD into voltage signal. There are several design issues such as gain, noise, recovery time and leakage current. Since the R-TIA generates output voltage by making the input current flow through the feedback resistor, it is advantageous in terms of speed. However, the feedback resistor degrades noise characteristic of TIA, it is disadvantageous in terms of sensitivity. Therefore, the R-TIA topology is widely used for few of few tens of meter range LADAR system with high accuracy of mm-level [14]–[17]. To adopt R-TIA topology to military application which requires high sensitivity for km range detection, it is needed to design R-TIA with bipolar transistors which has superior noise characteristic to CMOS or to use high power laser. However, both solutions are not proper in respect of cost efficiency.

Fig. 4 shows the schematic of the proposed TIA, which consists of a C-TIA based pre-amplifier, a C-R high-pass filter, and a second amplifier. Instead of using R-TIA, the proposed TIA adopts C-TIA topology, which is one of charge amplifier topologies and has advantages in noise, gain and speed compared to other charge amplifier topologies such as the source follower per detector (SFD) or the direct injection (DI) approaches [18]. Since the C-TIA converts input current into output voltage by charging the feedback capacitor which has lower noise characteristic than resister, the sensitivity of the LADAR receiver can be greatly improved. The C-TIA transfers the input charge to the feedback capacitor and produces an output voltage with amplitude given by

$$V = \frac{q}{C_F} \tag{1}$$

where q is the amount of charge and C_{F} the feedback capacitance.

The performance of the amplifier that constitutes the C-TIA affects the performances of C-TIA in two respects. One is charge collection efficiency and the other is rise time of the impulse response. The charge collection efficiency affects the gain of C-TIA and the rise time of the impulse response determines the minimum pulse width that can be detected. From (1), in general, the range of capacitor $C_{\rm F}$ is only a few tens of fF for a high conversion ratio. Meanwhile, the APD, which is attached to the input of the C-TIA, has 2.5 $\sim$ 5 pF range of parasitic capacitance $C_{\rm P}$ depending on the temperature. Therefore, to reduce charge leakage into the parasitic capacitance of the APD and increase the charge collection efficiency of $C_{\rm F}$, the gain of the amplifier that constitutes the C-TIA should be high enough and robust to temperature variation. In addition, the rise time of the impulse response of the C-TIA is determined by

$$\tau_r = \frac{C_P}{C_F}\frac{C_O}{g_m} = \frac{C_P}{C_F}\frac{1}{GBW} \tag{2}$$

where $C_{\rm O}$ is output capacitance and GBW is gain bandwidth of the amplifier.

In the design, a three-stage inverting amplifier [2] is adopted for the TIA, rather than a common source or cascode amplifiers, which has high DC gain of about 80 dB with GBW of about 6.8 GHz. With the amplifier having $C_{\rm F} = 250$ fF, the charge leakage into $C_{\rm P}$ is less than 0.1%, and simulation shows the rise time $\tau_{\rm r}$ around 1.5 ns which is small enough for the input pulse with pulse width of 5 ns. Moreover, to increase the dynamic range of the system, $C_{\rm F}$ is designed to vary in two steps. The capacitance ratio between the low and high gain modes is set to be 1:30. Since the selection switch has parasitic capacitance, it is also considered in the design.

In Fig. 4, the shunting resistor $R_{\rm F}$ compensates the temperature-dependent dark current of the APD. The value of $R_{\rm F}$ should be high enough so that it would not degrade the noise performance. When the shunting resistor $R_{\rm F}$ is connected, then, the output voltage of C-TIA is then given by

$$V = \frac{q}{C_F}e^{-\frac{t}{\tau_F}} \tag{3}$$

where $\tau_{\rm F} = R_{\rm F}C_{\rm F}$ is feedback time constant.

Having $R_{\rm F} = 1$ MΩ and $C_{\rm F} = 250$ fF, then, $\tau_{\rm F}$ is 250 ns which results in a slow recovery time and degrades the multi-target resolution of the LADAR system. In a typical C-TIA, a reset switch is inserted to resolve this problem. However, in this work, this approach is hard to apply since the charge injection contributes additional settling time for the reset. In the proposed design, the inverting amplifier in Fig. 4 is designed to operate properly over a wide range of DC bias considering the bias variation due to the continuous input integration and a $C_{\rm H} - R_{\rm H}$ high-pass filter is cascaded at the output for the pulse shaping.

When the $C_{\rm H} - R_{\rm H}$ high pass filter is cascaded to C-TIA with much smaller time constant $\tau_{\rm H} = C_{\rm H}R_{\rm H}$ than $\tau_{\rm F}$ ($\tau_{\rm H} \ll \tau_{\rm F}$), then the recovery time is now then dominated by $\tau_{\rm H}$ and can be greatly reduced. In addition, the $C_{\rm H} - R_{\rm H}$ high-pass filter also performs low-frequency noise rejection which is advantageous in the sensitivity. Since $\tau_{\rm H} \ll \tau_{\rm F}$ and $R_{\rm F} = 1$ MΩ which is large enough, the total transfer function of the C-TIA with high pass filter can be approximated as

$$\begin{aligned} H(s) &= H_{CTIA}(s)\cdot H_{HP}(s) \\ &= \frac{R_F}{1+s\cdot\tau_F}\cdot\frac{s\cdot\tau_H}{1+s\cdot\tau_H} \approx \frac{1}{s\cdot C_F}\cdot\frac{s\cdot\tau_H}{1+s\cdot\tau_H} \end{aligned} \tag{4}$$

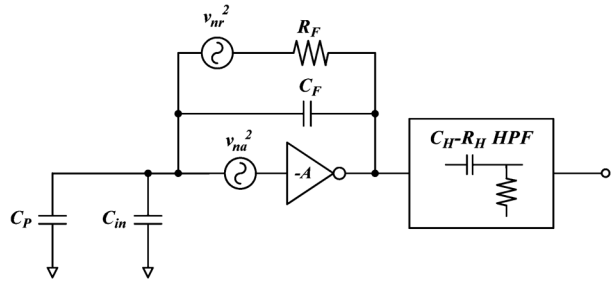


Fig. 5. Noise sources of the TIA.

where $H_{CTIA}(\rm s)$ and $H_{HP}(\rm s)$ are transfer functions of C-TIA pre amplifier and high pass filter, respectively.

In the design, $C_{\rm H}$ and $R_{\rm H}$ are 2 pF and 500 Ω, respectively. Then, $\tau_{\rm H}$ is calculated as 1 ns, and from (4), the total bandwidth is calculated as $f_0 = 1/(2\pi\cdot\tau_{\rm H}) \approx 160$ MHz. However, the simulation shows the total bandwidth of around 140 MHz which might be caused by parasitic R and C. Finally, a common-source second-stage amplifies shaped signal and the final TIA output is generated through the buffer.

The predominant noise sources of the TIA are from C-TIA based pre-amplifier. Fig. 5 shows the equivalent noise sources of the pre-amplifier which are thermal noise of the feedback resistor and the input-referred voltage noise of the core amplifier that are denoted as $v_{\rm nr}^2$ and v_{na}^2, respectively. $C_{\rm in}$ is the capacitance of input transistor of the amplifier. The thermal noise of the feedback resistor is given by

$$v_{nr}^2 = 4kTR_F \tag{5}$$

where k is the Boltzmann constant and T the temperature in Kelvin.

The noise contribution of the thermal noise of the feedback resistor at the output of $\rm C_H - R_H$ HPF can be calculated by [19]

$$v_{nr,out}^2 = \frac{kT}{C_f}\frac{\tau_H}{(\tau_F+\tau_H)} \approx \frac{kT}{C_f}\frac{\tau_H}{\tau_F} \tag{6}$$

Since $\tau_{\rm F}$ is much larger than $\tau_{\rm H}$, then, $v_{nr,out}^2$ can be neglected in the total output noise of the TIA. The noise of core amplifier is mainly coming from input transistors and its power spectral density is given by

$$v_{na}^2 = \frac{8}{3}\frac{kT}{g_m} + \frac{K_f}{C_{ox}^2WLf} \tag{7}$$

where $g_{\rm m}$ is the transconductance, $C_{\rm ox}$ is the gate oxide capacitance per area, $K_{\rm f}$ is the process dependent flicker noise parameter, and f is the frequency. The first term is the thermal noise of the input transistor, and the second term describes the 1/f noise which is mainly due to trapping of charges in the transistor channel. The noise contribution of v_{na}^2 at the final output of TIA can be calculated by [20]

$$v_{na,out}^2 = \left(\frac{C_T}{C_F}\right)^2\left(\frac{1}{3}\frac{kT}{g_m}\frac{A^2}{\tau_H} + \frac{K_f}{C_{ox}^2WL}\frac{A^2}{2}\right) \tag{8}$$

where $C_{\rm T}$ is total capacitance at the input of C-TIA pre amplifier including $C_{\rm F}$, $C_{\rm P}$ and $C_{\rm in}$ and A the second common source amplifier gain.

From (8), to minimize the noise, the size of the input transistors of the core amplifier are determined to achieve large $g_{\rm m}$ while maintaining small WL to make $C_{\rm in}$ small.

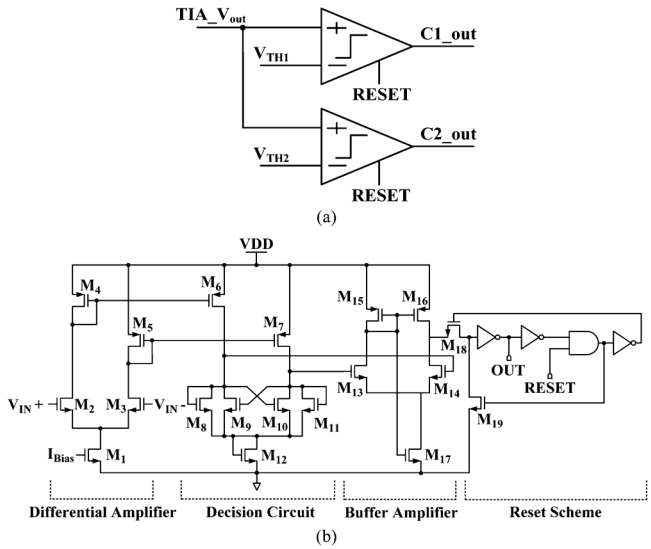


Fig. 6. (a) Double threshold comparator schematic; (b) circuit of the comparator.

B. Comparators

After the current pulse from the APD is converted into voltage by the TIA, two comparators compare the signal with pre-determined threshold voltages V_{TH1} and V_{TH2}, as shown in Fig. 6(a). As mentioned above, a comparator with single threshold can cause significant walk error. The proposed LADAR uses two threshold voltages V_{TH1} and V_{TH2} in the discriminator to improve walk error with relations given by

$$V_{TH2} = 2 \times V_{TH1} \tag{9}$$

The detail method of walk error improvement circuit will be discussed in the next section.

A conventional topology [21] is used for the comparator as shown in Fig. 6(b) where M_1 through M_7 constitute a differential amplifier with active loads which execute pre-amplification. Since the topology has no high impedance nodes in the pre-amplification stage without input and output, a high speed operation can be ensured. Since the offset of the comparator can lead to extra timing error, the comparator is designed to have a low offset. For the purpose, M_8 through M_{11} constitute a cross gate-connected positive-feedback decision circuit to increase the gain of the decision element. M_{13} through M_{17} constitute a self-biased differential output buffer amplifier which converts the output of the decision circuit into a logic signal. Moreover, the comparator must have hysteresis so that it should not respond to ripples or noises in the signal while making a decision. Therefore, as shown in Fig. 6(b), the output of the comparator is designed to reset its decision only when the reset signal is applied to the comparators despite the signal becomes lower than the threshold voltage.

C. Walk Error Improvement Circuit

To mitigate the walk error, there are various techniques have been proposed. The constant fraction timing method [19] reduces walk error by detecting the crossing point of the trailing edge of the original timing pulse and the leading edge of its delayed replica with a comparator. Other approaches use automatic gain control (AGC) [8], amplitude [14], or unipolar-to-bipolar shaping [15] to compensate the error.

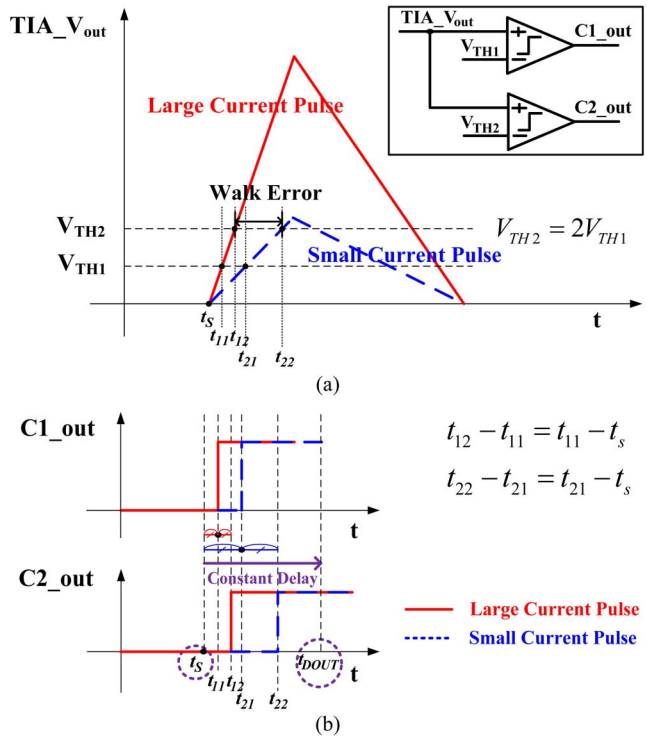


Fig. 7. Concept of constant-delay detection method: (a) TIA output and (b) comparator output.

However, these methods need to have linear dynamic range and it is typically less than 1:3000 which is not enough. To improve walk error with large dynamic range, the time-domain walk error compensation scheme is proposed in [16], [17]. It achieves low walk error over dynamic range of 1:100,000, however, the technique requires additional TDC to generate a pulse for compensation. Additionally, the TIAs of previous works adopts R-TIA topology with minimum detectable signal (MDS) level of a few μA, which make them incompatible as a few kilometers range detector but only a few tens of meter. Therefore, a new walk error improvement circuit with large dynamic range and which can be applicable to C-TIA is needed.

The concept of the proposed walk error improvement circuit is described in Fig. 7. In Fig. 7, t_{11} and t_{12} are the time points when the large amplitude signal reaches at V_{TH1} and V_{TH2} while t_{21} and t_{22} are the time points when the small amplitude signal reaches at V_{TH1} and V_{TH2}, respectively. In Fig. 7(a), with a double-threshold comparator circuit, shown in the inset, and assuming that $V_{\mathrm{TH2}} = 2V_{\mathrm{TH1}}$ as described in (9), the following relation can be derived by a simple geometric analysis.

$$t_{n2} - t_S = 2 \times (t_{n2} - t_{n1}) \tag{10}$$

where t_{n1} and t_{n2} are the time points when the output signal of the TIA reach at V_{TH1} and V_{TH2}, respectively, and t_{S} denotes the start time of the signal integration. From (10), a constant time t_{S} can be estimated by taking the time difference between t_{n1} and t_{n2}. As shown in Fig. 7(b), if an accurate estimation of t_{S} can be made from (10), then, by generating the output signal at some time t_{DOUT} which is a constant time delayed from t_{S}, $t_{\mathrm{DOUT}} - t_{\mathrm{s}}$, it is possible to detect the incoming signal with no walk-error regardless of the amplitude of the signal.

Fig. 8 shows the circuit schematic to implement the constant-delay detection method shown in Fig. 7 and schematic that

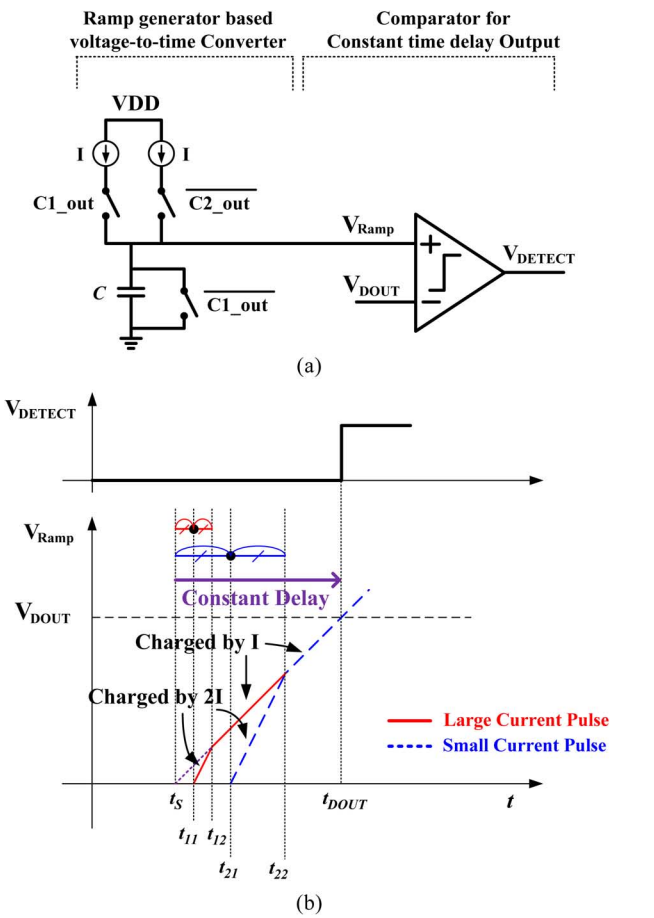


Fig. 8. Constant-delay detection method: (a) circuit implementation and (b) operation principle.

explains the operation principle. In Fig. 8(a), a voltage-to-time converter with a slope controllable ramp generator which consists of switched current sources and a charging capacitor is used to estimate $t_{\rm S}$, and a comparator is used to create a constant time-delayed output. As shown in Fig. 8(b), the time $t_{\rm S}$ is estimated by the amount of charges accumulated in the capacitor C. First, for the case of large TIA output, when the TIA output approaches $V_{\rm TH1}$ at time t_{11}, then, $C1\_OUT$ will go high and $C2\_OUT$ would still be at low. Then, following (10), the switched current sources charge C by $2I$ until the TIA output reaches $V_{\rm TH2}$ and $C2\_OUT$ becomes high at t_{12}. In that case, the amount of charges accumulated into C at t_{12} becomes identical to the case of when C is charged with I from $t_{\rm S}$ to t_{12}. After t_{12}, $C2\_OUT$ becomes high and the charging current is reduced to I. Then, at the time $t_{\rm DOUT}$ which is delayed by a constant amount with respect to $t_{\rm S}$ can be generated when the voltage across the capacitor C becomes $V_{\rm DOUT}$ which is the reference voltage of the comparator shown in Fig. 8(a). In the case of small TIA output, even though the charge accumulation starts at t_{21} which is later than t_{11}, the voltage across the capacitor C approaches $V_{\rm DOUT}$ at the same $t_{\rm DOUT}$. In other words, the voltage $V_{\rm RAMP}$ which is the voltage across the capacitor C always approaches $V_{\rm DOUT}$ at the same time $t_{\rm DOUT}$ independent of the amplitude of TIA output, accordingly, the walk-error can be diminished.

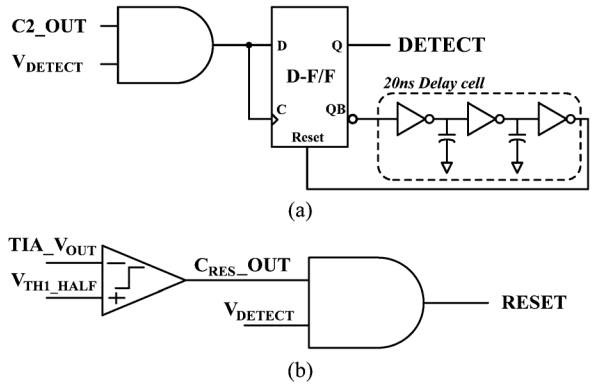


Fig. 9. Digital logic circuits to make: (a) final output and (b) reset signal.

D. Digital Output Block and Reset Logic

In Fig. 8(a), $V_{\rm DETECT}$ can become high even if the TIA output voltage does not become larger than $V_{\rm TH2}$, in which case the input signal should be considered as a noise. Moreover, the pulse width of $V_{\rm DETECT}$ varies depending on the amplitude of the input signal. Therefore, a digital logic circuits which consists of an AND gate and a D-Flip/Flop (D-F/F), as shown in Fig. 9(a), is used to reduce the false alarm rate and to ensure that the output signal would have a constant pulse width. In Fig. 9(a), first, when $V_{\rm DETECT}$ becomes high, the AND gate judges whether or not the output voltage of the TIA is noise. If the TIA output does not reach up to $V_{\rm TH2}$, which means that the detected signal is a noise, then, $C2\_OUT$ and the output of the AND gate would stay low. If the output goes above $V_{\rm TH2}$, the output of the AND gate becomes high and applied to the input of D-F/F. Then, due to the tied connection of the input D and clock C, D-F/F is being set to read data only mode at the rising edge of the input. The 20 ns delay-cell shown in Fig. 9(a) allows the generation of final output *DETECT* at node Q with a constant pulse width of 20 ns.

Fig. 9(b) shows the digital logic circuit to generate the reset signal *RESET* for the two comparators in Fig. 6(a). Since the output of the comparators should not vary during period of charging the capacitor to make a "constant delay" shown in Fig. 8, the outputs of comparators in Fig. 6(a) become low only when the *RESET* signal is applied even though the signal becomes lower than the reference voltage. The *RESET* signal is generated by the AND gate with two input signals shown in Fig. 9(b); One is C_{RES_OUT} produced by the comparator when the amplitude of TIA output voltage is lower than $V_{\rm TH1\_HALF}$ which is half the voltage of $V_{\rm TH1}$, while the other is $V_{\rm DETECT}$, as shown in Fig. 8(b).

Fig. 10 shows the timing diagram for overall operation of the proposed LADAR. It shows two cases; the amplitude of TIA output voltage being lower or higher than $V_{\rm TH2}$. As shown by the *DETECT* signal in Fig. 10, the former is detected as a noise while the latter being detected as a signal.

E. Over-Current Protection Circuit

If a very high optical power is applied to the APD, the TIA cannot handle the input current and can be damaged by the high voltage induced at the input. In the proposed design, as shown in Fig. 11, a simple and efficient over-current protection circuit is

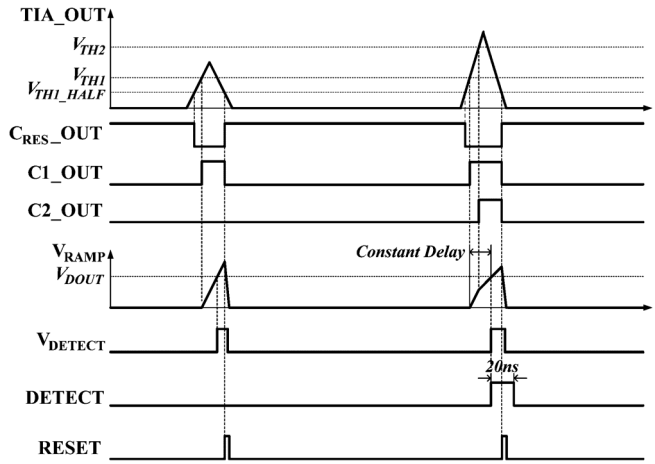


Fig. 10. Operation timing diagram of the proposed LADAR.

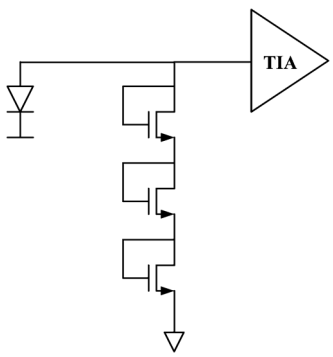


Fig. 11. Over-current protection circuit.

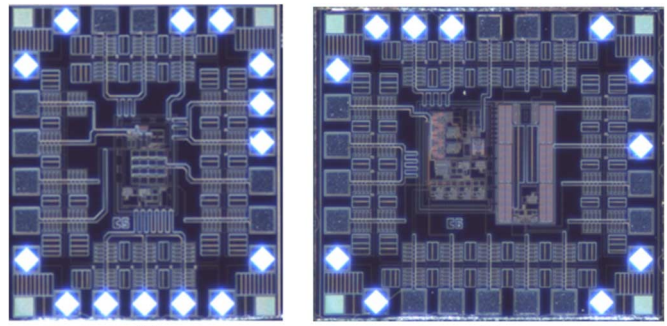
adopted at the input of the TIA in the form of a three diode-connected NMOS transistors in series. The overload current which is about 1 mA flows through the diode when the voltage at the input of TIA exceeds the turn-on voltage of the diodes, which is approximately 1.1 V.

F. APD Bias Circuits

Since the responsivity of APD varies with temperature, usually an extra cooling system is attached to the LADAR system to compensate the performance degradation by the gain variation of APD, which makes it cost inefficient. Instead, in the proposed LADAR receiver, the gain is controlled to stay constant by adjusting the bias voltage of APD. With a temperature sensor and a discrete circuit which references the temperature and the BGR voltage, the APD bias voltage is designed to change automatically, when the temperature varies from $-50\ ^{\circ}\mathrm{C}$ to $75\ ^{\circ}\mathrm{C}$.

III. Experimental Results

The proposed LADAR receiver is fabricated in a 0.35 μm CMOS technology as a two-chip solution, the TIA and remaining blocks. Separating the TIA from the remaining blocks helps to suppress the digital-to-analog crosstalk via supply or ground, leading to better sensitivity. The chip microphotographs of the TIA and remaining blocks are shown in Fig. 12, with sizes of $1.0 \times 1.2\ \mathrm{mm}^2$ and $1.3 \times 1.2\ \mathrm{mm}^2$, respectively. The two chips are assembled into a TO-8 stem with a radius of 7.2 mil, as shown in Fig. 13. In Fig. 13, an InGaAs APD is located at the center of the stem, and the total APD gain is set to 5 A/W. For the measurement, a 5 ns optical pulse shown in Fig. 14 is applied to the APD through an attenuator. As shown



(a) (b)

Fig. 12. Chip microphotograph of the (a) TIA, (b) remaining blocks.

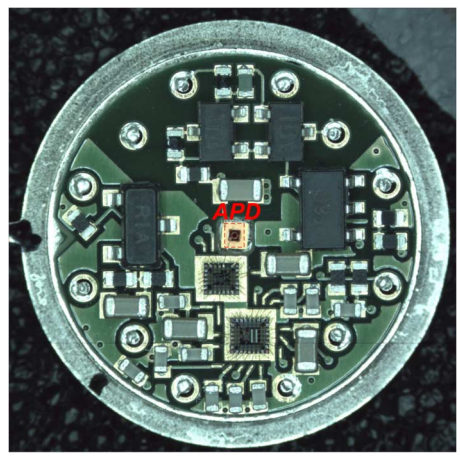


Fig. 13. Photograph of the proposed LADAR receiver with APD.

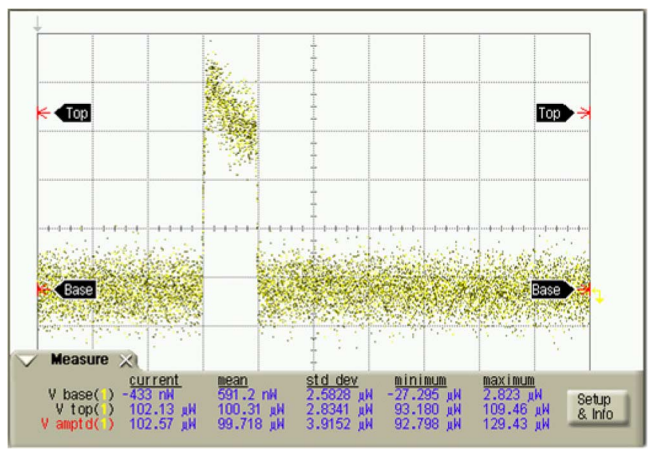


Fig. 14. Applied 5 ns optical pulse.

in Fig. 14, the laser pulse with rising and falling time less than 100 ps is used to minimize the nonlinear effect of laser pulse on the evaluation of receiver performances. Moreover, in Fig. 14, the extinction ratio of the optical signal can be estimated as 20 dB. The operation temperature is changed from $-40\ ^{\circ}\mathrm{C}$ to $85\ ^{\circ}\mathrm{C}$ within a chamber.

Fig. 15 shows the measured rms noise at the output node of the TIA. The measured rms noises are 6.0 and 1.9 mV for high and low gain mode, respectively. Since the rms noise in the high-gain mode is 6.0 mV, the minimum detectable signal (MDS) is calculated as $6.00 \times 3.3 = 19.8\ \mathrm{mV}$ when $\mathrm{SNR} = 3.3$. To estimate the MDS of the input optical power, a replica of the TIA output which is used for optical alignment is measured, as shown in Fig. 16. Fig. 16(a) depicts the results when the input

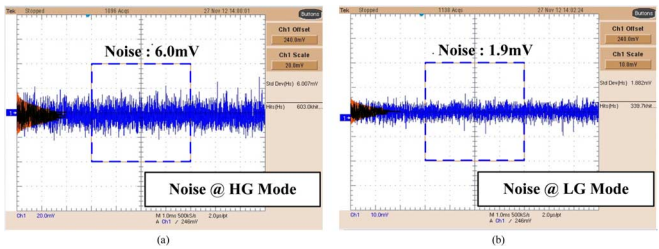


Fig. 15. Measured rms noise at the output of the TIA in the (a) high-gain and (b) low-gain modes.

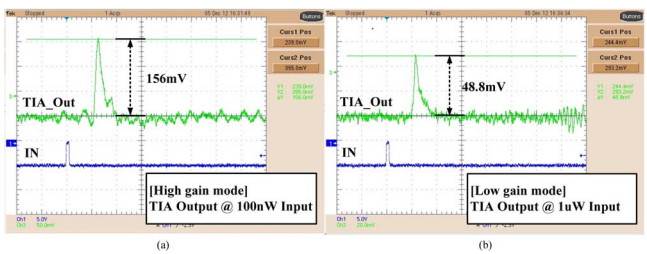


Fig. 16. Measured output of the TIA in the (a) high-gain mode with 100 nW input, and (b) low-gain mode with 1 uW input.

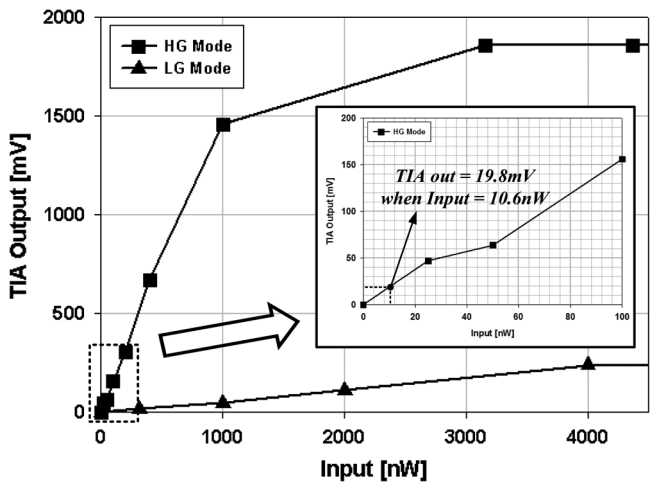


Fig. 17. Optical input power vs. output voltage of the TIA in the high and low gain modes.

is 100 nW in the high-gain mode where amplitude of the TIA output voltage is 156 mV. Fig. 16(b) shows that the amplitude of output voltage is 48.8 mV when the input is 1 μW in the low-gain mode. These results represent TIA gain of 110 and 78 dBΩ for high and low gain modes, respectively. Fig. 17 shows a graph of the TIA output voltage versus the input power in the high and low gain modes. The slopes of the two curves represent the gain of the TIA under each gain modes, and the ratio of the two gains is 1:30. From Fig. 17, the minimum detectable optical signal of the receiver can be estimated as 10.6 nW, in which case the TIA output becomes 19.8 mV. Since the total APD gain is set to 5 A/W, the minimum detectable current of the TIA would be 53 nA. Considering the TIA bandwidth of around 140 MHz, the input referred noise current is calculated as 1.36 pA/$\sqrt{\text{Hz}}$. In addition, in Fig. 17, since the maximum input power that can be applied in the high-gain mode is 4.4 μW, the estimated dynamic range 1:400. Moreover, when the applied input power increases to around 5 μW in the low-gain mode, the TIA gain is reduced and apparently the output voltage saturates. This occurs due to the limited extinction ratio of the optical source. Since the extinction ratio of the optical source

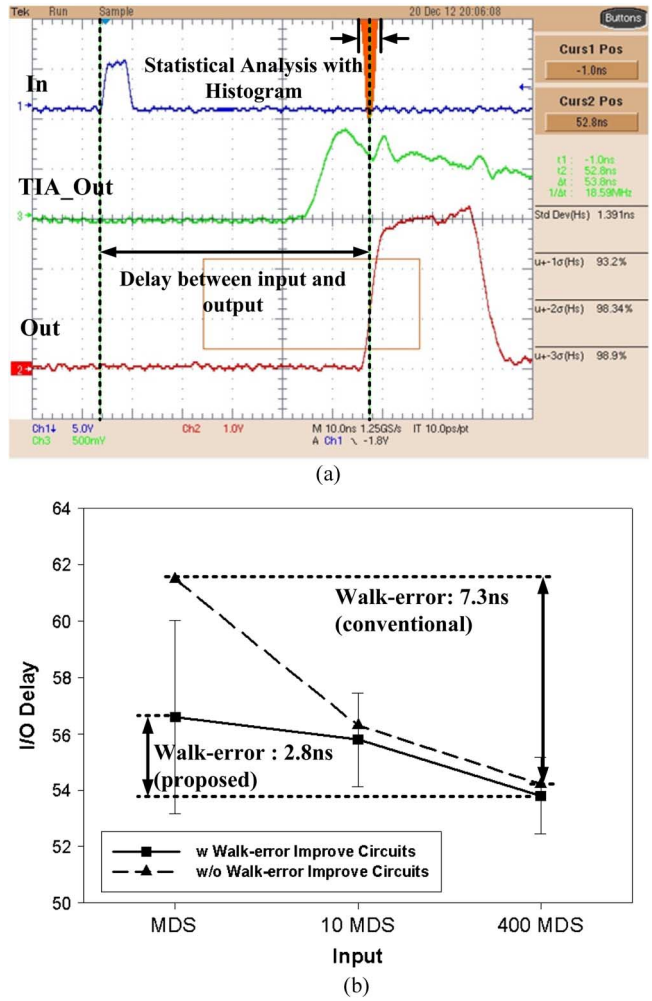


Fig. 18. Walk-error measurement: (a) input/output waveform and (b) I/O delay vs. the input power.

is only 20 dB, the APD leakage current increases with increase in input power, driving the first amplifier of the TIA into improper bias. However, in real situation, such a large amount of APD leakage current does not occur. Therefore, assuming that the extinction ratio is high enough and TIA operates similarly both in the high and low gain modes, the total dynamic range of the receiver can be estimated as 1 to $400 \times 30 = 12\,000$.

Fig. 18 shows the measured input/output waveforms and I/O delay vs. input power of the proposed optical receiver. In Fig. 18(a), the walk error is measured in an in-direct way by measuring the I/O delay differences for three different levels of input powers. In the I/O delay, even though the timing errors are added by the jitter of the optical input, the circuit timing delay difference from the input to the output, and the nonlinearity related to the TIA, Fig. 18(b) shows a clear improvement of maximum walk error, represented by the reduction from 7.3 ns to 2.8 ns for input of MDS to 400 MDS. Moreover, the simulation results show that when the rise time of the laser increases from 100 ps to 2 ns which is long enough for 5 ns optical pulse, only 0.4 ns increases in the walk-error. Therefore, it implies that the effect of the rise time of the laser pulse to the walk error is negligible. Since the receiver is targeted for military application for the range detection of a few km where the required accuracy is normally a few meters [10]. The walk error of 2.8 ns, which corresponds to the timing error of 42 cm, is acceptable.

TABLE I
RECEIVER PERFORMANCE COMPARISON

		This Work	[15]	[16]	[17]	[23]
Type		Integrated	Integrated	Integrated	Integrated	Hybrid
Technology		CMOS 0.35μm	BiCMOS 0.35μm	BiCMOS 0.35μm	CMOS 0.13 μm	NA
PD	Type	InGaAs APD	Si APD	Si APD	Si APD	InGaAs APD
	C_{PD}	2.5-5pF	1.5pF	1.5pF	1.5pF	< 5pF
	Wavelength	1550nm	NA	NA	NA	1550nm
Pulse Specification		5ns	6ns	3ns	3ns	10-28ns
Power Consumption		79mW	220mW	115mW	45mW	420mW
Bandwidth		160MHz	200MHz	230MHz	300MHz	NA
Input Referred Noise		1.36pA/√Hz	9.2pA/√Hz	3.29pA/√Hz	5.48pA/√Hz	NA
Current MDS (SNR=3.3)		53nA	430nA	330nA	330nA	NA
Optical MDS (SNR=3.3)		10.6nW	NA	NA	NA	20nW @10ns pulse 8nW @28ns pulse
Gain Control		1:30 Dual Gain	NA	NA	NA	1:25 TPG
Dynamic Range		1:12,000	1:2750	1:100,000	1:10,000	1:100,000
Walk Error		±1.1 - 1.4ns	± 55ps	± 15ps	±37ps	NA
Multiple Target Resolution		50ns (7.5m) @ 400nW	NA	NA	NA	67ns (10m) @ 50nW
Operating Temperature		-40 ~ +85 °C	-20 ~ +50°C	-10 ~ +50°C	-10 ~ +70°C	-45 ~ +85°C
Output		TTL/CMOS Digital Duration ~20ns	NA	NA	NA	TTL/CMOS Digital Duration ~40ns

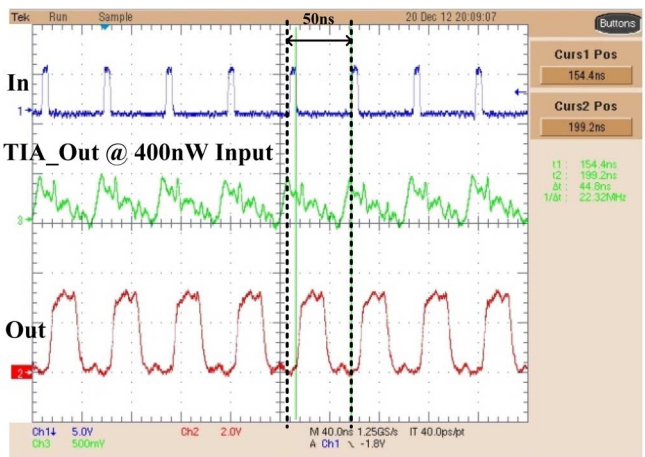


Fig. 19. Multi-target resolution measurement of the proposed LADAR receiver.

The TIA output voltage is actually measured after a buffer for the purposed of optical alignment. Due to the slow response of the buffer, measuring the multi-target resolution using the recovery time of the integrated signal becomes ineffective. Instead, the multi-target resolution is measured by measuring the maximum input power with a certain input period, 50 ns, as shown in Fig. 19. With input signal of 50 ns period, the maximum input power for which the output follows the input period is measured as 400 nW. In other words, when the input power exceeds 400 nW with a 50 ns period, the period of the output signal becomes wider than 50 ns which indicates that the multiple target resolution is higher than 50 ns and target detection is missed.

For the temperature variation of -40 °C to 85 °C, the noise and MDS varies only less than 5% while the walk error varies about 25% from 2.2 ns to 2.8 ns. In addition, the multi-target resolution varies about 15%.

Table I shows the performance summary of the proposed LADAR receiver in comparison with a recently publish works which are for few tens of meter detection [15]–[17] and an existing commercial product available for 30 m–2 km range detection [23]. As shown in the Table I, though the proposed LADAR receiver is implemented in a 0.35 μm CMOS technology which has a cost advantage compared to BiCMOS, 0.13 μm CMOS or hybrid type technology, yet it shows comparable performances. As shown in Table I, the proposed LADAR receiver consumes lower power, achieves lower MDS and lower noise than others. Since [15]–[17] are designed for tens of meter range detection which prefer SNR as 10 or 20, the MDS is normalized with SNR of 3.3 for the right comparison. In addition, the multiple target resolution of the proposed LADAR receiver is also shorter than that of [23]. The walk error of the proposed receiver is 2.8 ns (±1.4 ns) which is higher than [15]–[17], however, it is reasonable for the km range detection. If the MDS is set with SNR of 10 or higher by changing the threshold voltages of the comparators, the walk error can be reduced down to less than ±1 ns.

IV. CONCLUSION

An integrated pulsed TOF LADAR receiver for military application with high sensitivity and low walk-error has been proposed and implemented in a 0.35 μm CMOS technology. The measurement results have confirmed the performances of the proposed LADAR receiver with MDS of 10.6 nW with 5 ns pulse at SNR $=$ 3.3, 2.8 ns of maximum walk-error, and 1:12,000 of total dynamic range over -40 °C to $+85$ °C of operating temperature which fully satisfies the requirement of application.

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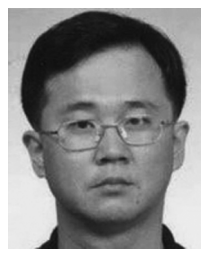

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