A 5.8-GHz DSRC Transceiver With a 10-μA Interference-Aware Wake-Up Receiver for the Chinese ETCS

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***Abstract*—This paper presents a fully integrated 5.8-GHz dedicated short-range communication transceiver with a 10-μA interference-aware wake-up receiver (WuRx) for Chinese electronic toll collection system terminals that can operate with a low standby and operating current consumption. To reduce the current consumption, a high-gain RF envelope detector using a voltage-boosting method is proposed for both the WuRx and receiver (Rx) while the proposed high-power ASK modulator extends output dynamic range in low power consumption. Additionally, a delay-based bandpass filter is adopted in the WuRx to filter out interference from automotive applications, thus increasing the battery lifetime by reducing the probability of a false wake-up. The proposed transceiver is fabricated using 0.13-μm CMOS technology with a chip size of 2.8 mm^2 for the target frequency range of 5.8 GHz. The measured results demonstrate sensitivities of -44 and -61 dBm for the WuRx and Rx, dissipating currents of 10 μA and 19 mA from 3.3-V supply voltage, respectively. The transmitter exhibits a normal output power of $+5$ dBm at an operating current of 46 mA.**

***Index Terms*—CMOS integrated circuits (ICs), dedicated short-range communication (DSRC), electronic toll collection system (ETCS), interference suppression, radio transceiver, wake-up receiver (WuRx).**

I. Introduction

RECENTLY, an electronic toll collection system (ETCS) has become a widely used communication system in automotive vehicles. The ETCS uses 5.8-GHz dedicated short-range communication (DSRC) channels, which provides a high-speed radio communication link between an on-board unit (OBU) and a roadside unit (RSU). In a Chinese national standard [1], a wake-up receiver (WuRx) is mandated due to the battery powered OBU, as seen in Fig. 1. Therefore, the DSRC transceiver presented in the authors' prior work [2] cannot be used in the Chinese OBU because of its high current dissipation of approximately 150 mA and the absence of a WuRx, although it has excellent performance. Besides, the receiver (Rx) should be able to receive both 5.83- and 5.84-GHz channels. Accordingly, the frequency conversion structure [3] is less preferred than the envelope-detector-based one since power-hungry phase-locked loop (PLL) and automatic channel scanning circuits [4] are indispensable for two-channel reception. Most of the WuRx's have been implemented with a simple RF envelope detector (RFED) using Schottky diodes [5], [6] or MOSFETs operating in the weak-inversion region [7]. However, these WuRx's neither filter out the interferers, nor amplify the input signal, thus being vulnerable to high-power interferences originating from mobile phones and WiFi devices. Although a number of works for Chinese DSRC transceivers have been reported [8]–[11], none of them provides a solution for high-power interferers and false wake-up problems. In addition, previous works show other problems that need to be resolved, such as poor wake-up [8], Rx sensitivities [9] not meeting the Chinese standard, or too much operating current in the linear power amplifier (PA) of the OBU [10]. Thus far, there have been no reports for fully integrated ETCS transceiver chips, except the authors' prior work [12].

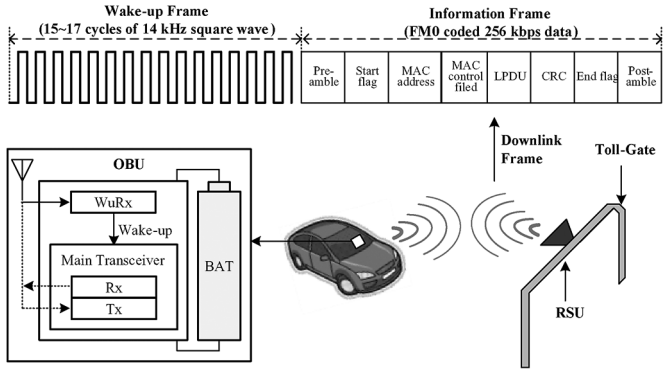

Fig. 1. DSRC system and the downlink frame structure of the Chinese ETCS.

This paper presents a fully integrated low-current CMOS transceiver with a WuRx that satisfies all specifications of the Chinese ETCS. In the proposed transceiver, a high-gain RFED is proposed for the signal-to-noise ratio (SNR) improvement

Manuscript received January 30, 2014; revised May 23, 2014, July 23, 2014, and September 21, 2014; accepted September 28, 2014. Date of publication October 22, 2014; date of current version December 02, 2014. This work was supported by the Center for Integrated Smart Sensors funded by the Korean Ministry of Science, ICT and Future Planning as Global Frontier Project (CISS-2012M3A6A6054195).

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Digital Object Identifier 10.1109/TMTT.2014.2362118

TABLE I
PARAMETERS FOR THE BATTERY LIFETIME CALCULATION

Symbol	Description	Value
Q	Battery capacity	1,000 mAH
T_L	Required lifetime (5 years)	43,800 H
N_t	Number of transactions (5 years)	18,250
T_t	Transaction time	0.3 s
T_{up}	Uplink time	0.2 T_t
T_{dn}	Downlink time	0.8 T_t
I_{stby}	Current in standby mode	0.022 mA
I_{up}	Current in uplink	50 mA
I_{dn}	Current in downlink	30 mA
N_{tf}	Number of false wake-ups (3.4 years)	1,253,502
T_{tf}	Receiver on-time when false wake-up occurs	0.1 T_t
T_{Lf}	Lifetime when false wake-up occurs (3.4 years)	30,084 H

in both WuRx and Rx while the proposed high-power ASK modulator saves power consumption in the transmitter (Tx) without a loss of dynamic range. Moreover, the proposed low-power delay-based bandpass filter (DBPF) substitutes for the conventional *RC* filter in the WuRx and eventually leads to the sharp interference filtering without external surface acoustic wave (SAW) filters.

This paper is organized as follows. In Section II, WuRx design issues in the Chinese ETCS is discussed for better understanding. Section III describes the proposed transceiver architecture. Section IV describes the implementation details of the proposed transceiver. Section V summarizes the measured performance of the implemented transceiver in comparison with previous works and Section VI concludes this paper.

II. WuRx DESIGN ISSUES FOR THE CHINESE ETCS

A. Standby Current in WuRx

The average maintenance time of a Chinese ETCS terminal is expected to be longer than two years assuming ten transactions per day [13]. However, since the commercially required maintenance period is typically five years with a 1000–2000-mAH 3.6-V lithium-ion battery, the low-power WuRx implementation is a critical issue for DSRC system design. The required standby current of an OBU is given by

$$I_{\mathrm{stby}} = \frac{Q - (I_{\mathrm{up}}T_{\mathrm{up}} + I_{\mathrm{dn}}T_{\mathrm{dn}})N_t}{T_L - T_tN_t} \tag{1}$$

where the parameters are defined in Table I. From (1), the standby current can be calculated to be approximately 22 μA for the 1000-mAH battery. Using the typical values for the battery-lifetime calculation parameters in Table I, the total estimated transaction time is only approximately 1.5 h during the five-year period, which corresponds to 0.003% of the lifetime. It means that the standby current consumption in the WuRx directly determines the battery lifetime.

B. False Wake-Up

In addition to low standby current in the WuRx, we need to reduce the false wake-up probability. The false wake-ups occur when various interferences, as seen in Fig. 2, are not filtered out enough and wrongly wake up the Rx. Since the Rx has extremely higher current consumption than that of the WuRx, increasing false wake-ups definitely reduce the battery lifetime. The battery lifetime including a false wake-up is expressed as

$$T_{Lf} = \frac{Q - (I_{\mathrm{up}}T_{\mathrm{up}} + I_{\mathrm{dn}}T_{\mathrm{dn}})N_t - I_{\mathrm{dn}}T_{tf}N_{tf}}{I_{\mathrm{stby}}} + T_tN_t + T_{tf}N_{tf} \tag{2}$$

where the parameters are defined in Table I. From (2), the battery lifetime will decrease by approximately 31.4% if there are 1000 false wake-ups per day. Thus, in addition to the reduction in the standby-mode current, the false wake-ups should be minimized to increase the battery lifetime.

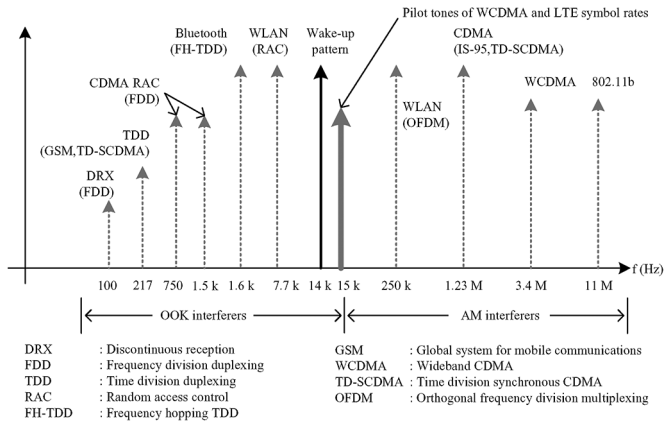

Fig. 2. Frequency distribution of the AM/OOK interferers.

According to [14], the power level of the interferer to avoid a false wake-up of the OBU should be below approximately 0 dBm. However, the power levels of the interferers from wireless local are networks (WLANs), mobile phones, and Bluetooth reaches up to +13 dBm [15] near the OBU. These interferers are transmitted as signals with amplitude variations based on two different mechanisms: an AM signal caused by the peak-to-average power ratio (PAPR) in active-mode operation and an on–off-keying (OOK) signal caused by their time-division transmit–receive operation. An in-depth analysis for the amplitude variations for various wireless communication systems is described in [16]–[23] and the frequency distribution of the AM/OOK interferers are graphically summarized in Fig. 2. Unfortunately, the pilot tones in a code division multiple access (CDMA) system and the symbol rate of the long-term evolution (LTE) system have a 15-kHz envelope signal, which is too close to be filtered from the 14-kHz wake-up pattern of the Chinese ETCS. Hence, false wake-up reduction methods should be adopted in the WuRx of the Chinese ETCS terminal in order to protect the OBU from interferers.

C. Offset Voltage and Noise Versus Required Minimum SNR

In the Chinese DSRC standard, FM0 [1] is used for data encoding. Since forward error correction (FEC) is not applied in FM0 modulation, the errors at comparator output directly degrades the system bit error ratio (BER). That is, the noise and offset voltage at the input of the comparator can trigger the comparator and eventually leads to false wake-ups. Thus, the com-

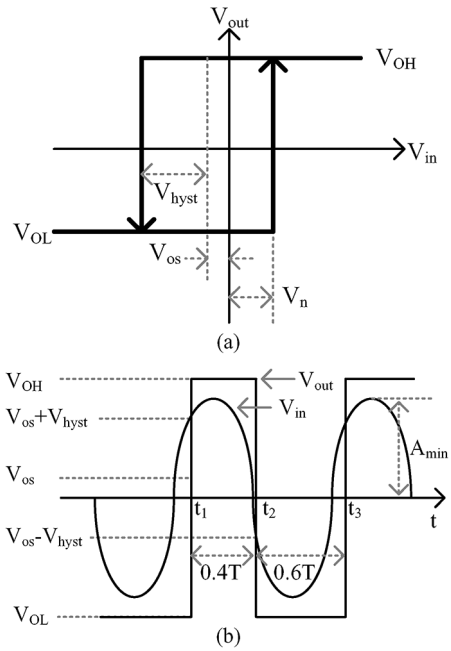

Fig. 3. Transfer characteristics of a hysteresis comparator with noise, offset voltages, and output duty requirement. (a) Comparator transfer characteristics including the effects of offset and noise voltages. (b) Example of comparator output waveform for a sinusoidal input under noise and offset voltages when the duty of the output signal is 40%–60%.

parator should be designed in a hysteresis structure in order to be insusceptible to both noise and offset voltage. Fig. 3(a) illustrates the comparator transfer characteristics including the effects of the offset ($V_{\rm os}$) and noise voltages (V_n). The hysteresis voltage $V_{\rm hyst}$ of the comparator should be greater than the sum of the input noise and offset voltages caused by device mismatches, as given by

$$V_{\rm hyst} > V_n + V_{\rm os} = |\mu_{\rm os}| + \alpha\sqrt{\sigma_n^2 + \sigma_{\rm os}^2} \tag{3}$$

where σ_n is the noise voltage, $\mu_{\rm os}$ is the average offset voltage, and $\sigma_{\rm os}$ is the standard deviation of the offset voltage. For an error rate of 10^{-5}, required in the Chinese National Standard, the coefficient α should be approximately 4.27. $V_{\rm hyst}$, $V_{\rm os}$, and V_n should be determined based on this value and (3).

Meanwhile, the duty requirements in common ASK demodulators are 40%–60% even though the permissible duty ratio depends on the modem performance. Fig. 3(b) shows an example of the comparator output waveform for a sinusoidal input along with the noise and offset voltages when the duty of the output signal is 40%–60%. Assuming that a sinusoidal signal ($V_{\rm in}$) at the input of comparator is given by $v_{\rm in}(t) = A\sin(2\pi ft)$, as shown in Fig. 3(b), the minimum voltage magnitude $A_{\rm min}$ of the comparator input to meet the duty requirement of the output $V_{\rm out}$ can be estimated as

$$A_{\rm min} = (V_n + 2V_{\rm os}) \times\sqrt{1+\left(\frac{1-\cos 0.8\pi}{\sin 0.8\pi} - \frac{2(V_n+V_{\rm os})}{\sin 0.8\pi(V_n+2V_{\rm os})}\right)^2} \tag{4}$$

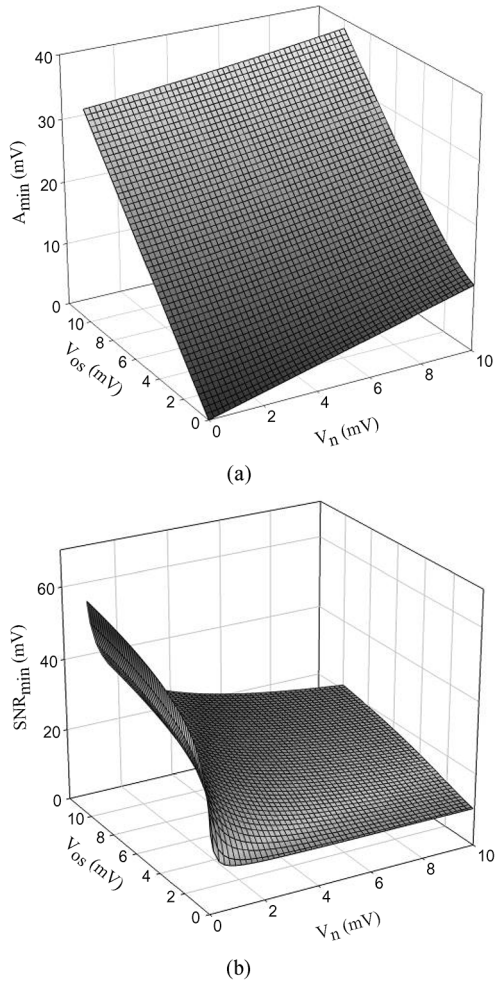

Fig. 4. Graphical representation of the minimum input level and the minimum required SNR of the comparator to meet the 40% and 60% duty. (a) Minimum input level of the comparator. (b) SNR requirement.

where the cosine and sine terms are derived from the 40%–60% duty requirement. The offset voltages from the preceding blocks can be removed by the dynamic referencing of the comparator [12]. Therefore, considering that the offset voltage effect has already been applied to (4), the minimum required SNR of the comparator, $\rm SNR_{min}$, is expressed as

$$\mathrm{SNR_{min}} = \frac{1}{2}\frac{(V_n+2V_{\rm os})^2}{V_n^2} \times\left[1+\left(\frac{1-\cos 0.8\pi}{\sin 0.8\pi} - \frac{2}{\sin 0.8\pi}\frac{V_n+V_{\rm os}}{V_n+2V_{\rm os}}\right)^2\right]. \tag{5}$$

Fig. 4 shows $A_{\rm min}$ and $\rm SNR_{min}$ of the comparator versus $V_{\rm os}$ and V_n to meet the 40%–60% duty requirements. As seen in Fig. 4(a) and (b), $A_{\rm min}$ increases more rapidly with an increase in $V_{\rm os}$ than V_n while $\rm SNR_{min}$ remains nearly constant regardless of V_n for small $V_{\rm os}$ and gradually increases as $V_{\rm os}$ increases. In particular, $\rm SNR_{min}$ increases drastically when $V_{\rm os}$ becomes larger than V_n. This reveals a remarkable fact that minimizing the ratio of $V_{\rm os}/V_n$ at the comparator input can significantly reduce the required $\rm SNR_{min}$ and it can directly results in high sensitivity of an ASK Rx.

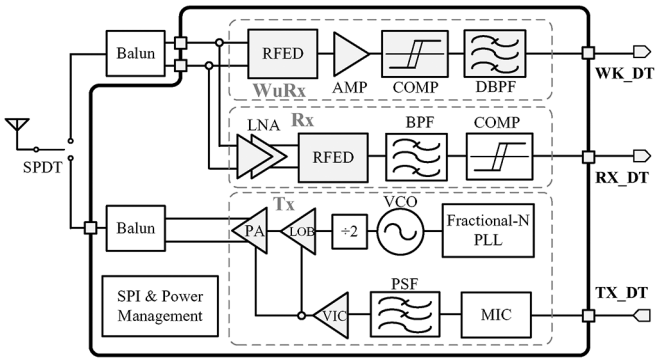

Fig. 5. Block diagram of the proposed DSRC transceiver for the Chinese ETCS.

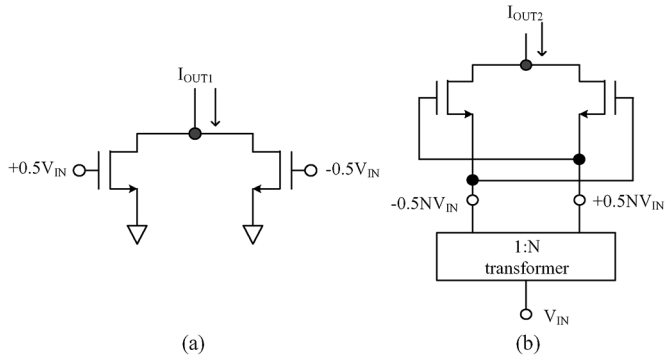

Fig. 6. RFEDs. (a) Conventional. (b) Proposed voltage boosted envelope detector.

III. Proposed Transceiver Architecture

Fig. 5 shows the block diagram of the proposed DSRC transceiver for the Chinese ETCS. The transceiver adopts an RFED architecture [3] for both the WuRx and Rx and a high-power ASK modulator with an adaptive local oscillator (LO) buffer for Tx [24], [25]. In WuRx and Rx, a high-gain RFED structure is proposed that helps to improve the system SNR without additional current consumption while the proposed DBPF effectively cuts out high-power interferences, leading to significant false wake-up reduction. The proposed high-power ASK modulator not only allows low-power Tx implementation, but also overcomes its inherent poor output dynamic range with an adaptive LO buffer.

In Fig. 5, the WuRx consists of an RFED, a baseband amplifier, a comparator with hysteresis acting as a 1-bit analog-to-digital converter (ADC), and a DBPF. A low-noise amplifier (LNA) is added to the Rx in order to improve the sensitivity in front of the RFED and the input ports of the WuRx and Rx are shared to accommodate a single antenna. An external transformer is adopted on the receive side after the antenna, which helps maximize the gain of the WuRx RFED for the given amount of current consumption. The Tx consists of a modulation index controller (MIC), a pulse-shaping filter (PSF), a voltage-to-current converter (VIC), a PA acting as a high-power ASK modulator, and a fractional-N PLL with a voltage-controlled oscillator (VCO).

IV. Circuit Design

In this section, the circuit-implementation details of the proposed 5.8-GHz DSRC transceiver in Fig. 5 are described. The designs of the RFED, hysteresis comparator, and DBPF for the WuRx path are explained in detail. The designs of the two-stage LNA and RFED for the Rx path are also presented. With the Tx path, the design details of the VIC and the high-power ASK modulator with an adaptively biased LO buffer are described.

A. WuRx

1) RFED: In general, MOSFETs in the weak-inversion regime have been used for RFEDs implemented in CMOS technology. However, they tend to offer poorer sensitivity at high operating frequencies compared to Schottky-diode-based implementations owing to their relatively low gain and high output noise [8]. The proposed voltage-boosted RFED allows high gain, and thus high sensitivity of the WuRx utilizing a transformer without extra current consumption. Fig. 6 shows schematics of the conventional and proposed RFEDs. With the conventional CMOS envelope detector in Fig. 6(a), the output current I_{OUT1} is proportional to the square of the input voltage because it uses the even-order distortion property of the transconductance and is approximately expressed as

$$I_{\mathrm{OUT1}} \propto \frac{\alpha_2}{2}(V_{\mathrm{IN}})^2 \tag{6}$$

where α_2 is the gain of the second-order nonlinear output, and V_{IN} is the magnitude of the input signal. Fig. 6(b) shows the proposed voltage-boosted envelope detector, where a cross-coupling $1:N$ turns-ratio external transformer is added in combination with a conventional RFED. In Fig. 6(b), the $1:N$ transformer is used for single-to-differential conversion and N-times amplification of the input voltage. The cross-coupled differential driving of the input signal doubles the amplitude at the gate source terminals of the input transistors, and the resulting output current I_{OUT2} is represented by

$$I_{\mathrm{OUT2}} \propto 2\alpha_2(NV_{\mathrm{IN}})^2 = 4N^2 I_{\mathrm{OUT1}}. \tag{7}$$

From (7), the envelope detector in Fig. 6(b) increases the gain by approximately $4N^2$ times compared to that of the conventional topology in Fig. 6(a) [26].

Fig. 7 shows the schematic of the proposed envelope detector including a baseband amplifier and its simulation results. In Fig. 7(a), an off-chip balun X1 with a turns ratio of $\sqrt{2}$ is used. C_1 is used for impedance matching between the transformer and the input port of the cross-coupled differential pair. The input transistors, M_1 and M_2, are cross-coupled via coupling capacitors, C_2 and C_3. Three parallel resonant circuits, $L_{m1}-C_{m1}$, $L_{m2}-C_{m2}$, and $L_{m3}-C_{m3}$, are adopted to reject the WCDMA signals of the 15-kHz pilot tones. For wider bandwidth and considering 5% tolerance in the component values that constitutes the trap circuits, the resonant frequency of $L_{m1}-C_{m1}$ is set to approximately 1.8 GHz, and the others ($L_{m2}-C_{m2}$ and $L_{m3}-C_{m3}$) are set to approximately 2.2 GHz with the component values of $L_{m1}=3.6$ nH, $C_{m1}=2$ pF, $L_{m2}=L_{m3}=2.1$ nH, and $C_{m2}=C_{m3}=2.2$ pF. Using these off-chip filtering circuits, WCDMA signals can be suppressed sufficiently. The cascode transistors, M_3 and M_4, are high-voltage devices adopted to protect M_1 and M_2 from the high battery supply

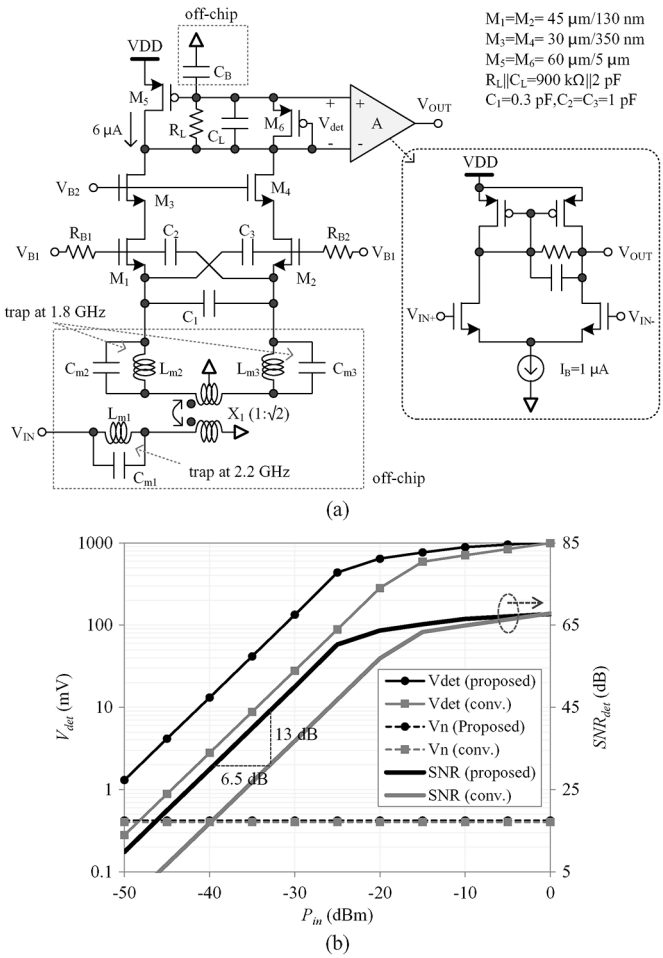

Fig. 7. Circuit implementation of the proposed RFED. (a) Circuit schematic. (b) Simulated output voltage, noise, and SNR of the proposed and conventional RFEDs.

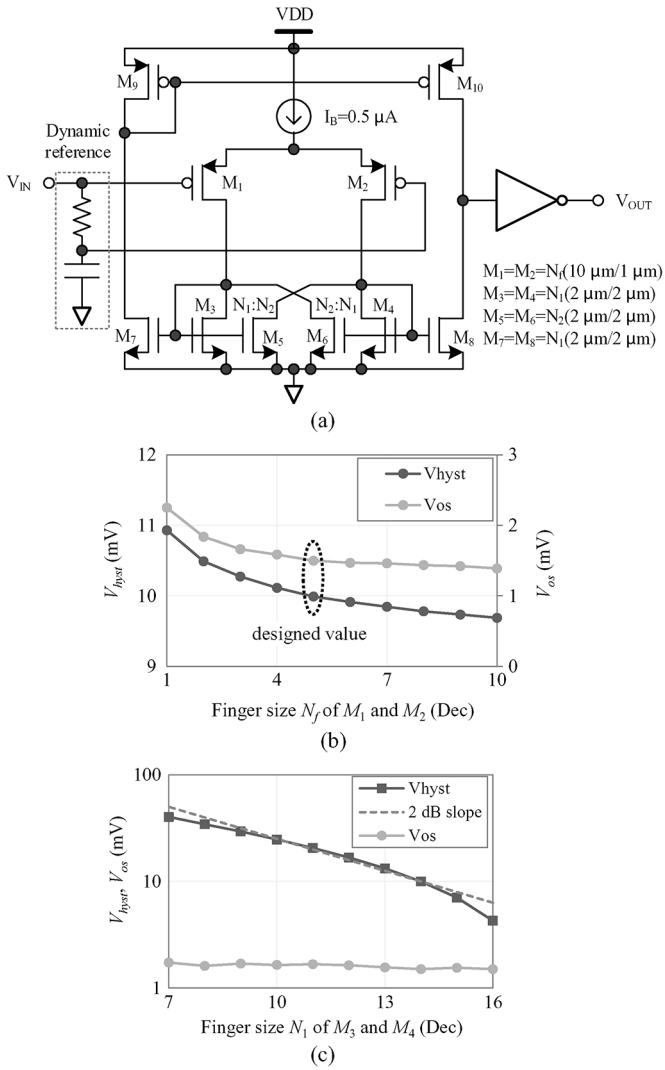

Fig. 8. Comparator circuit diagram for the WuRx. (a) Hysteresis comparator with positive feedback. (b) Optimization of offset voltage and (c) hysteresis voltage.

voltage of 3.6 V. In Fig. 7(a), the capacitor C_L connected in parallel with the load resistor R_L is adopted to suppress the high-frequency components at the output. M_5 and C_B stabilize the dc operating point while the diode-connected transistor M_6 limits the output voltage swing at high input power. The voltage conversion gain of the proposed RFED is given by [26]

$$A_{\mathrm{RFED}} \approx I_{\mathrm{DC}}(R_L \| R_{M6}) \frac{V_{\mathrm{IN}}}{(nV_T)^2} \tag{8}$$

where n is the subthreshold slope factor, V_T is the thermal voltage (kT/q), I_{DC} is the bias current of the input transistors, and R_{M6} is the resistance of the voltage-limiting transistor M_6. In Fig. 7(a), amplifier A is inserted at the RFED output in order to reduce the sensitivity degradation effect caused by the offset voltage of the following comparator block. Fig. 7(b) shows the simulated output and noise voltage of the conventional and proposed RFEDs. The output SNR of the proposed RFED increases by 13 dB compared to the conventional one, which is lower than the theoretically estimated value of 18 dB $(4N^2 = 8)$ in (7) due to power loss of the transformer and matching circuits.

2) Comparator: Fig. 8(a) shows a circuit schematic of the hysteresis comparator used in the WuRx. The negative input node is dynamically referenced through an *R–C* filter, which has a value of 1 MΩ and 100 pF, respectively. The size of the input transistors M_1 and M_2 and the overdrive voltages of the current mirrors composed of the M_3–M_5 and M_4–M_6 pairs are increased to minimize the offset voltage. Fig. 8(b) shows the simulation results for the hysteresis and offset voltages of the comparator according to the size of the input transistor pair. Although offset voltage decreases as the finger size N_f increases, N_f is selected to 5 considering the chip size. Variations of V_{hyst} according to the size of the M_3–M_5 and $M_4 - M_6$ pairs are shown in Fig. 8(c). As the output voltage of the RFED is proportional to the square of the input voltage, as seen in (8), N_1 and N_2 are selected to have approximately 2-dB slope of V_{hyst} in log scale. V_{hyst} has an average value of 10 mV and a standard deviation of 1.5 mV when $N_1 = 14$ and $N_2 = 18$, and can be adjusted by changing N_1 to meet (3) via digital control switches [control switches are omitted in Fig. 8(a)].

3) DBPF: An RF SAW filter in front of the RFED [7] is inappropriate for WuRx due to its insertion loss and high material cost. A correlation technique [7] requires a high design complexity and leads to high latency. A narrowband BPF after the

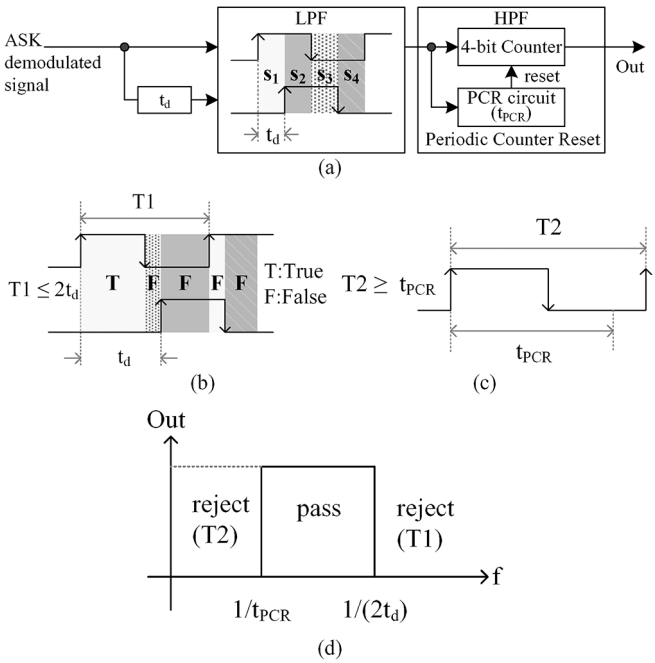

Fig. 9. Delay-based BPF concept. (a) Conceptual block diagram and (b) the timing diagram of the state machine when the period of input signal T_1 is shorter than $2t_d$. (c) Timing diagram of the PCR circuit when the period of input signal T_2 is larger than the $t_{\rm PCR}$. (d) Cutoff frequency of the DBPF.

RFED [6] usually implemented by the passive *RC*-based filter, which tends to exhibit poor selectivity owing to the low-current requirement. To overcome these limitations, a low-current high-selectivity DBPF is proposed without using conventional high-current filters such as analog active or digital filters.

Fig. 9(a) shows the basic concept of a DBPF. The proposed DBPF is composed of a low-pass filter (LPF) and high-pass filter (HPF) in cascade that adopts a time delay t_d for the demodulated wake-up signal. In Fig. 9(a), the input signal and its delayed signal in the LPF have four unique states: $s_{1(1,0)}$, $s_{2(1,1)}$, $s_{3(0,1)}$, and $s_{4(0,0)}$. As seen in Fig. 9(b), since the four states are not defined properly if the period of the input signal T_1 is shorter than $2t_d$, the input signal cannot be delivered to the output, but be filtered out by the state machine. It means that the interference from frequencies higher than $1/(2t_d)$ can be removed effectively. The HPF in Fig. 9(a), which generates an interrupt signal using a 4-bit asynchronous counter, is reset periodically by the time constant $t_{\rm PCR}$ of the periodic counter reset (PCR) circuit. Thereby, as shown in Fig. 9(c), interference will be rejected by the reset operation when the frequency of the interference $1/T2$ is lower than $1/t_{\rm PCR}$. Fig. 9(d) shows that the cutoff frequency of the DBPF is determined by both the time delay and time constant of the PCR circuit. Finally, the AM/OOK interferers, except 15-kHz envelope signals in Fig. 2, can be removed by choosing appropriate values of t_d and $t_{\rm PCR}$. The LTE and WCDMA signals can be suppressed by simple L–C trap circuits in the matching network because their RF frequencies are far from those of the Chinese ETCS.

More importantly, the counter in the DBPF can reduce the occurrence of a false wake-up in the presence of unstable input signals such as glitches that can occur by the noise and interference near the sensitivity level. The number of false wake-ups from LTE signals can also decrease as the counter value increases because the occurrence probability of consecutive 15-kHz envelope signals [14] is lower than that of a nonconsecutive one. Therefore, there is a tradeoff between the wake-up time and the error rate, and it is desirable that the counter should be set to as low value as possible unless a false wake-up is a problem.

In Fig. 9(a), the LPF is composed of a delay block, state machines, edge detectors, and combinational logic gates. Fig. 10 shows the implementation details of the LPF. In Fig. 10(a), the delay block consists of eight delay cells implemented with capacitively loaded inverters. Inverting buffers are inserted between the delay cells for sufficient drive of the subsequent blocks. Fig. 10(b) shows a schematic of the state machine that defines the four unique states for LPF operation. In Fig. 10(b), each state is stored in the data flip-flop (DFF) at the rising or falling edge of both input and time-delayed input signals via the delay cell. If all four states are "TRUE," the output $y(t)$ goes to "HIGH." However, $y(t)$ drops to "LOW" if any one of the four states are "FALSE," rejecting the input signal. Unfortunately, $y(t)$ of the state machine exhibits a periodic frequency response as the four unique states are defined properly and also repeated with an increase in the input-signal frequency. Fig. 10(c) shows the frequency response of the state machine. In Fig. 10(c), the input signal with a period of t_d to 2_{td} will generate a rejected signal at the output, whereas signals with a period of 0.75 t_d to t_d and a period greater than $2t_d$ generate a pass signal at the output. These operations repeat with a period of $1/t_d$. To remove this periodic frequency response of the first-order LPF, two more state machines with a half and quarter period of delay ($0.5t_d$ and $0.25t_d$) are added in the LPF [$SM2$ and $SM3$ blocks of the third-order LPF in Fig. 10(d)]. Although the additional two state machines have similar frequency response as that of the first-order LPF with periods of $t_d/2$ and $t_d/4$, the composite frequency responses of the three state machines in combination with the delay cell provide third-order LPF frequency characteristics, as shown in Fig. 10(e).

Fig. 11 shows the circuit schematic and operational timing diagram of the HPF [see Fig. 9(a)]. In Fig. 11(a), the counter block of the HPF is periodically reset by the PCR circuit, which is charged and discharged at the rising edge of the input and delayed signals, respectively. If the voltage $V_{\rm PCR}$ reaches up to half of the supply voltage, i.e., the logic threshold of the inverter, the counter will be reset. In Fig. 11(b), the reset time $t_{\rm PCR}$ is approximately 0.7 times the RC time constant, which defines the cutoff frequency of the HPF

$$f_{\rm HPF} = \frac{1}{t_d + t_{\rm PCR}} = \frac{1}{t_d + 0.7RC}. \tag{9}$$

The value of t_d has a strong dependence on process, voltage, and temperature (PVT) variations up to +44%, as shown in Fig. 12. Fortunately, there are no interference signals over the frequency range of 15–250 kHz, except the WCDMA and LTE signals, as shown in Fig. 2; thus, the delay calibration circuits can be omitted. In this work, the nominal cutoff frequency of the LPF and HPF are set to approximately 30 and 10 kHz, respectively, considering PVT variations. In Fig. 12, the effects of PVT variations on the cutoff frequency of the HPF is about ±4%, and

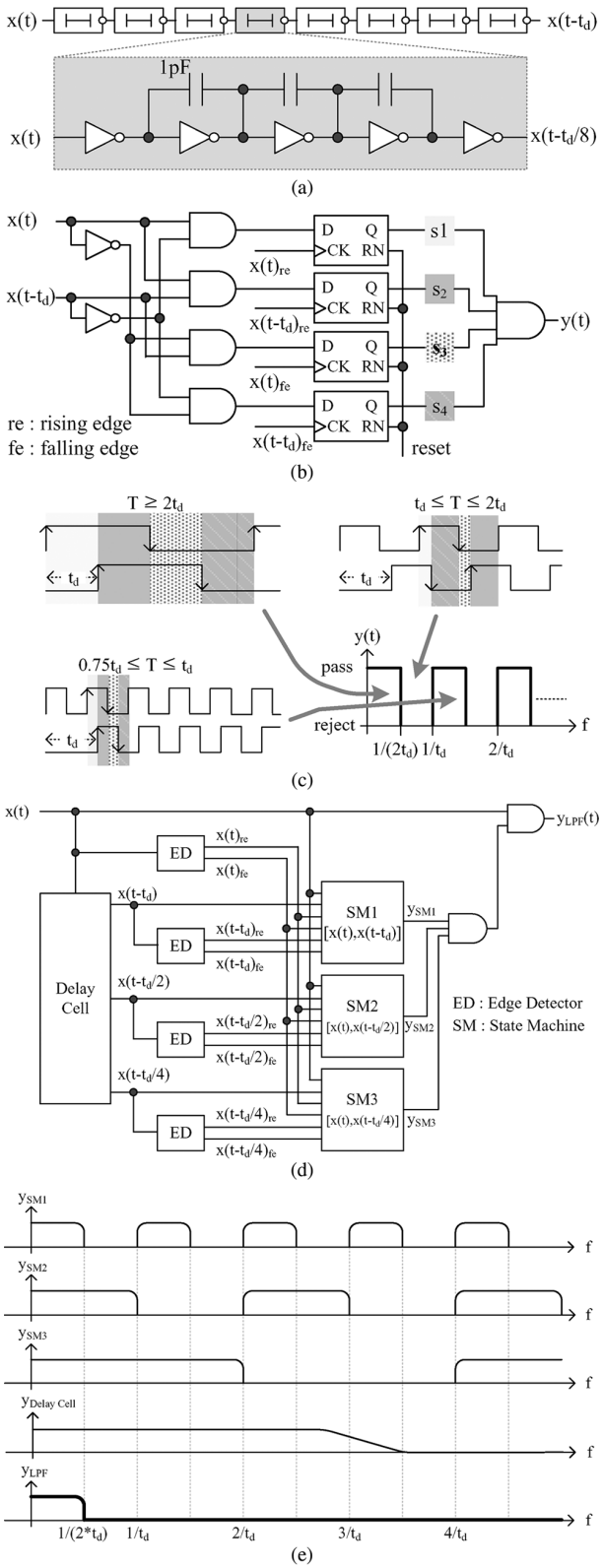

Fig. 10. Delay-based LPF implementation details. (a) Delay cell, (b) state machine, (c) frequency response of the state machine, (d) third-order LPF block diagram, and (e) estimated frequency response of the third-order LPF.

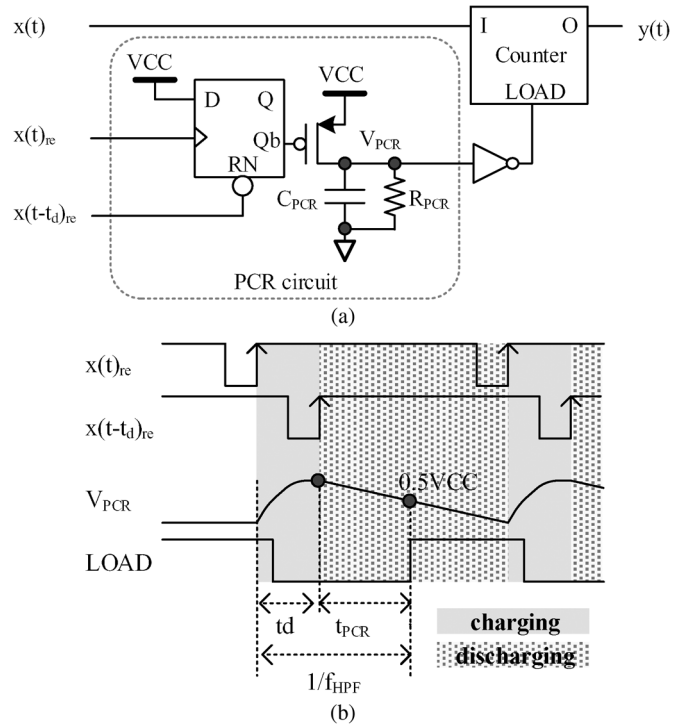

Fig. 11. Delay-based HPF. (a) Circuit schematic and (b) operating waveform.

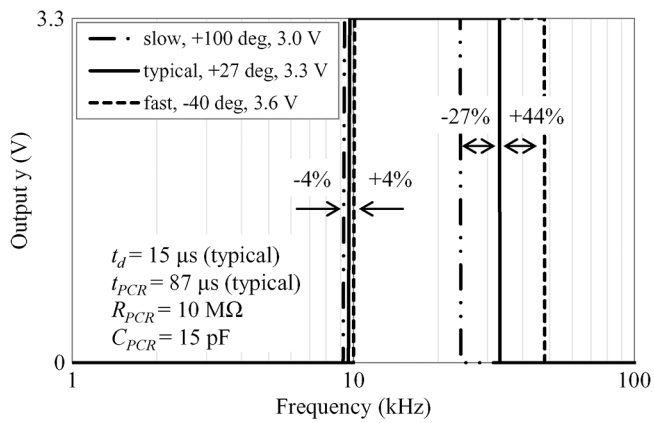

Fig. 12. Simulation results of the DBPF with process (typical, slow, fast), temperature ($-40\ ^\circ\mathrm{C} \sim +100\ ^\circ\mathrm{C}$), and voltage ($3 \sim 3.6$ V) variations.

can be negligible because t_{PCR} can be set stably using high-precision external components and is also sufficiently greater than t_d. The proposed DBPF dissipates very little standby current because it consists of only standard logic gates and passive devices.

B. Rx

Fig. 13 shows a circuit schematic of the RF front-end for the Rx in which a two-stage differential LNA with *LC*-tuned loads is placed in front of the RFED to increase sensitivity. The LNA is designed for a gain and noise figure of 20 and 5.5 dB, respectively. The RFED is implemented by p-channel MOSFETs, and the input transistors are cross-coupled for voltage boosting. Similar to the RFED in Fig. 7(a), the load consists of a dc feedback, an RC filter, and a voltage limiter using a diode-connected transistor. The subsequent analog baseband blocks for the Rx consist of a BPF and comparator, as shown in Fig. 5. The Rx BPF is implemented as a capacitively coupled second-order Butterworth LPF that has a 3-dB bandwidth of approximately

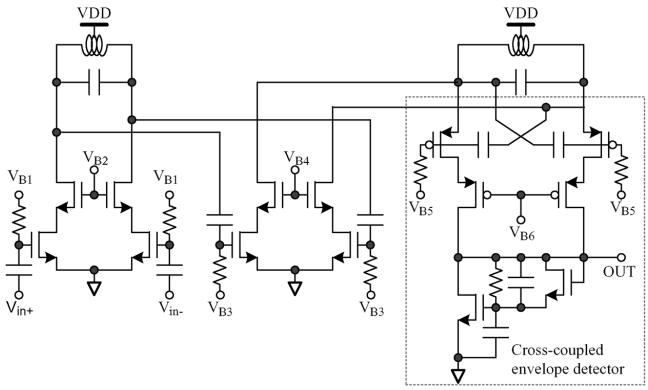

Fig. 13. Circuit schematic of the RF front-end for Rx path.

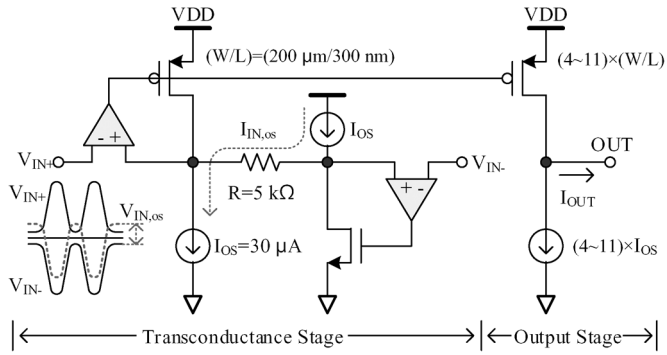

Fig. 14. Circuit schematic of VIC.

250 kHz. Further, a hysteresis comparator is designed to convert the detected envelope signal into digital bit streams.

C. Tx

The Tx consists of an MIC, a PSF, a VIC, a PA, and a fractional-N PLL, as shown in Fig. 5, and the 5.8-GHz LO signal propagates directly from the fractional-N PLL with an integrated third-order loop filter. Since the PA generates large RF switching noise that could induce frequency pulling on the VCO [27], the oscillator is designed to operate at 11.6 GHz and a frequency divider and an LO buffer are added. In the Tx, an FM0-encoded 1-bit data stream with a data rate of 512 kb/s is ASK modulated with a variable index between 0.5–1.0 and a step size of 0.5 through the MIC block. The bandwidth-controllable third-order Gaussian LPF is designed to adjust the bandwidth of the ASK-modulated transmit signal.

1) VIC: The VIC block converts the modulating voltage signal into current and sets the bias current of the adaptive LO buffer and PA via a mirroring operation. Fig. 14 shows a schematic of the VIC with a transconductance of $1/R$. Assuming an ideal ASK input signal, the positive input voltage $V_{\mathrm{IN}+}$ in Fig. 14 is always greater than the negative input voltage $V_{\mathrm{IN}-}$. However, the opposite condition may occur owing to nonideal effects such as the dc offset, resulting in abnormal operation. To guarantee proper VIC operation, i.e., to provide a path for the negative offset current $I_{\mathrm{IN,os}}$ caused by the negative offset voltage $V_{\mathrm{IN,os}}$, an intentional offset current I_{OS} is added to the transconductance stage. The same I_{OS} is also subtracted at the output stage because I_{OS} in the transconductance stage reduces the linear dynamic range of the output power by limiting the minimum power.

2) High-Power Adaptive-LO ASK Modulator: As seen in the Tx part of Fig. 5, we adopt a high-power ASK modulator structure to minimize the operating current consumption. However, the conventional high-power ASK modulator is not preferred for the Chinese ETCS due to its poor linear dynamic range: it requires ~26 dB of dynamic range in the Tx. In a conventional high-power ASK modulator, as shown in Fig. 15(a), large LO switching is desirable in the aspect of maximum output swing since it minimizes drain-to-source voltage V_{DS} of M_1. However, as seen in Fig. 15(a), the LO leakage at the output node, $V_{\mathrm{LO,leak}}$, affects the output power level when it is in the valley region and finally distorts the modulation index m of the output signals thereby limiting the dynamic range. In order to resolve this, an adaptive LO is applied for switching in the proposed PA where the envelope of the output signal is proportional to the amplitude of the modulating signal. Therefore, for large output, a large LO signal minimizes the turn-on resistance of M_1 to increase maximum available output, while for small output, a small LO signal minimizes the value of LO leakage at the output to avoid distortion in its valley region. Fig. 15(b) shows the output power versus ASK modulated input power in both the conventional and proposed PAs. As seen in Fig. 15(b), adoption of an adaptive LO signal can enlarge the output dynamic range of the PA from $(P_{1\mathrm{dB}} - P_{\min} - P_{VDS}, \mathrm{sat} - \mathrm{P_{LO,leak}})$ to $(P_{1\mathrm{dB}} - P_{\min})$, where $P_{1\mathrm{dB}}$, $P_{\min}$, $P_{VDS,\mathrm{sat}}$, and $P_{\mathrm{LO,leak}}$ are the 1-dB compression point of the PA, the valley power of the ASK-modulated output signal, the lossy power from $V_{\mathrm{DS,sat}}$, and the leakage power from $V_{\mathrm{LO,leak}}$, respectively.

Fig. 16 shows a schematic of the proposed PA with an adaptive LO buffer to increase the dynamic range [25], where the bias current $I_{\mathrm{MOD,LOB}}$ from the VIC enables the adaptive LO buffer to generate an output signal $V_{\mathrm{LO\_PA}}$ proportional to the modulating signal V_{MOD}. When V_{MOD} is very low, the $V_{\mathrm{LO\_PA}}$ remains at the minimum level, which drives the PA switches (M_3 and M_4) with minimum LO leakage at the PA output stage. As the amplitude of V_{MOD} increases, the $V_{\mathrm{LO\_PA}}$ also increases linearly, compensating the nonlinearity of the PA caused by the switching loss at a very high output power. The transistors M_1 and M_2 and the capacitor C_1 constitute a positive peak detector that generates the envelope signal $V_{\mathrm{LO\_}P}$ of the $V_{\mathrm{LO\_PA}}$ to enable accurate current mirroring of the PA. Further, the PA is also biased by a modulating current $K \cdot I_{\mathrm{MOD,PA}}$, which is provided from a current mirror with a size ratio of K. The core switching transistors M_3 and M_4 are 1.2-V nMOS transistors, considering the higher operating frequency. However, 3.3-V nMOS transistors are adopted for the cascode transistors M_5 and M_6 in order to fully utilize the supply voltage of 3.6 V while preventing unwanted breakdown. Since the fall time of node X determined by the transconductance $gm, M6$ and gate-to-source capacitance $Cgs, M6$ of M_6 is far slower than the rise time determined by the on-resistance $R_{\mathrm{on},M4}$ of M_4 and $Cgs, M6$, the maximum operating frequency $f_{\max}$ is approximately given by

$$f_{\max} \approx \frac{g_{m,M6}}{C_{\mathrm{gs},M6}} = f_{T,M6} \quad (= f_{T,M5}) < \frac{1}{T_{\mathrm{LO}}/2} \qquad (10)$$

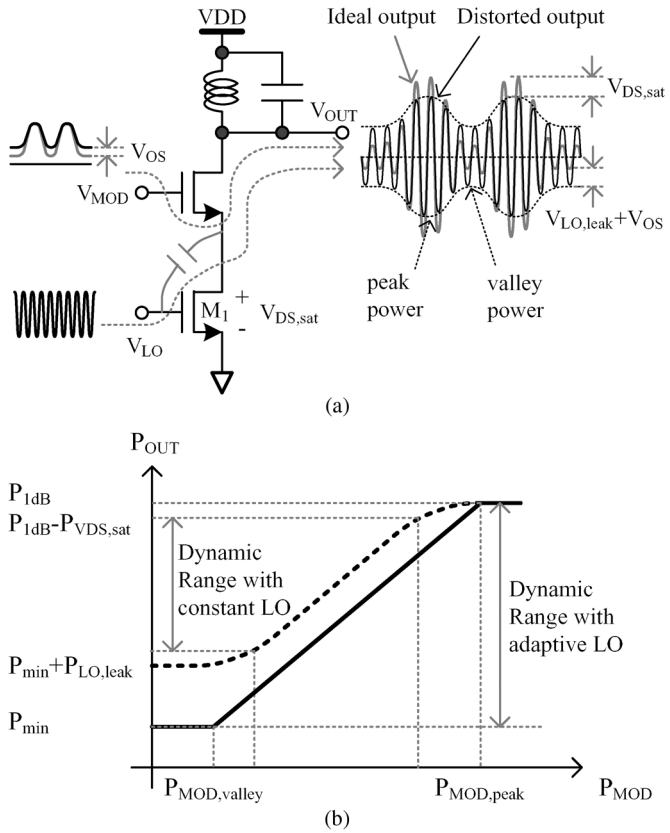

Fig. 15. A cConventional high-power ASK modulator. (a) Circuit schematic and (b) output power versus ASK modulated input power for constant and adaptive LO signals.

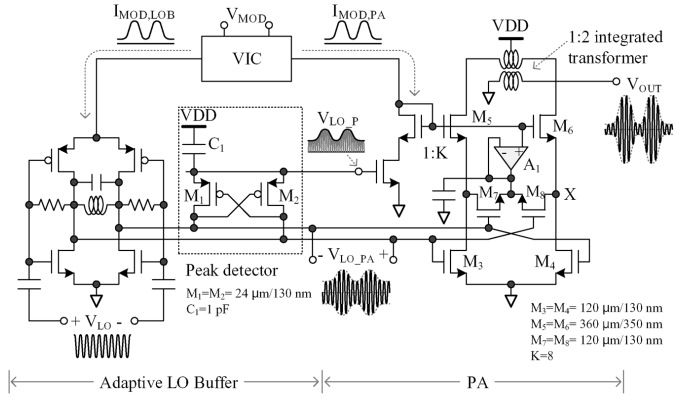

Fig. 16. Circuit schematic of the high-power ASK modulator with an adaptive LO buffer.

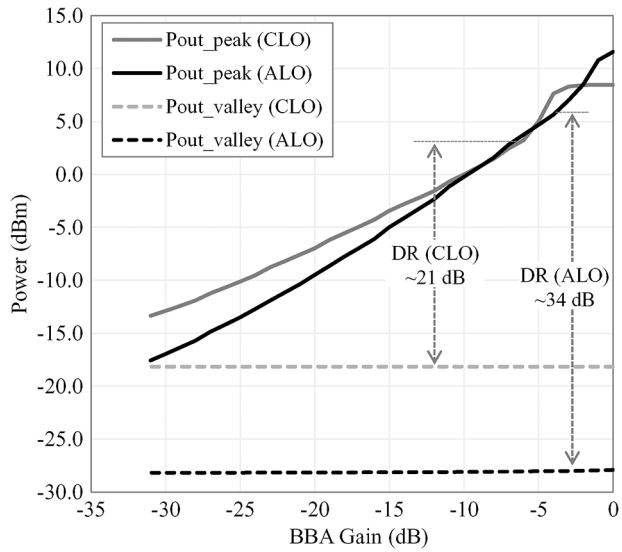

Fig. 17. Simulated output power dynamic range of the proposed PA with constant (CLO) and adaptive (ALO) LO buffers.

where $T_{\rm LO}$ is the period of the LO. To compensate for the lower switching speed of the cascode transistors, the switches M_7 and M_8 are added, which provide a faster discharge path from the source node of M_5 or M_6 to the common ground when either switch M_3 or M_4 is off. The enhanced maximum operating frequency $f'_{\rm max}$ is calculated as

$$f_{\rm max} \approx \frac{g_{m,M8}}{C_{{\rm gs},M6}} = \frac{g_{m,M8}}{g_{m,M6}} f_{T,M6} \approx 3 f_{T,M6} \qquad (11)$$

where $g_{m,M8}$ is the transconductance of M_8. With the adoption of M_7 and M_8, the maximum operating frequency of M_5 and M_6 can be increased by roughly three times as in (11) [25]. At the output, an integrated transformer with a turns ratio of 2:1 is implemented to convert the differential output into a single-ended signal.

Fig. 17 shows the simulated output power dynamic range of the PA according to the various gain setting. The dynamic range of the PA increased by 13 dB adopting the proposed adaptive LO buffer and thereby meets the required modulation index of 0.5–0.9.

V. Experimental Results

The transceiver in Fig. 5 is fabricated using a standard 130-nm CMOS process occupying 2.8 mm^2, as seen in a die photomicrograph of Fig. 18. Fig. 19 shows the measurement setups for the WuRx/Rx, Tx, and false wake-up. In Fig. 19(a), the ASK-modulating and RF-carrier signals are generated by the function and signal generators, respectively, to measure the sensitivity, which is measured by the duty ratio of the demodulated signal. As shown in Fig. 19(b), a function generator and spectrum analyzer are used for the Tx measurements. In Fig. 19(c), the false wake-up measurements are performed by adopting a smartphone as an interference signal generator, which receives real-time audio/video streams through WLAN, Bluetooth, or cellular networks. The smartphone and prototype WuRx are separated by approximately 10 cm as a possible worst case situation in an automotive environment. The number of false wake-ups are measured using the trigger function of the oscilloscope in a given time period of 3 min.

For the design parameters described in Sections IV-A and IV-B, the sensitivity of the WuRx and Rx can be estimated using (4), (5), and (8). Fig. 20 shows the estimated amplitude signal $A_{\rm in}$ at the input of the comparator for the WuRx [see Fig. 20(a)] and Rx [see Fig. 20(b)] paths as a function of the RF input power $P_{\rm IN}$ for various values of m. In Fig. 20, $A_{\rm min}$ is the minimum required input voltage at the input of the comparator for signal detection with the offset and noise voltages in (4), and $A_{\rm min\_noise}$ is $A_{\rm min}$ without the offset voltage. The intersection points of $A_{\rm in}$ with the $A_{\rm min}$ and $A_{\rm min\_noise}$ lines

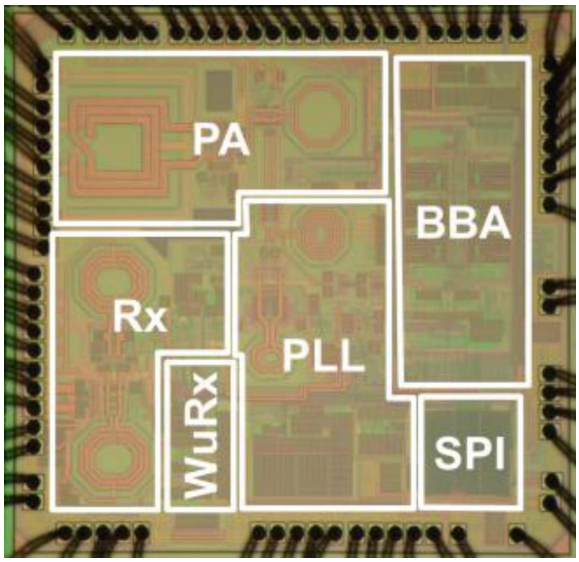

Fig. 18. Photomicrograph of the prototype transceiver chip.

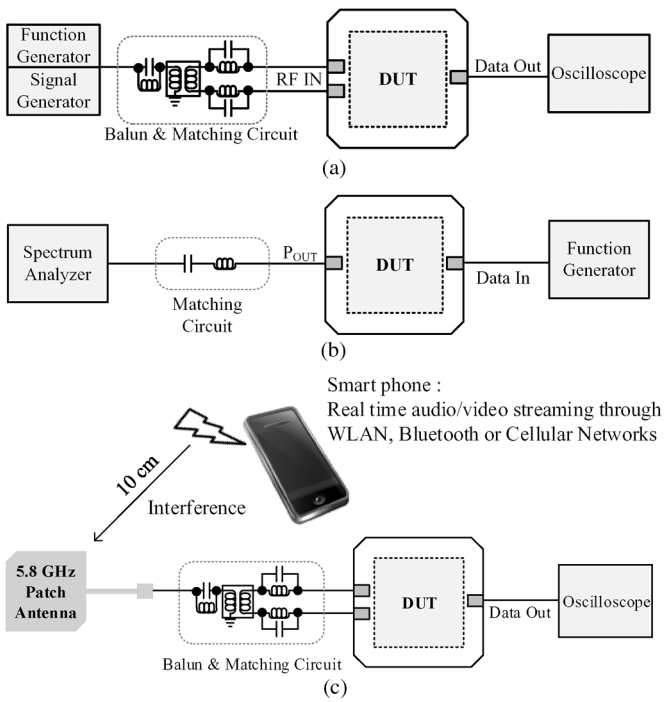

Fig. 19. Measurement setups for: (a) WuRx and Rx, (b) Tx, and (c) false wake-up.

represent the sensitivities $P_{\rm SNS}$ and $P_{\rm SNSnoise}$, respectively. In Fig. 20(a), when the WuRx has an offset voltage of 1.5 $\rm mV_{rms}$ and a noise voltage of 1.2 $\rm mV_{rms}$ at the input of the comparator, $A_{\rm min}$ satisfying the 40%–60% duty requirement is approximately 24 mV, which corresponds to $\rm SNR_{min} = 26$ dB from (5). Therefore, the estimated sensitivity is approximately -42 dBm. If there is no offset voltage, $A_{\rm min}$ and $\rm SNR_{min}$ become 5.4 mV and 13 dB, respectively, improving the sensitivity to -49 dBm. Fig. 20(b) shows that an LNA for the Rx improves the sensitivity to approximately -61 dBm when the noise and offset voltages at the input node of the comparator are 8 and 1.2 $\rm mV_{rms}$, respectively. In addition, $\rm SNR_{min}$ with and without the offset voltage are approximately 14.9 and 13 dB, respectively.

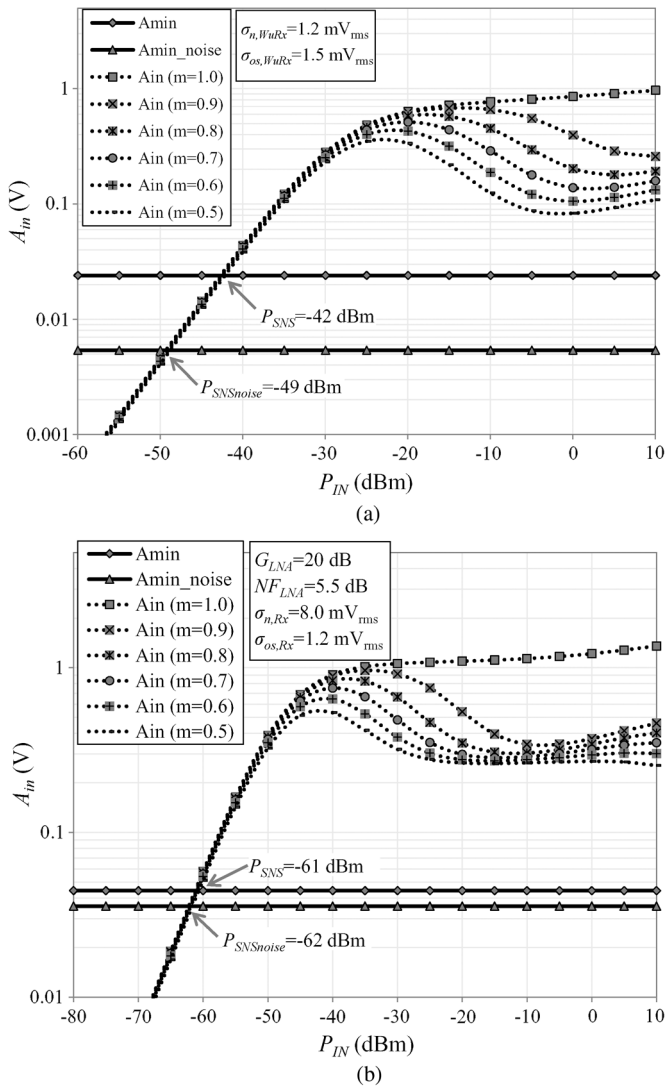

Fig. 20. Estimated amplitude of the signal at the input of the comparator for the: (a) WuRx and (b) Rx path.

Without the offset voltage, $\rm SNR_{min}$ appears to be the same for the WuRx and Rx.

Fig. 21(a) and (b) shows the measured duty ratio versus the input power of the WuRx and Rx, respectively, for $m = 0.5$ and 1.0. In Fig. 21(a), A and B represent the maximum and minimum duty ratios of the demodulated signal, respectively. From Fig. 21(a), the measured sensitivity of the WuRx is approximately -44 dBm, which is 4 dB lower than the requirement of the standard for 0-dBi antenna gain. There is a difference of approximately 1 dB in the sensitivity for $m = 0.5$ or 1.0. Fig. 20(a) shows that the maximum input level of the WuRx is not limited even if the output voltage is limited. However, Fig. 21(a) shows a maximum input level of approximately $+8$ dBm, which is induced by the collapse in the operating point of A in Fig. 7 by the excessively low dc voltage of the detector output node for a high input power. From Fig. 21(b), the Rx sensitivity is approximately -61 dBm, which is approximately 10 dB lower than the requirement. Unlike the WuRx, the maximum input level of the Rx is not limited because the input stage of the BPF is configured in a rail-to-rail topology. Fig. 21(c) shows the sample variations for the sensitivities of the WuRx and Rx. Note that the

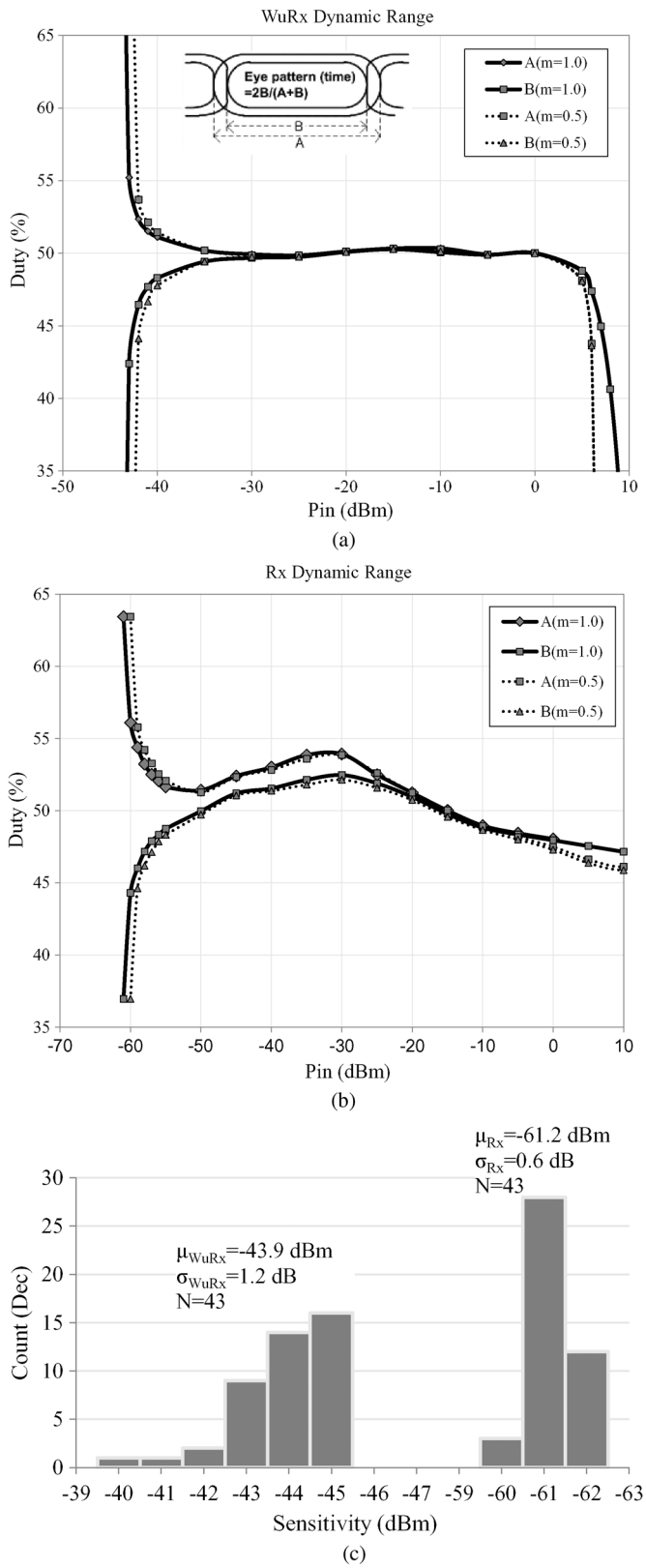

Fig. 21. Measured duty ratio versus input power of: (a) WuRx, (b) Rx, and (c) chip-to-chip sensitivity variations for WuRx and Rx.

WuRx exhibits larger variations than the Rx because the offset voltage of the comparator has a greater effect on the sensitivity, as analyzed in Fig. 20.

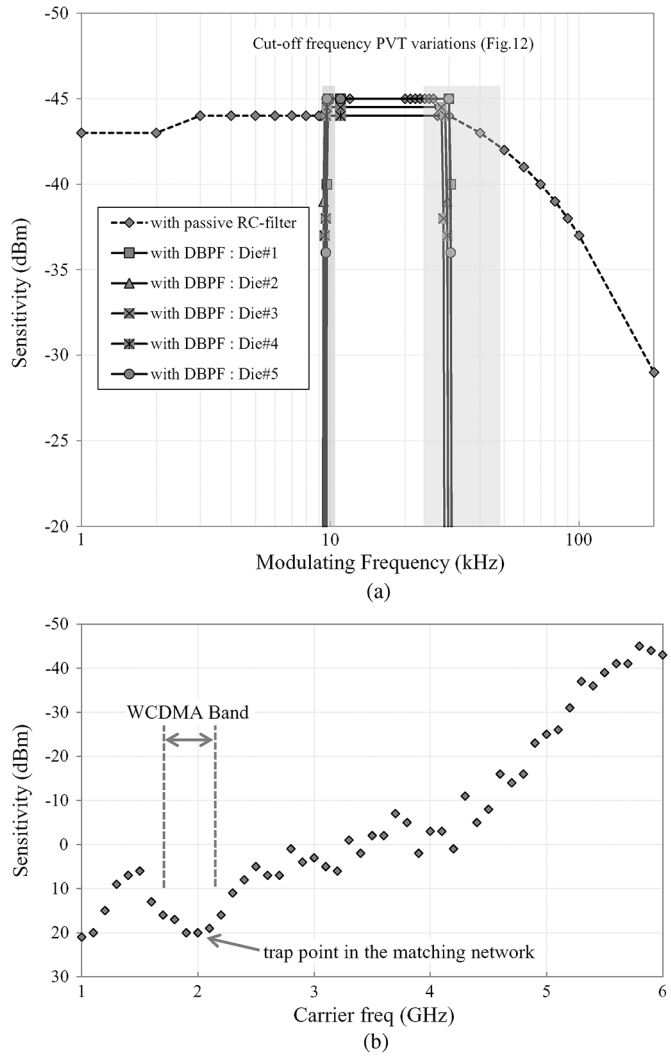

Fig. 22. Frequency response of the WuRx. (a) Modulating frequency response and (b) carrier frequency response with the effects of the antenna and WCDMA trap circuits.

Fig. 22 shows the measured sensitivity of the WuRx as a function of the modulation frequency. In Fig. 22(a), the WuRx with a passive RC filter exhibits a 3-dB bandwidth of approximately 50 kHz. It can be observed that the RC filter cannot sufficiently reject the interferers owing to its slow frequency slope. The measured frequency response of the DBPF exhibits a passband between 10–30 kHz, which is nearly matched to the cutoff characteristics of the simulation results, as shown in Fig. 12. From Fig. 22(b), the sensitivity of the carrier frequency band, where the 15-kHz pilot tones of the WCDMA system exist, is reduced by an additional 10 dB owing to the three parallel LC-resonant circuits in Fig. 7 in addition to the frequency characteristics of the patch antenna.

Fig. 23 shows the details of the current dissipation in the WuRx. Note that the RFED dissipates approximately 70% of the standby currents, whereas the DBPF consumes a very low sub-microampere current. The measured standby current of the WuRx is approximately 10 μA, which is lower than the example case of 22 μA described in Section II.

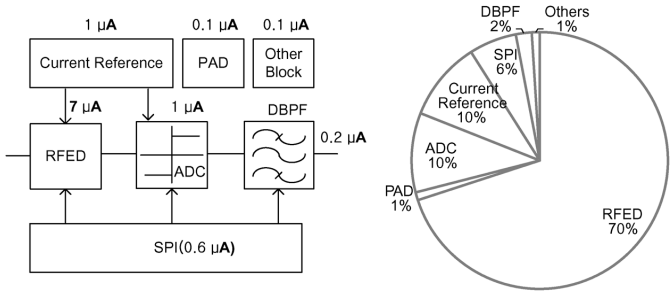

Fig. 23. Measured standby current of the WuRx.

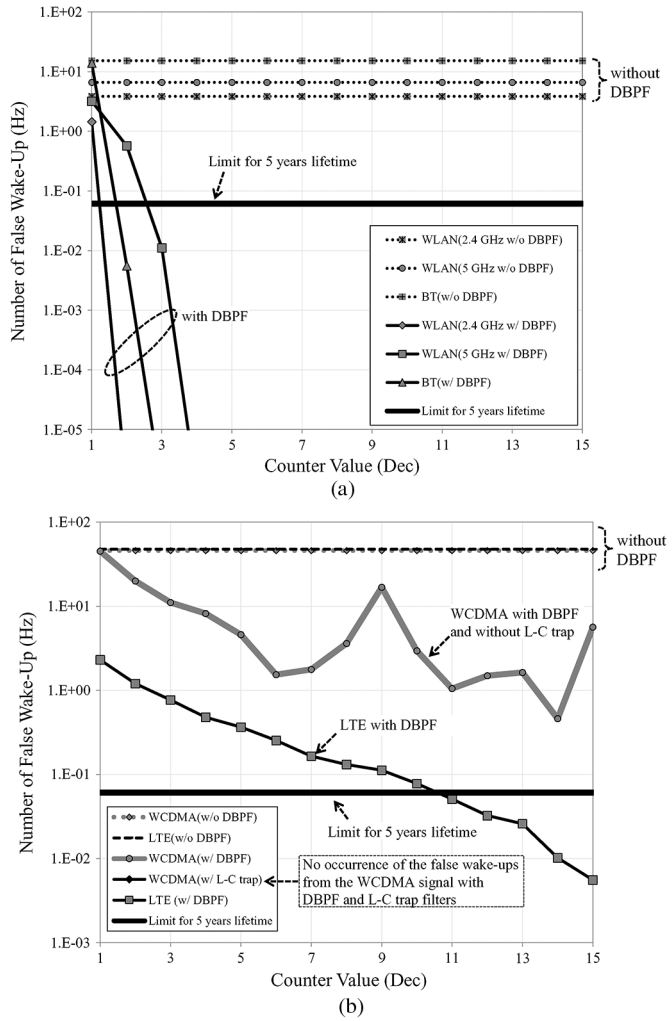

Fig. 24. Probability of the false wake-ups versus the counter value of the DBPF. Dotted lines represent the number of false wake-up per second without the DBPF. Solid lines are the number of false wake-up per second with the DBPF. (a) Response of the WuRx for WLAN and Bluetooth and (b) response of the WuRx for WCDMA and LTE.

Fig. 24 shows the false wake-up responses of the WuRx to various interferences with or without a DBPF and/or an LC-resonant trap. Fig. 24(a) shows that the false wake-up caused by the WLAN and Bluetooth is well rejected for a counter value of the DBPF greater than 3. However, Fig. 24(b) shows that the pilot tones of the WCDMA and LTE orthogonal frequency-division multiplexing (OFDM) signals are not completely removed by the DBPF alone. False wake-ups from the WCDMA signals occur regardless of the counter value of the DBPF, and the occurring frequency ranges between 0.5–46 Hz. As the occurring frequency of false wake-ups is limited to approximately 0.06 Hz with a 10-μA standby current, the lifetime of the OBU would become less than five years owing to interference from the WCDMA system. However, with the adoption of the LC trap filters (Fig. 7), the false wake-up from the WCDMA signals ceased. In contrast, Fig. 24(b) also shows that the number of false wake-ups from the LTE system depends on the counter value of the DBPF. Since the 15-kHz envelope signal of the LTE envelope signal has random probability [14], an increase in the counter value lowers the probability of false wake-ups further. If the counter value is greater than 11, the number of false wake-ups is below the limit of a five-year lifetime. Fig. 24 shows that the proposed DBPF with the LC trap filters reduces the false wake-ups much more efficiently compared to the conventional WuRx with only passive RC filters.

TABLE II
WuRx COMPARISON

	Standby Current	Operating Frequency	Data Rate	Sensitivity	Interference Filtering
This Work	10 μA (3.6 V)	5.8 GHz	14 kHz	-44 dBm	L-C filter + DBPF
[3]	104 μA (0.5 V)	2 GHz	100–200 kbps	-72 dBm	BAW resonator
[5]	0.18 μA (1.5 V)	434 MHz	2–80 kbps	-51 dBm	SAW + R-C filter
[6]	13.8 μA (1.45 V)	915 MHz	455 kbps	-69 dBm	SAW + IF BPF
[7]	2.4 μA (1.0 V)	868 MHz	100 kbps	-71 dBm	SAW + 64bit correlator

Table II summarizes the comparison of the proposed WuRx with other previously reported works [3], [5]–[7] considering interference-rejection issues. From Table II, the RF front-end typically adopts a SAW filter and some baseband analog- or digital-circuit techniques. In [5], a preamble detection circuit, similar to the HPF of the proposed DBPF, is implemented using an RC filter to remove the global system for mobile communications (GSM) OOK signal. In [6], a low-current narrowband IF filter technique is suggested, but the implementation details are not described. In [7], a correlation circuit having a 64-bit predetermined wake-up pattern is adopted to increase the sensitivity and to reduce the false wake-up probability, which has the drawback of a large wake-up latency caused by the correlation process. In [3], microelectromechancial systems (MEMS) technology is used to implement a high-Q front-end filter, but its performance may not be sufficient or suitable enough to reject the high-power interference. The data in Table II suggest that the proposed interference-rejection methods are simpler and more effective than previously reported approaches, while dissipating a reasonable amount of standby current at higher operating frequency of 5.8 GHz.

Fig. 25 shows the measured output power spectrum of the Tx for the highest data rate of 512 kb/s. The measured peak output power of the Tx is approximately $+5$ dBm, and the adjacent channel power ratio (ACPR) is approximately -59 dBc. The maximum and minimum output power ranges of the proposed

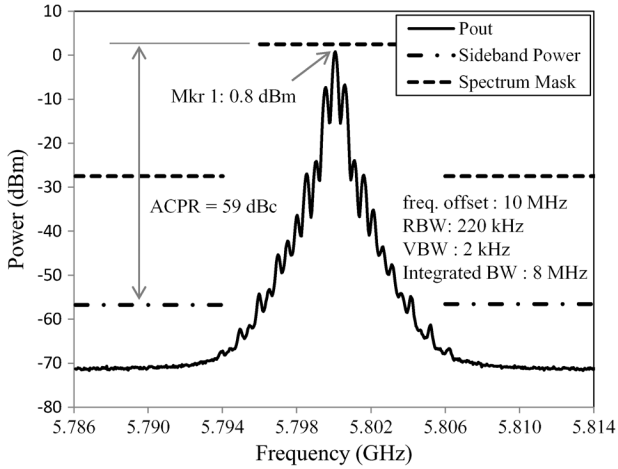

Fig. 25. Measurement results of the Tx output power and ACPR. The 0.8-dBm power level of marker 1 is equal to the peak power level of about +5 dBm. The ACPRs of upper and lower band are about −59 dBc.

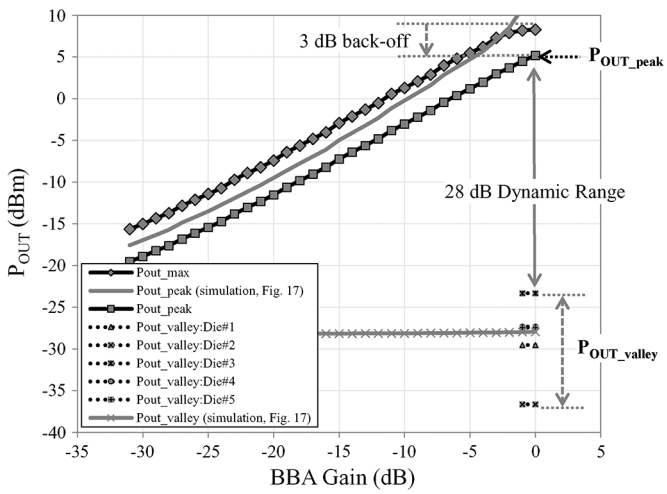

Fig. 26. Measurement results of the Tx output power dynamic range.

Tx are shown in Fig. 26. The output 1-dB compression point is approximately +8 dBm. Since the nominal output power is +5 dBm, there is a margin of approximately 3 dB for the back-off. As shown in Fig. 26, there are large variations in the output-valley power due to the dc offset and LO leakage, resulting in modulation-index errors. In Fig. 26, the usable modulation-index range increases to 92% because the linear output power range is approximately 28 dB. Fig. 27 shows that m ranges from 45% to 92%, which is sufficient to meet the standard requirements of 50%–90%. The measured modulation-index error is less than 10%.

The overall performance of the proposed 5.8-GHz DSRC transceiver is summarized in Table III in comparison with the requirement [1] and authors' prior works [2], [12]. Although several companies have been developing transceiver integrated circuits (ICs) for the Chinese ETCS [28], [29], to the best of the authors' knowledge, there is no previously published work on a fully integrated chip solution for the Chinese ETCS, except the authors' previous work [12]. In this work, compared to [12], the standby current of the WuRx is reduced to 10 μA by reducing

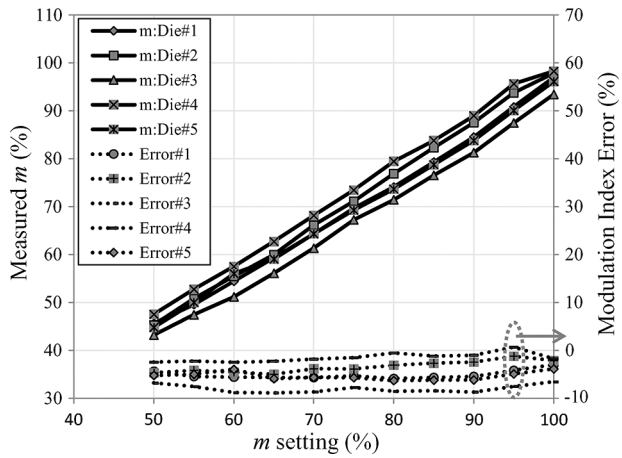

Fig. 27. Measurement results of the Tx modulation index.

TABLE III
PERFORMANCE SUMMARY OF THE PROTOTYPE

Parameter		[1]	[2]	[12]	This Work
Technology		-	0.13 μm CMOS		
Supply Voltage (V)		-	3.0–3.6	3.0–3.6	3.0–3.6
Operating Freq. (GHz)		5.8	5.8	5.8	5.8
WuRx	Wake-up freq. (kHz)	14	-	14	14
	Sensitivity (dBm)	≤ -40	-	-45	-44
	Current (uA)	22*	-	15	10
Rx	Data rate (kbps)	256	1,024	256	256
	Sensitivity (dBm)	≤ -50	-84	-61	-61
	Current (mA)	30*	52	19	19
Tx	Output power (dBm)	≤ +10	+ 10	+ 5	+ 5
	Modulation index (%)	50–90	55–95	45–95	45–95
	Data rate (kbps)	512	1,024	512	512
	Occupied BW (MHz)	≤ 5	4.5	3	3
	ACPR (dBc)	≤ -30	-43	-53	-59
	Spurious emission (dBm)	≤ -30	-	-51	-49
	Current (mA)	50*	150	40	46
Battery Lifetime (Years)		5*	-	7.2	10.8

* Example parameters in battery lifetime calculation (Table I)

the leakage current, and the Tx current is increased by approximately 6 mA owing to the additional frequency divider for the 11.6-GHz VCO in order to mitigate the LO-pulling problem [27]. On the basis of the standard requirements [1] and the example parameters in Table I, the battery lifetime of this work is estimated to be approximately 10.8 years, which corresponds to roughly twice the amount of the requirement. Considering the significantly reduced number of false wake-ups, by adopting the proposed DBPF in Fig. 24, the proposed transceiver is expected to fully operate for at least five years.

VI. Conclusion

This paper has presented a complete 5.8-GHz DSRC transceiver including the WuRx for Chinese ETCS terminals in a standard 130-nm CMOS process. In the WuRx, a high-gain RFED using a voltage-boosting technique and a low-current DBPF enable SNR improvement and a significant reduction in the standby current, leading to an increased battery lifetime of up to approximately ten years. At the same time, a low-current high-power adaptive-LO ASK modulator in the Tx allows lower operating current consumption after each wake-up. On the basis of the intensive investigation of automotive-application interference, it is found that the proposed DBPF may be able to guarantee a sufficient amount of interference rejection, thus potentially increasing the battery lifetime and reducing application costs.

Acknowledgment

The authors would like to thank Jinkyung Jung and Jinsung Yi of PHYCHIPS for the chip layout and interference analysis of the cellular networks, respectively. The authors would also like to thank Dr. Won Seok Lee and Professor Jong-Won Yu of the Radio Frequency System Solution Laboratory at KAIST for the 5.8-GHz patch-antenna design and evaluation.

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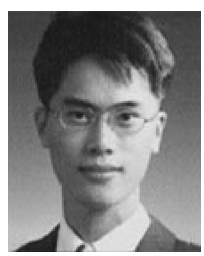

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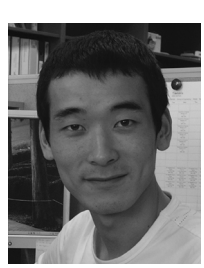

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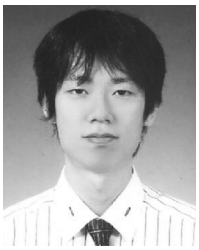

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