A 2.2 mW, 40 dB Automatic Gain Controllable Low Noise Amplifier for FM Receiver

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***Abstract*—This paper presents an automatic gain controllable low noise amplifier (AGC-LNA) for FM receiver (FMRx). The proposed LNA adopts current reused dual g_m-boosting technique for the power saving. And, a simple analog type automatic gain control (AGC) loop is proposed that provides high resolution gain control. Implemented in a 65 nm CMOS technology, measurements show power regulation range of 40 dB with ±1 dB error, less than −11 dB of S11, variable voltage gain range of −12 to 30 dB over the frequency range of 88∼108 MHz, noise figure (NF) of less than 2.9 dB, P1dB of higher than −24.2 dBm, and IIP3 of higher than −12.7 dBm in the high gain (HG) mode, while dissipating only 1.8 mA from a 1.2 V supply, respectively.**

***Index Terms*—AGC, automatic gain control, FM, FM radio, FM receiver, frequency modulation, LNA, low noise amplifier, received signal strength indicator, RSSI, variable gain low noise amplifier, VGLNA.**

I. Introduction

RECENTLY, with the extensive use of smart phones and mobile devices, various add-on functions are implemented. FM radio is one of the essential add-on functions, such that small size, low power, and high performance CMOS solution for the FM receiver (FMRx) is in need [1]. As a key block of the Rx, the LNA design involves demanding challenges to satisfy the performance requirements; low noise figure (NF), reasonable gain, and high linearity while dissipating as little power as possible. Furthermore, in order to increase the dynamic range of Rx input and tolerance to the interferers, high resolution gain control is essential.

The previously reported FMRx LNAs are focused on lower power [2], [3] and smaller size [4]; but relatively little work has been done on improving performance while maintaining low power consumption. The LNAs reported in [2]–[4] adopt programmable gain (PG) control technique with little details for the automatic gain control (AGC) loop. Their digital AGCs have much less issue with stability and all the digital parts can be generated automatically with technology scaling. However, digital AGCs not only need analog-to-digital converter (ADC) to control the gain, but also require DSP work most of the time, moreover, the switching noise from the digital control circuit can be an issue. Furthermore, the PGLNAs require many control bits and switches which complicate the design, especially, when the LNA is utilized as a single IP, extra pads are needed. There are two trade-offs in previously reported FMRx LNAs [2]–[4]. One is performance versus power consumption and the other the gain control resolution versus complexity. This paper reports a low power, high performance, and automatically gain controllable LNA (AGC-LNA) that overcomes above trade-offs. The rest of the paper is organized as follows. Section II describes the design details of the proposed AGC-LNA, Section III the measurement results, and Section IV the conclusion.

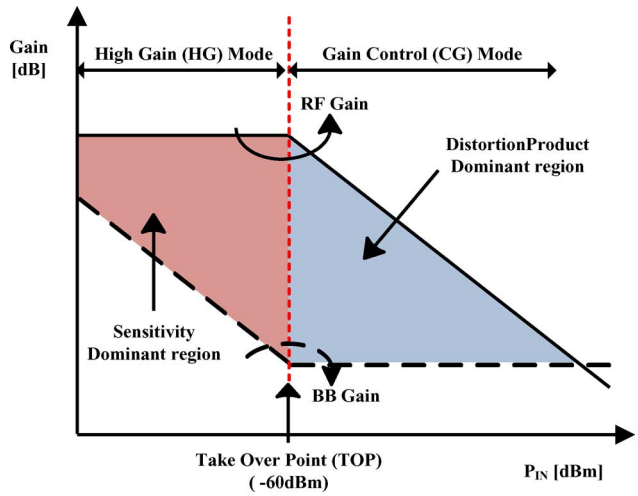

Fig. 1. Gain control scheme reported in [5].

II. AGC-LNA Design

A. Gain Control Scheme

Fig. 1 shows the gain control scheme reported in [5] that has been adopted in the proposed LNA. In Fig. 1, the LNA operates in two modes: high gain (HG) and gain control (GC) modes. In the HG mode, small input signals are injected into Rx, where the Rx performance is dominated by the sensitivity, described as sensitivity dominant region [5]. Thus, the Rx front-end is configured to provide maximum gain to minimize NF and the gain control is done in the base-band (BB) stages. In the GC mode, the higher level input signals are injected into Rx, where the Rx performance is limited by the intermodulation distortion products, described as distortion product dominant region [5]. In this region, the Rx front-end gain is adjusted according to the power level of input signal to avoid Rx system saturation. In the proposed AGC-LNA, the boundary input power level (take-over point; TOP) between HG and GC mode is set at −60 dBm which is determined by the Rx budget analysis to optimize Rx signal to noise ratio (SNR).

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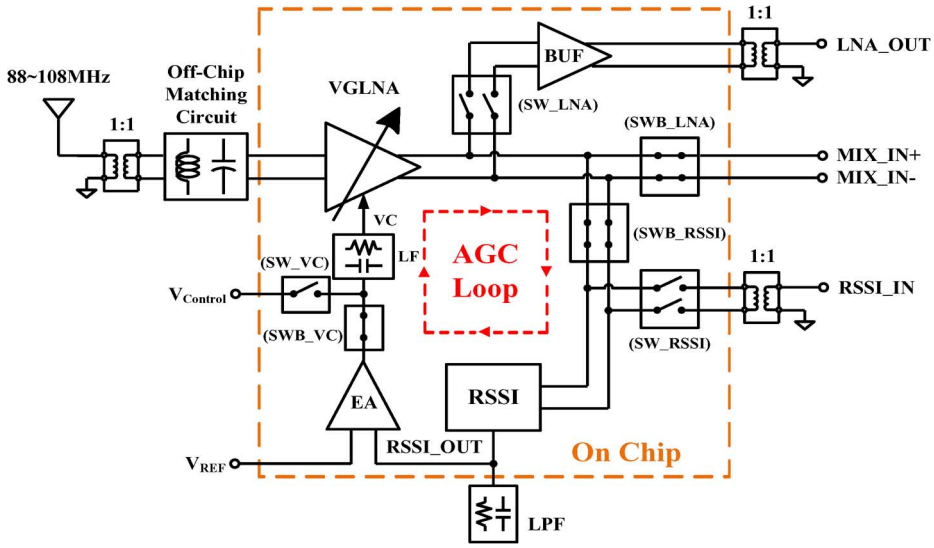

Fig. 2. Block diagram of the proposed AGC-LNA.

TABLE I
MEASUREMENT MODE VERSUS THE SWITCH CONDITIONS

SW_LNA	SW_RSSI	SW_VC	Measuring Block
ON	ON	ON	VGLNA
X	ON	X	RSSI
ON	OFF	OFF	AGC-LNA Loop
OFF	OFF	OFF	Receiver

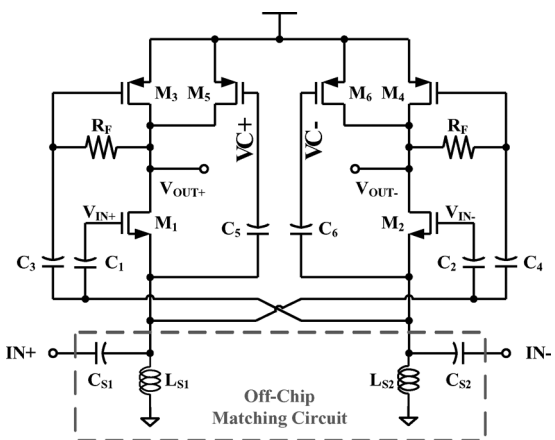

Fig. 3. Schematic of the proposed VGLNA.

B. Architecture

Fig. 2 shows the block diagram of the proposed AGC-LNA. It consists of a variable gain LNA (VGLNA), received signal strength indicator (RSSI), error amplifier (EA), and loop filter (LF). The on-chip buffer (BUF) and off-chip control voltage ($V_{Control}$) pin are added for the measurement purpose. And, three switch pairs (SW_LNA, SW_RSSI, and SW_VC) are added to measure functional operation of individual blocks. The RSSI senses the output power of the VGLNA and generates the corresponding dc output voltage (RSSI_OUT). The EA compares the RSSI_OUT with the reference voltage (V_{REF}) and generates feedback control signal (VC) to control the gain of the VGLNA. The LF is added to stabilize the AGC loop. Table I shows the measurement mode for different combination of switches operations. In Table I, the don't-care operation is expressed as X.

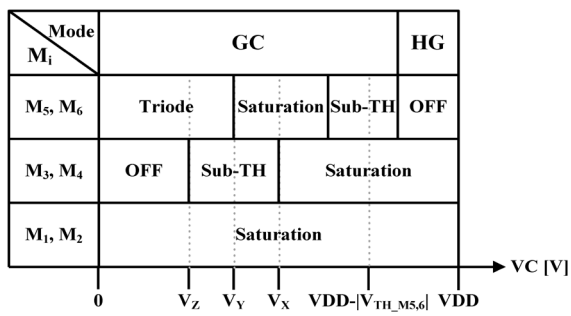

Fig. 4. Operational regions of the transistors versus VC.

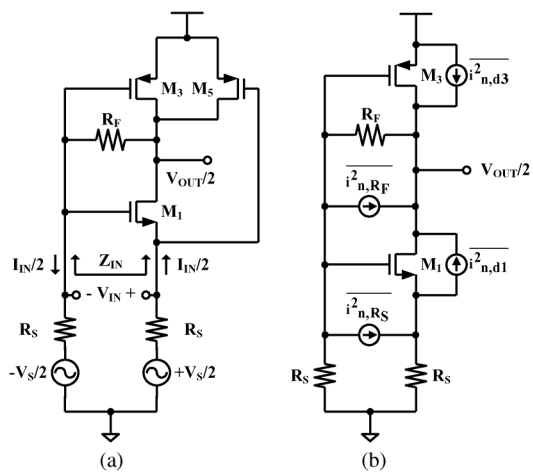

Fig. 5. Simplified half circuit of the proposed VGLNA for the analysis of (a) Z_{IN}, A_V, and (b) NF.

C. VGLNA Design

Fig. 3 shows the schematic of the proposed VGLNA which consists of off-chip matching components $(L_{S1,S2}, C_{S1,S2})$, ac-coupling capacitors (C_{1-6}), transconductance stage $(M_1 - M_4)$, gain control stage (M_5, M_6), and self-biasing resistor (R_F). The proposed LNA adopts current-reused dual g_m-boosting technique which is realized by the cross-coupled common-gate (CG) pairs (M_1, M_2) in combination with PMOS pairs (M_3, M_4), leading to high gain with lower power consumption.

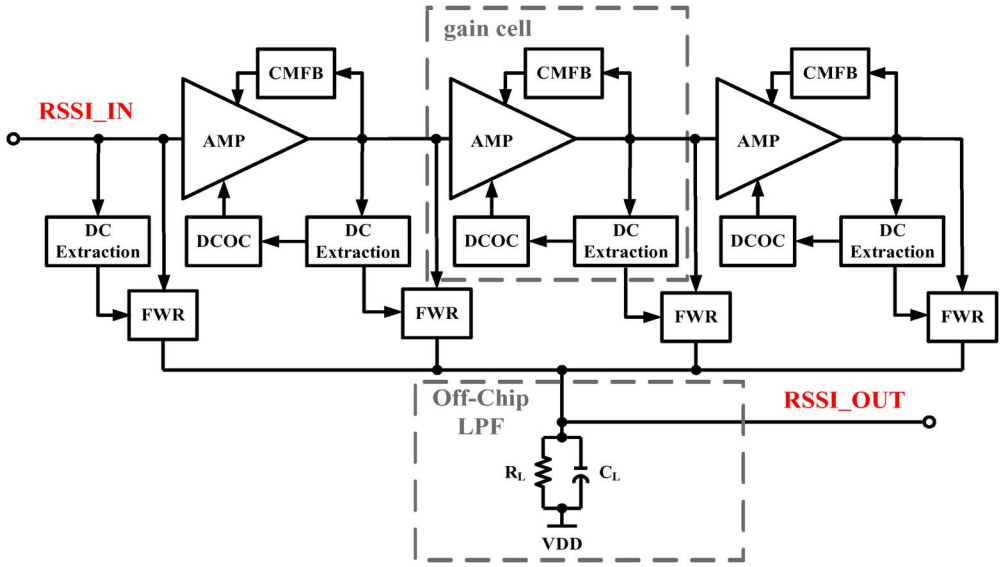

Fig. 6. Block diagram of the proposed received signal strength indicator.

In Fig. 3, the operational regions of the transistors are varied as a function of the gain control signal VC, which is shown in Fig. 4. As can be seen from Fig. 4, in HG mode, M_{1-4} and $M_{5,6}$ operate in saturation and cut-off region, respectively. However, in GC mode, with decease in VC, M_{3-6} change their operational regions. $M_{3,4}$ move from saturation to sub-threshold (Sub-TH) and then to cut-off regions. $M_{5,6}$ move from Sub-TH to saturation and then to triode regions. In Fig. 4, $V_{TH\_M5,6}$ represents the threshold voltage of $M_{5,6}$, V_X the value of VC when $M_{3,4}$ enter Sub-TH region, V_Y the value of VC when $M_{5,6}$ enter triode region, V_Z the value of VC when $M_{3,4}$ enter cut-off region, respectively.

Fig. 5 shows the simplified half circuit of the proposed VGLNA for the analysis of input impedance (Z_{IN}), voltage gain (A_V), and NF. In Fig. 5(a), V_S represents the input-source signal, R_S the source resistance, V_{IN} the equivalent input voltage, I_{IN} the equivalent input current, and V_{OUT} the output voltage, respectively. In Fig. 5(a), off-chip matching components are neglected to simplify the equivalent half circuit. From Fig. 5(a), the Z_{IN} of the proposed VGLNA is given by

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{[(r_{o3}\|r_{o5})+R_F]r_{o1}+(r_{o3}\|r_{o5})R_F}{[(r_{o3}\|r_{o5})+R_F](2g_{m1}r_{o1}+1)+[(g_{m5}-g_{m3})R_F+1](r_{o3}\|r_{o5})} \quad (1)$$

where r_{oi} is the output impedance of transistor M_i and g_{mi} the transcoductance of M_i, respectively. In (1), $r_{o3,5}$ and $g_{m3,5}$ are varied as a function of the gain control signal VC, however, as can be seen from Fig. 4, M_1 stays in saturation region. Therefore, assuming $2_{gm1} \cdot r_{O1} \gg 1$ and $r_{O1} \gg R_F$, Z_{IN} is approximately $1/(2 \cdot g_{m1})$, regardless of the region of operation for $M_{3,5}$. The A_V of the proposed VGLNA is given by

$$A_V = \frac{V_{IN}}{V_S} \cdot \frac{V_O}{V_{IN}} \approx \frac{Z_{IN}}{R_S + Z_{IN}} \cdot \left(2g_{m1} + g_{m3} - g_{m5} + \frac{1}{r_{o1}} - \frac{1}{R_F}\right) \times (r_{o1} \parallel r_{o3} \parallel r_{o5} \parallel R_F) \quad (2)$$

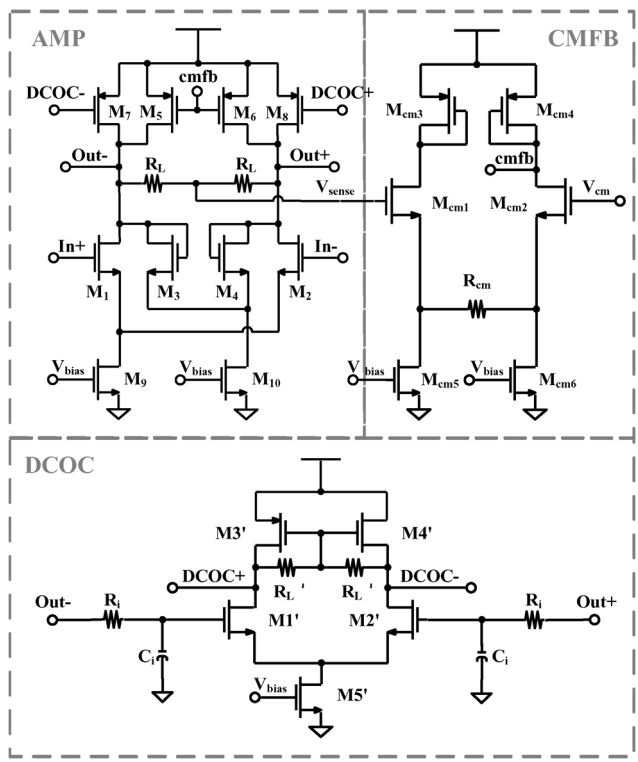

Fig. 7. Schematic of the proposed gain cell.

from (2), the proposed VGLNA achieves HG when g_{m5} is zero. However, with increase in g_{m5}, A_V decreases by the decrease in overall transconductance and the output resistance. The A_V can be controlled by the transconductance of $M_{1,3}$ and M_5 with opposite polarities. Furthermore, the proposed VGLNA adopts dual g_m-boosting by the cross-coupled CG transistor (M_1) and the current-reused common-source transistor (M_3) in one current branch. Therefore, the proposed VGLNA can achieve high gain and gain control capability with low power consumption.

In Fig. 5(b), noise current from M_5 is neglected, while $\overline{i^2_{n\_R_s}}$, $\overline{i^2_{n\_R_F}}$, and $\overline{i^2_{n\_di}}$ represent the mean-squared thermal noise cur-

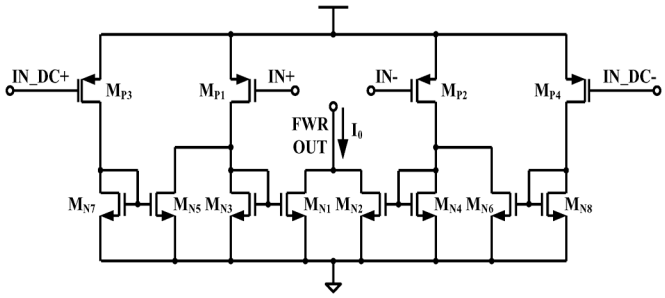

Fig. 8. Schematic of the full wave rectifier reported in [7].

rent generated by R_S, R_F, and transistor channel, respectively, given by

$$\overline{i_{n,RS}^2}=\frac{4KT}{R_s}\cdot\Delta f, \overline{i_{n,RF}^2}=\frac{4KT}{R_F}\cdot\Delta f, \overline{i_{n,di}^2}=4KT\gamma g_{doi}\cdot\Delta f \tag{3}$$

where Δf is the bandwidth, γ the coefficient of channel thermal noise of MOSFET, g_{doi} the zero-bias drain conductance of transistor M_i, respectively. Assuming $g_{m1,3}\cdot r_{o1,3}\gg 1$, the noise transfer function (H_i) of each noise source in Fig. 5(b) can be expressed as

$$H_{R_S}=\frac{V_o}{\overline{i_{n,R_S}}}\approx 2R_F \cdot\frac{(g_{m1}+g_{m3})R_S+g_{m1}\left(\frac{1}{g_{m1}}\|R_S\right)(1-g_{m1}R_S)}{(g_{m1}+g_{m3})R_S-\left(\frac{1}{g_{m1}}\|R_S\right)g_{m1}{}^2R_S+1} \tag{4}$$

$$H_{d1}=\frac{V_o}{\overline{i_{n,d1}}}\approx 2R_F \cdot\frac{1-\left[g_{m1}\left(\frac{1}{g_{m1}}\|R_S\right)\right]}{(g_{m1}+g_{m3})R_S-\left(\frac{1}{g_{m1}}\|R_S\right)g_{m1}{}^2R_S+1} \tag{5}$$

$$H_{d3}=\frac{V_o}{\overline{i_{n,d3}}}\approx\frac{2R_F}{(g_{m1}+g_{m3})R_S-\left(\frac{1}{g_{m1}}\|R_S\right)g_{m1}{}^2R_S+1} \tag{6}$$

$$H_{RF}=\frac{V_o}{\overline{i_{n,R_F}}}\approx 2R_F. \tag{7}$$

In Fig. 5(b), with transistors, only the channel thermal noise is considered. From (4)–(7), assuming input is matched ($\mathrm{R_S}\approx 1/(2\cdot g_{m1})$) and $g_{m1}=g_{m3}=g_m$, the noise factor (F) of the proposed VGLNA can be given by

$$\begin{aligned}F&=\frac{\overline{V_{n\_OUT,total}^2}}{\overline{V_{n\_OUT,R_S}^2}}\\&\approx 1+\frac{|H_{d1}|^2\cdot\overline{i_{n,d1}^2}+|H_{d3}|^2\cdot\overline{i_{n,d3}^2}+|H_{R_F}|^2\cdot\overline{i_{n,R_F}^2}}{|H_{R_S}|^2\cdot\overline{i_{n,R_S}^2}}\\&\approx +1\frac{(4^2+6^2)}{7^2}\cdot g_mR_S\cdot\frac{\gamma}{\alpha}+\frac{11^2}{7^2}\cdot\frac{R_S}{R_F}\\&\approx 1+\frac{1}{1.88}\cdot\frac{\gamma}{\alpha}+\frac{1.23}{g_mR_F}\end{aligned} \tag{8}$$

where $V_{n\_OUT,total}$ is the total output noise voltage, $V_{nOUT,RS}$ the noise voltage at the output caused by $\overline{i_{n\_rs}^2}$, and $\alpha_i=g_{mi}/g_{d0i}$, respectively. As can be seen from (8), the NF

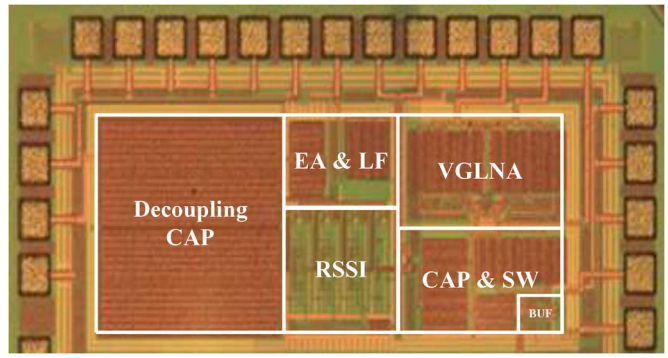

Fig. 9. Chip photograph.

of the proposed VGLNA is similar to the cross-coupled CG LNA $(1+\gamma/2\alpha)$ [6] while consumes smaller power.

D. RSSI Design

Fig. 6 shows the block diagram of the proposed RSSI which consists of three gain cells, four full wave rectifiers (FWRs), and an off-chip low-pass filter (LPF). The input to the RSSI is amplified and rectified by each gain cell and FWRs. Then the outputs of FWRs are added up and filtered into a dc voltage output (RSSI_OUT). In each gain stage, the feedback-type dc offset cancellation (DCOC) circuit is added since the dc offset from the output of each amplifier can severely degrade the performance of rectifiers.

Fig. 7 shows the schematic of the gain cell shown in Fig. 6. As can be seen in Fig. 7, AMP adopts the diode-connected load $(\mathrm{M_{3,4}})$ for the process independent voltage gain. In Fig. 7, the CMFB stabilizes the output common-mode level, while the DCOC prevents the dc-offset amplification. The DCOC performs negative feedback operation by detecting the output dc level of the AMP through the LPF (R_i and C_i) and adjusting bias current of $\mathrm{M_{7,8}}$. By the CMFB and DCOC, the output common-mode level variation and dc offset of the gain cell are reduced by a factor of each loop gain, respectively.

Fig. 8 shows the schematic of the FWR [7] which converts the ac input voltage into a rectified output current (I_0). The sum of the output current from all four FWRs in Fig. 6 is injected into the off-chip LPF $(R_L\|C_L)$ and the amount of dc voltage at the output of LPF represents the received signal strength.

E. AGC-LNA Stability Analysis

In the proposed AGC-LNA, there is a feedback (FB) path from the output to the gain control stage $(\mathrm{M_{5,6}})$ of the VGLNA shown in Fig. 2. The transfer functions of each block (T_i) in the FB path can be expressed as

$$\mathrm{T_{RSSI}(s)}=\frac{\Delta\mathrm{RSSI\_OUT(s)}}{\Delta\mathrm{P_{IN}(s)}}\approx\frac{S_{RSSI}}{1+\mathrm{s}/\omega_{RSSI}} \tag{9}$$

$$\mathrm{T_{EA}}=(\mathrm{s})=\frac{\Delta\mathrm{VC(s)}}{\Delta\mathrm{RSSI\_OUT(s)}}\approx\frac{A_{EA}}{1+\mathrm{s}/\omega_{EA}} \tag{10}$$

$$\mathrm{T_{VGLNA}(s)}=\frac{\Delta\mathrm{V_o(s)}}{\Delta\mathrm{VC(s)}}\approx-\frac{g_{m5,6\_VC}\cdot\mathrm{Z}_{OUT}}{1+\mathrm{s}/\omega_{VGLNA}} \tag{11}$$

where $\Delta\mathrm{P_{IN}(s)}$ is the RSSI input power deviation from wanted power level, $\Delta\mathrm{RSSI\_OUT(s)}$, $\Delta\mathrm{VC(s)}$, and $\Delta\mathrm{V_O(s)}$ the small signal variation of each node in the FB path, respectively. S_{RSSI} is the ratio between the low frequency input power and the dc output voltage (RSSI_OUT) in V/dB [8], A_{EA}

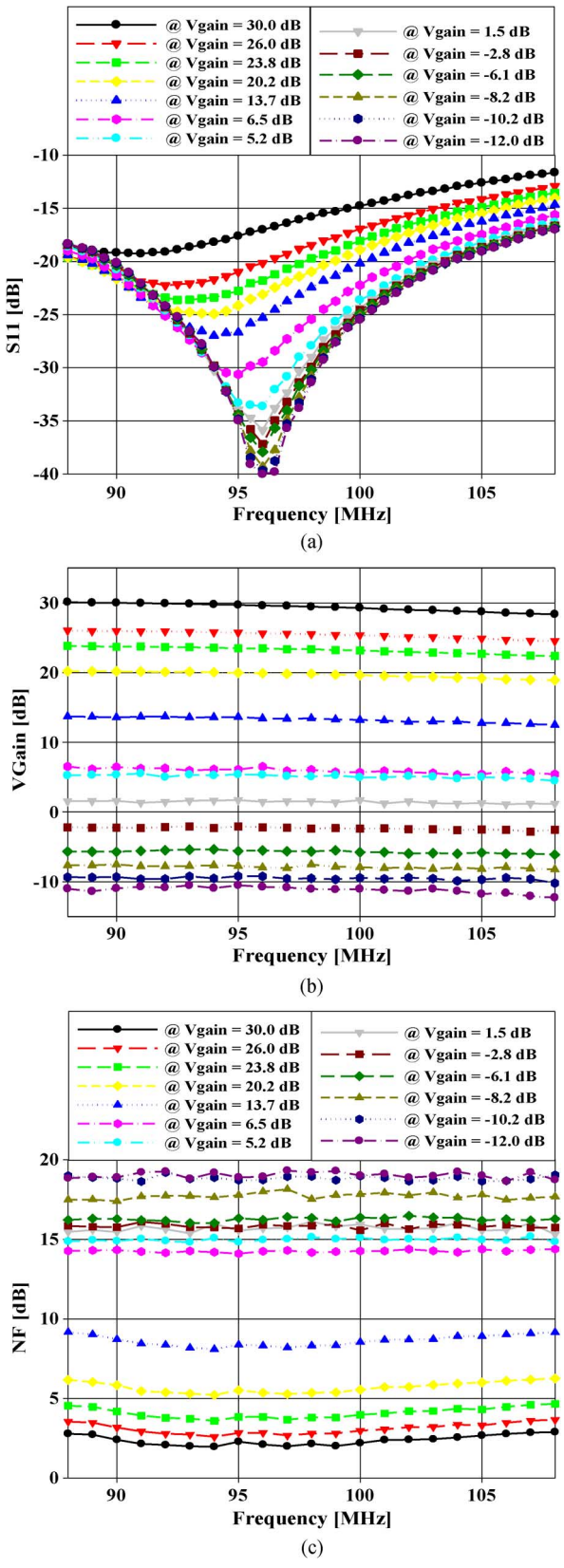

Fig. 10. Measurement results; (a) S11, (b) voltage gain, (c) NF, (d) P1dB, and (e) IIP3 versus frequency for various gain settings.

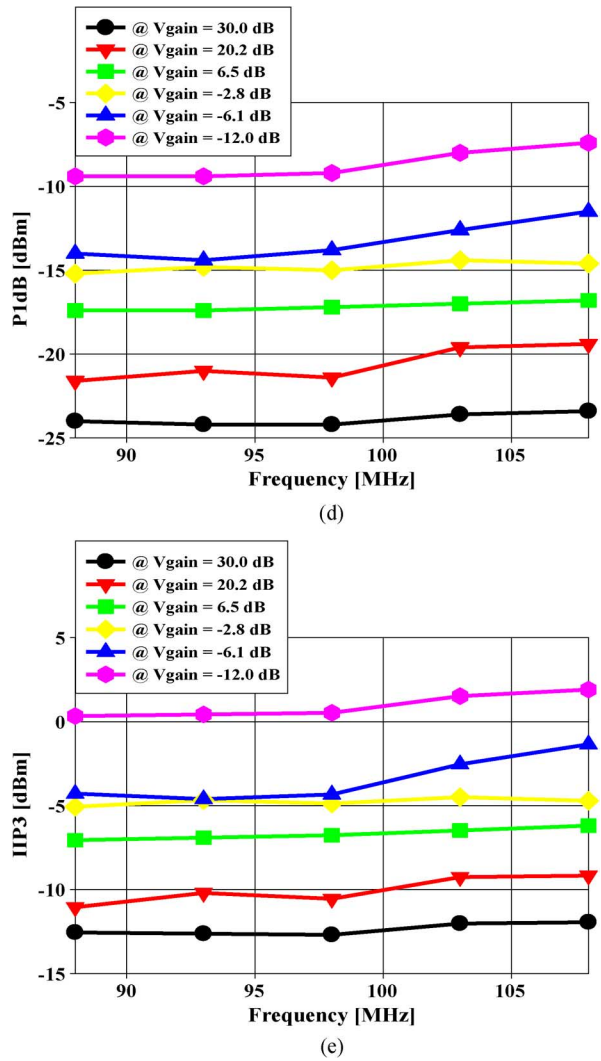

Fig. 10. *(Continued.)* Measurement results; (a) S11, (b) voltage gain, (c) NF, (d) P1dB, and (e) IIP3 versus frequency for various gain settings.

the dc gain of the EA, $g_{m5,6\_VC}$ the transconductance of the gain control transistor $(\mathrm{M}_{5,6})$ that varies as a function of VC, Z_{OUT} the output impedance of the VGLNA, ω_{RSSI}, ω_{LF}, and ω_{VGLNA} the angular frequency of each block in the FB path, respectively.

In Fig. 2, by breaking the loop at the junction between the output of VGLNA and the input of RSSI and assuming $\mathrm{R_S} = 50$, the loop gain transfer function T(s) and phase margin (PM) can be given by

$$\begin{aligned}\mathrm{T(s)} &= -\frac{\Delta \mathrm{V_o(s)}}{\Delta \mathrm{V_{IN}(s)}} = -\frac{\Delta \mathrm{V_o(s)}}{\Delta \mathrm{P_{IN}(s)}} \cdot \frac{\Delta \mathrm{P_{IN}(s)}}{\Delta \mathrm{V_{IN}(s)}} = \mathrm{T(0)} \cdot \mathrm{H(s)} \\ &\approx \frac{S_{RSSI} \cdot A_{EA} \cdot g_{m5,6\_VC} \cdot Z_{OUT}}{\left(1+\frac{s}{\omega_{RSSI}}\right)\left(1+\frac{s}{\omega_{LF}}\right)\left(1+\frac{s}{\omega_{VGLNA}}\right)} \\ &\quad \cdot \frac{\Delta \mathrm{P_{IN}(s)}}{10^{(\Delta \mathrm{P_{IN}(s)}+20)/20}} \end{aligned} \tag{12}$$

$$\begin{aligned}\mathrm{PM} \cong 180^\circ &- tan^{-1}\left(\frac{\omega_{UGF}}{\omega_{LF}}\right) \\ &- tan^{-1}\left(\frac{\omega_{UGF}}{\omega_{RSSI}}\right) - tan^{-1}\left(\frac{\omega_{UGF}}{\omega_{VGLNA}}\right)\end{aligned} \tag{13}$$

where $\Delta \mathrm{V_{IN}(s)}$ is $\Delta \mathrm{P_{IN}(s)}$ in the voltage domain, T(0) the dc value of T(s), H(s) the frequency response, ω_{UGF} the unity gain frequency of the AGC loop in rad/sec, respectively.

TABLE II
PERFORMANCE SUMMARY IN COMPARISON WITH PREVIOUSLY REPORTED FM VGLNAS

Performance	This Work	JSSC 2004 [2]	TCASI 2008 [4]	NXP 2011 [10][a]	Infineon 2012 [11][a]
Frequency [MHz]	88~108	88~108	76~108	10~200	10~1000
Supply [V]	1.2	0.9	1.35	2.85	3
Current[b] [mA]	1	0.25	4.5	3.2	2.8
S11 [dB]	< -11.6	< -6	-	-0.5	-0.5
Vgain Range [dB]	-12 ~ 30 (Continuous steps)	14 / 34 (Two steps)	0.5 ~ 32.5 (1dB steps)	19 (Fixed gain)	19.5 (Fixed gain)
NF [dB]	2.0 ~ 2.9[c] (@HG) 18.6 ~ 19.2[c] (@LG)	5~8[d] (@HG)	< 7.5[e] (@HG) (< 1.5 nV / $\sqrt{\text{Hz}}$)	1.2	1.2
P1dB [dBm]	-24.2 ~ -23.4 (@HG) -9.4 ~ -7.4 (@LG)	-	-	-23	-
IIP3 [dBm]	-12.7 ~ -11.9 (@HG) 0.3 ~ 1.9 (@LG)	-	-16.5 (@HG) -5.2 (@LG)	-15	-14
AGC Type	Voltage Controlled	Switch Controlled	Switch Controlled	-	
Technology [nm]	65	180	180	-	-
FOM[f] (@ HG)	1.49	-	0.03	0.097	0.14

[a] Measured at 100 MHz of input frequency.
[b] The current consumption for LNA only.
[c] LNA only,
[d] Rx NF with maximum LNA gain. Rx NF is dominated by LNA NF.
[e] NF of LNA with tunable antenna interface.
[f] $FOM = Gain\,[abs] \cdot IIP3\,[\text{mW}]/\{(NF-1)\,[abs] \cdot PD\,[\text{mW}]\}$ [12].

In (12), $g_{m5,6\_VC} \cdot \text{Z}_{\text{OUT}}$ varies as a function of VC. And, the steady-state error between the VGLNA output power and the wanted output power is inversely proportional to T(0) [9]. Therefore, to decrease the steady-state error, minimum value of T(0) should be larger than 1 which can be ensured by a large value of $S_{RSSI} \cdot A_{EA}$·.

From (13), there are three poles (ω_{RSSI}, ω_{VGLNA}, and ω_{LF}) in the AGC loop. To stabilize the AGC loop, the non-dominant poles (ω_{RSSI}, ω_{VGLNA}) in the AGC loop should be located far away from the dominant pole (ω_{LF}), ω_{RSSI}, $\omega_{VGLNA} \gg \omega_{LF}$, hence, ω_{UGF} is equal to T(0)·ω_{LF}.. Assuming $\omega_{RSSI} \approx \omega_{VGLNA} = \omega_{RSSI,VGLNA}$, PM can be simplified as

$$\text{PM} = 90^\circ - 2tan^{-1}\left(\frac{\text{T}(0)\cdot\omega_{LF}}{\omega_{RSSI,VGLNA}}\right). \qquad (14)$$

From (14), in order to achieve PM higher than 60° to stabilize the AGC loop, ω_{LF} should satisfy the condition of

$$\omega_{LF} \le \frac{\omega_{RSSI,VGLNA}\cdot tan15^\circ}{\text{T}(0)}. \qquad (15)$$

Therefore stability is ensured by proper location of ω_{LF} in the LF.

III. MEASUREMENT RESULTS

The proposed AGC-LNA shown in Fig. 2 is implemented in a 65 nm CMOS technology. Fig. 9 shows the chip photograph, which is 2.3×0.9 mm^2 in size including bond pads and the core size is 1.5×0.5 mm^2. Fig. 10 shows the measured S11, voltage gain (A_V), NF, P1dB, and IIP3 for the gain range of -12 to 30 dB over the frequency range of 88 to 108 MHz. As shown in Fig. 10 , over the gain variation range, S11 stays below -11.6 dB, and NF, P1dB, and IIP3 vary 2.0~19.2 dB, $-24.2 \sim -7.4$ dBm, and $-12.7 \sim 1.9$ dBm, respectively. It can be seen that, in the HG mode, the proposed VGLNA show less than -11.6 dB for S11, AV of 28~30 dB, NF of 2.0~2.9 dB, P1dB of $-24.2 \sim -23.4$ dBm, and IIP3 of $-12.7 \sim -11.9$ dBm, respectively. The proposed VGLNA dissipates 1 mA from a 1.2 V supply over the whole gain range.

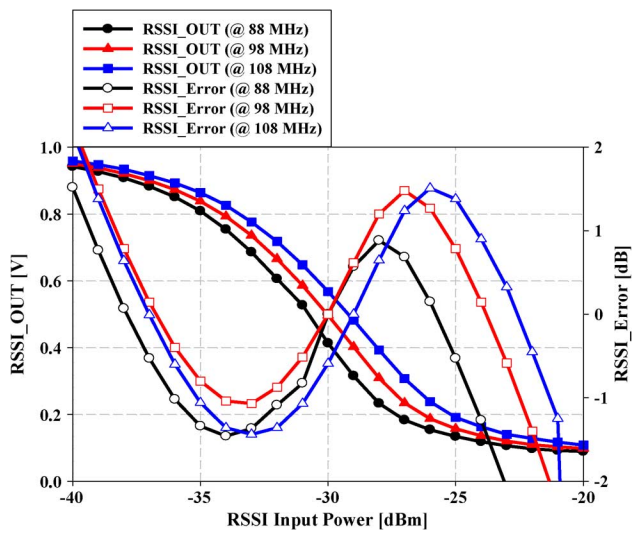

Fig. 11. Measured RSSI_OUT and dB-linear error versus the RSSI input power.

In Table II, the performance of the proposed VGLNA is summarized and compared with the previously reported FM VGLNAs. From Table II, the proposed VGLNA shows good overall performance and best figure of merit (FOM) while dissipating small amount of power.

Fig. 11 shows the measured dc voltage of the RSSI_OUT and dB-linear error versus the RSSI input power at three different operating frequencies, 88, 98, and 108 MHz. The measurement results show dB-linear range of 15 dB with ± 1.5 dB error in the RSSI_OUT while consuming less than 0.8 mA from a 1.2 V supply.

Fig. 12 shows the measured output versus input power level of the proposed AGC-LNA. In Fig. 12, with AGC loop, the

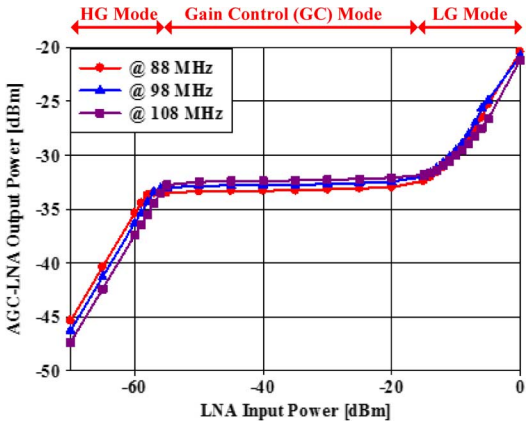

Fig. 12. Measured AGC-LNA output power versus the input power.

output power of VGLNA is regulated to a wanted power level of −33 dBm over 40 dB of input range with less than ±1 dB error. The proposed AGC-LNA dissipates 1.8 mA in total, 1.0 and 0.8 mA for VGLNA and RSSI+EA, respectively, from a 1.2 V supply.

IV. Conclusion

A low power, high performance, and automatically gain controllable LNA (AGC-LNA) for FM receiver (FMRx) is reported. By the adoption of a current-reused dual gm-boosting, the proposed LNA achieves low power consumption. And, analog type automatic gain control loop is proposed that simplify the implementation with high resolution gain control. Implemented in a 65 nm CMOS technology, measurements show 40 dB of closed loop power regulation range with ±1 dB error, less than −11 dB for S11, variable voltage gain range of −12 to 30 dB over the frequency range of 88∼108 MHz, noise figure (NF) of less than 2.9 dB, P1dB of higher than −24.2 dBm, and IIP3 of higher than −12.7 dBm in the high gain (HG) mode, while dissipating only 1.8 mA frvom a 1.2 V supply, respectively.

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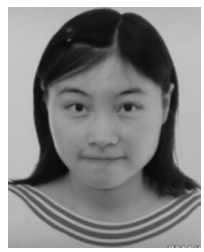

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