Spur Reduction Techniques With a Switched-Capacitor Feedback Differential PLL and a DLL-Based SSCG in UHF RFID Transmitter

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***Abstract*—This paper presents a robust spur reduction technique using a switched-capacitor feedback differential phase-locked loop (PLL) and a delay-locked-loop (DLL)-based spread-spectrum clock generation in a UHF-band RF identification transmitter (TX). The proposed differential PLL is characterized by adopting a switched-capacitor common-mode feedback and distributed varactor biasing scheme to the differential charge pump and voltage-controlled oscillator designs, respectively, which results in down to −94 dBc in reference spur rejection with all digital parts off. Additionally, by adopting an 8-bit DLL and Hershey-Kiss modulated profile together, the proposed spread-spectrum clock generator shows more than 20-dB electromagnetic-interference reduction while providing up-, down-, and center-spread modes. Implemented in a 0.18-μm CMOS process, the proposed TX achieves $< -$ 80-dBc spur suppression with 25-dBm transmit power at 920 MHz, which complies with the most stringent regulatory spectral mask without a surface acoustic wave filter.**

***Index Terms*—Differential phase-locked loop (PLL), distributed varactor biasing, electromagnetic-interference (EMI) reduction, RF identification (RFID), spread-spectrum clock generator (SSCG), spur rejection, surface acoustic wave (SAW)-less transmitter (TX), switched-capacitor common-mode feedback (SC-CMFB).**

I. Introduction

As THE demand for fully integrated system-on-chip (SoC) solutions continues to grow, there has been increased interest in the analog/digital coexistence issue in relation to system design. Although SoC generally offers advantages of lower power and cost compared to multi-chip solutions, it inevitably suffers from radiated electromagnetic interference (EMI) due to digital switching noise. The EMI is prone to turn into spurious single tones at the harmonic frequencies of the clock signal, and consequently threatens the reliability of data processing in RF and analog circuits in the wireless transceiver. Fig. 1 describes the spectrum mask in an ARIB-T107 standard set by regulatory agencies from Japan, which has the most stringent specification requirements of UHF band RF identification (RFID) applications; i.e., a spur level of $< -$ 79 dBc with 24-dBm transmit power [1]. To satisfy this specification, spur rejection in the analog part of the SoC is required, as well as that from EMI in the digital part. In general, as shown in Fig. 1, the reference spur at f_0 and digital switching spur at $2f_0$ are the most crucial factor violating the spectral mask requirement in wireless transceiver design. In order to overcome this spur issue, most industrial RFID transmitters (TXs) are accompanied by external components such as surface acoustic wave (SAW) filters. However, the external SAW filter increases manufacturing and assembly costs. In order to suppress the reference spur at f_0 without SAW filters the differential phase-locked loops (PLLs) are widely used. In a differential phase-locked loop (DPLL), the op-amp based common-mode feedback (CMFB) is preferred to reduce up/down current mismatch in the charge pump (CP) that is one of the main causes of the reference spur [2]. However, even if the op-amp-based CMFB mitigates up/down current mismatch, differential error in the DPLL still needs to be resolved [3]. Meanwhile, as a simple and straightforward solution to alleviate the EMI, a spread-spectrum clock generator (SSCG) has been reported [4], [5]. An SSCG varies the clock frequency with continuous up/down modulation, thus

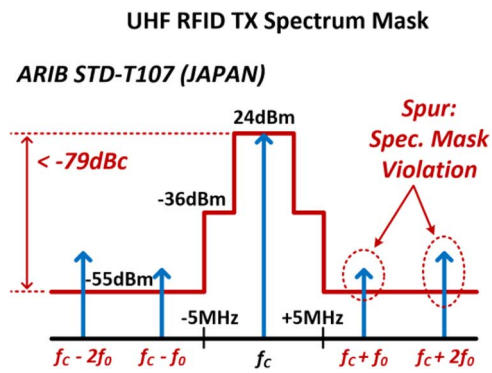

Fig. 1. Spectrum mask in ARIB-T107 standard.

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decentralizing the concentrated spectrum such that the radiated power level in a given bandwidth is reduced. In our previous work [6], the SSCG based on a delay-locked loop (DLL) was proposed for EMI reduction and manifested its effectiveness satisfying the ARIB-T107 spectrum mask. However, since reduction of the reference spur in the PLL is also significant, the explanation how to reduce the reference spur should have been discussed in [6]. In this paper, a spur reduction technique for a 920-MHz UHF-band RFID TX using a switched-capacitor common-mode feedback differential phase-locked loop (SC-CMFB PLL) in addition to the DLL-based SSCG is presented. The TX complies with the UHF-band RFID spectral mask specification without requiring a SAW filter. In the proposed PLL, the differential CP minimizes differential errors by adopting SC-CMFB, while the op-amp-based CMFB helps to match its up/down current. The main advantages of SC-CMFBs are that they impose no restrictions on the maximum allowable differential input signals, have no additional parasitic poles in the CM loop, and are highly linear [7]. Additionally, contrary to the structures utilizing op-amps or other active circuits [3], SC-CMFB has benefits in the aspects of power consumption, design complexity, and loop stability since it is all composed of passive elements such as capacitors and switches. Moreover, the distributed varactor biasing scheme [8] is adopted in the differential voltage-controlled oscillator (VCO) for better spur rejection through more linearized and differential tuning curve. Apart from the spur reduction in analog part of the TX, the SSCG helps to reduce EMI from digital switching noise. The proposed SSCG is implemented with a direct digital phase domain modulation (DDPM) scheme along with a 256 phase generator, an 8-bit DLL, and a Hershey-Kiss (H-K) profile generator, and thereby provides robust EMI reduction in conjunction with area efficiency. This paper is organized as follows. Sections II and III depict the TX architecture and SC-CMFB DPLL, respectively. Sections IV and V describe operating principle and implementation details of the proposed SSCG. Finally, Section VI presents experimental results and Section VII concludes this paper.

II. TX Architecture

Fig. 2 presents a block diagram of the presented RFID TX. As shown in the figure, the TX adopts a mixer based direct conversion architecture that consists of a baseband modem, a 9-bit digital-to-analog converter (DAC), a low-pass filter (LPF) for channel selection, an up-mixer, and a driving amp (DA) along with an external power amp (PA) that amplifies signals to a level appropriate for transmission (>25 dBm). The TX is designed to satisfy the spur specification at 25-dBm PA output power in ARIB-T107 by utilizing a DPLL and SSCG. For ARIB-T107 specification, the spurs from both the PLL reference clock in the analog part and EMI in the digital part should be considered simultaneously. For the spur rejection in the analog part, a DPLL is adopted, while a DLL-based SSCG suppresses the spurs from EMI in the digital part. The proposed DPLL is characterized by the structures of the differential CP using SC-CMFB and the differential VCO with linearized tuning curves. The SC-CMFB-based CP reduces its differential errors without extra power consumption or stability

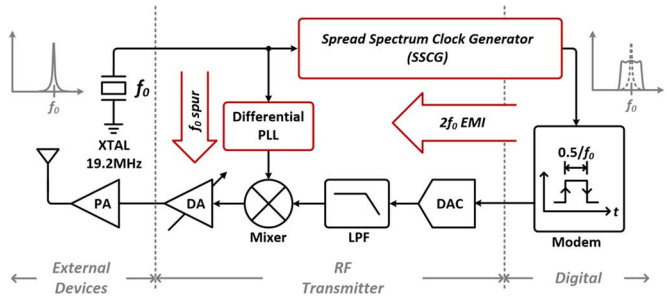

Fig. 2. TX architecture.

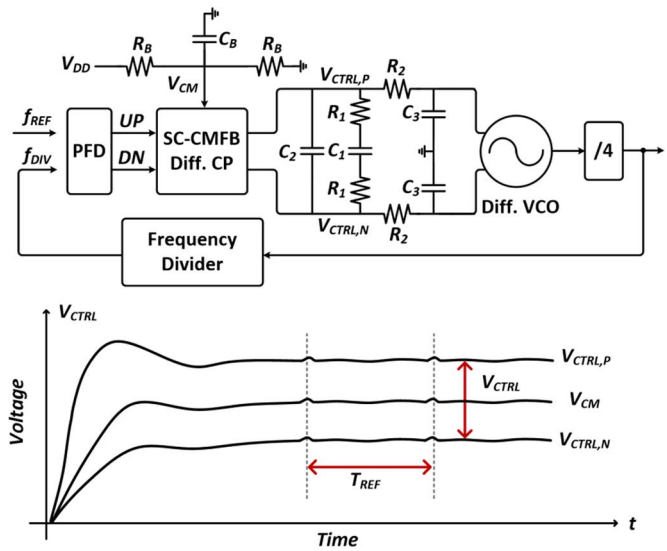

Fig. 3. Architecture and operating principle of DPLL.

issues by using only passive elements, while the conventional CPs utilize active circuits including op-amps. Besides, the distributed varactor biasing scheme is adopted in VCO design, which linearizes the frequency tuning curves. This facilitates the design of differential tuning curves in the VCO to be more accurate and thereby optimizes the spur rejection performance of the DPLL. Contrary to the conventional SSCG, the proposed SSCG is designed based on the DLL and suppresses the spurs at $2f_0$ by reducing EMI in the digital part of the SoC through the H-K modulation profile [5]. Since the switching clock in SC-CMFB circuits and the operating clock in the SSCG share the reference clock of the PLL, an additional clock generation is unnecessary.

III. DPLL Utilizing SC-CMFB CP

Fig. 3 shows the block diagram and operating principle of the proposed DPLL. As seen in Fig. 3, the proposed DPLL is comprised of a tri-state phase-frequency detector (PFD), an SC-CMFB differential CP, a loop filter (LF), a differential VCO, and frequency dividers. A delta–sigma modulator (DSM) is not depicted in the figure, but digitally integrated. Fig. 3 shows the operating principle of the DPLL. A DPLL suppresses the reference spurs, caused by CP differential errors or directly passed through supply paths, by designing VCO tuning curves in a differential configuration. For a better spur rejection, as seen in Fig. 3, the control voltages of the differential VCO, $V_{\mathrm{CTRL},P}$

and $V_{\mathrm{CTRL},N}$, should be settled symmetrical to the common-mode voltage, V_{CM}. For this, the differential errors in the CP have to be reduced in advance. In addition, the frequency tuning curves in a differential VCO should also be linear so that the DPLL can achieve spur rejection regardless of the settling points of $V_{\mathrm{CTRL},P}$ and $V_{\mathrm{CTRL},N}$. According to [2], the amount of the reference spur in the PLL, P_{RS}, is given by

$$P_{\mathrm{RS}} = 20\log\left[\frac{\sqrt{2}(I_{\mathrm{CP}}R_1/2\pi)\Phi_\varepsilon K_{\mathrm{VCO}}}{2f_0}\right] - 20\log\frac{f_0}{f_{P\_\mathrm{LF}}} \tag{1}$$

where I_{CP}, R_1, Φ_ε, K_{VCO}, f_0, and f_{P_LF} are the CP current, the resistor value in the LF, the amount of the phase offset by up/down current mismatch in the CP, VCO gain, the reference frequency for the PFD, and the pole frequency of the LF, respectively. As seen in (1), in order to reduce the reference spurs, it is helpful to decrease the CP current, VCO gain, and the pole frequency of the LF or increase the reference frequency. However, the increase of f_0 is not desirable due to the cost of XTAL and EMI increase, while the decrease in I_{CP} or f_{P_LF} is restricted owing to phase noise and speed degradation in the PLL. On the other hand, since a decrease in K_{VCO} is desirable in phase-noise performance, it can be beneficial to realize spur rejection by using a multi-bit capacitor bank in the VCO design. The proposed PLL is characterized by the structures of the differential CP and VCO. The proposed CP is designed utilizing an op-amp-based up/down current matching technique [2] and minimizes its differential errors by adopting SC-CMFB. The differential VCO is basically designed in a differential varactor structure where each varactor cell is more linearized by distributed varactor biasing scheme [8]. This linearization allows the differential frequency tuning curves to be more symmetrical regardless of the control voltage of the VCO.

A. SC-CMFB Differential CP

Fig. 4 describes the schematic of SC-CMFB circuits and its modeling for principle understanding. As seen in Fig. 4, C_{A+} is charged by the amount of $C_{A+} \times V_{\mathrm{DC}}$ during Φ_1 and delivered to C_{B+} during Φ_2, which leads to voltage level shifting at output nodes. Thereby, C_{B+} is precharged, as seen in Fig. 5(a), and this can be modeled as seen in Fig. 5(b). The bias voltage V_{CMFB} can be calculated as follows:

$$V_{\mathrm{CMFB}} = \frac{(C_{B+}V_1 + C_{B-}V_2)}{(C_{B+} + C_{B-})}. \tag{2}$$

Since $V_1 = V_{\mathrm{CTRL},P} - V_{\mathrm{DC}}$ and $V_2 = V_{\mathrm{CTRL},N} - V_{\mathrm{DC}}$, assuming $C_{B+} = C_{B-}$, (2) yields

$$\begin{aligned} V_{\mathrm{CMFB}} &= \frac{(C_{B+}V_{\mathrm{CTRL},P} + C_{B-}V_{\mathrm{CTRL},N})}{(C_{B+} + C_{B-})} - V_{\mathrm{DC}} \\ &= \frac{(V_{\mathrm{CTRL},P} + V_{\mathrm{CTRL},N})}{2} - V_{\mathrm{DC}} \\ &= V_{\mathrm{CM}} - V_{\mathrm{DC}} \end{aligned} \tag{3}$$

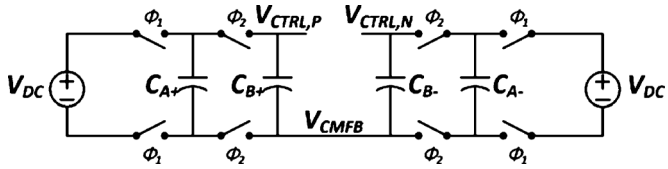

Fig. 4. Schematic of SC-CMFB circuits.

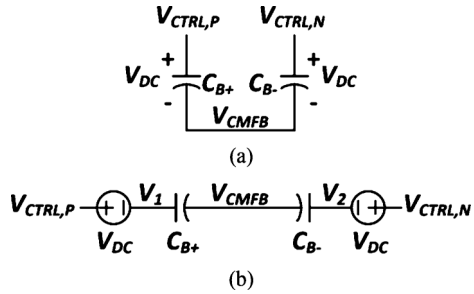

Fig. 5. Operating principle and modeling of SC-CMFB.

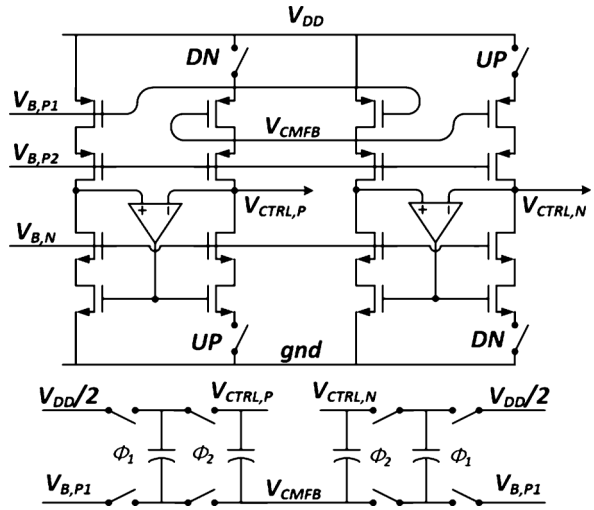

Fig. 6. Schematic of SC-CMFB DPLL.

where $V_{\mathrm{CM}} = (V_{\mathrm{CTRL},P} + V_{\mathrm{CTRL},N})/2$ is the output common-mode voltage. Therefore, it is evident that the output common-mode sensing and comparison are achieved [7]. Fig. 6 shows the schematic of the proposed differential CP. Based on the op-amp CMFB, the up/down currents are matched regardless of output voltage variation. As mentioned earlier, SC-CMFB is utilized to minimize differential error without additional power consumption and stability issues. Since the VCO is designed to have the center point of its tuning curve at $V_{DD}/2$, the reference voltage is set to be $V_{DD}/2$. Therefore, during the first phase Φ_1, the voltage, $V_{DD}/2 - V_{B,P1}$, is charged to the capacitor and finally generates the proper CMFB voltage, V_{CM}-V_{DC}. For switching in the SC-CMFB circuit, the reference clock of the PLL is co-used without additional clock generation. Since the bandwidth of the LF is set to 10 kHz, 19.2 MHz of the reference clock does not degrade spur characteristics.

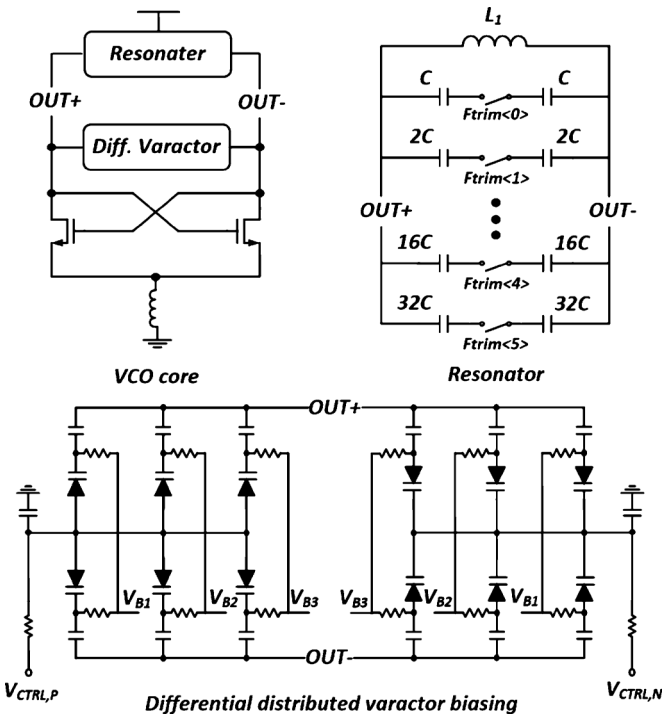

Fig. 7. VCO structure with distributed varactor biasing.

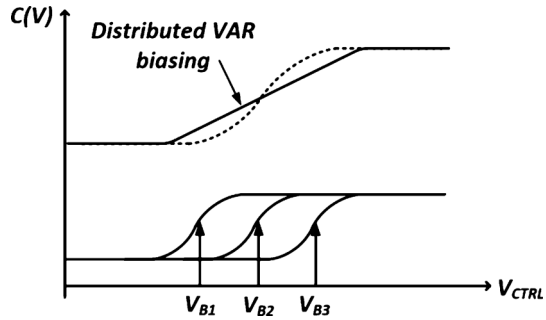

Fig. 8. Operating principle of distributed varactor biasing scheme.

TABLE I
VCO DESIGN PARAMETERS

Operation frequency	3.1 – 4.1 GHz
VCO gain (K_{VCO})	10 ~ 20 MHz/V
L	2.2 nH
C	223 fF ~ 1.65pF
Q factor of resonator	13.3
Supply voltage	2.5 V
Current consumption	27 mA

TABLE II
PASSIVE ELEMENT VALUES IN LF

R_1	R_2	C_1	C_2	C_3
4.7 kΩ	8 kΩ	16.5 nF	2.2 nF	80 pF

B. Differential VCO With Distributed Varactor Biasing

Fig. 7(a) describes the schematic of the differential VCO. The VCO is basically designed in an nMOSFET-only structure with inductive source degeneration. In the resonator design, a symmetrical spiral inductor and 6-bit capacitor bank are used. For reference spur rejection, as well as common-mode noise suppression, we utilize differentially tuned varactors where the distributed varactors are biased independently to have more linear frequency tuning curve. For a given frequency tuning range, a single varactor presents a relatively higher VCO gain ($K_{\rm VCO}$) variation up to the control voltage and further nonlinear tuning curve than those of the distributed varactor biasing scheme. An excessive variation in $K_{\rm VCO}$ causes PLL loop gain variation and finally leads to PLL stability issues. In addition, nonlinear $K_{\rm VCO}$ disturbs the differential configuration of frequency tuning curves in VCOs. Since the differential error reduction in $K_{\rm VCO}$ is also as important as that in the CP for reference spur rejection, the linearization of the tuning curve is significant. Fig. 8 is the principle of the distributed varactor biasing scheme. As seen in Fig. 8, each of the varactors in Fig. 7(a) is biased to V_{B1}, V_{B2}, and V_{B3}, respectively, and thereby the corresponding tuning curves are shifted so that the total capacitance variation up to the control voltage becomes more linear. The combination of differential error minimization in the CP and VCO tuning curves eventually results in reference spur rejection. The design parameters including $K_{\rm VCO}$, operation frequency, the values of elements in resonators, and power consumption are summarized in Table I.

C. Frequency Dividers and LF

The frequency dividers in the feed-through path and in the feed-back path in Fig. 3 are designed in current-mode-logic (CML) and dual modulus types, respectively. The LF is basically designed in second order, but one more R-C network is added to further suppress the reference spur. For 10 kHz or there about PLL bandwidth, the external passive elements are used, except R_2 and C_3. The passive element values of the LF in Fig. 3 are summarized in Table II.

IV. PRINCIPLE OF DDPM IN SSCG

Fig. 9 shows the operating principle of the DDPM scheme. As seen in Fig. 9, the DDPM allows to achieve spread-spectrum function by shuffling the multiple equi-spacing (ΔT) delay taps with a phase-modulated multiplexer (MUX) [4]. Even though the DDPM scheme has benefits in area and power aspects by eliminating the use of the bulky PLL, it requires an infinite number of phases owing to its inherent characteristic of phase modulation. As can be seen in Fig. 3, since the phase is persistently accumulated, the phase modulation can be extended to infinity in the time domain while the frequency modulation ($f_{\rm MOD}$) keeps changing up and down within a limited boundary. In order to realize an infinite number of phases, a phase-wrapping technique was developed in [4]. This technique utilized a finite number of delay cells instead of an infinite number of delay cells, where the wrap-around is done moving back by the number of taps per period. However, as the calibration logic operates adjusting the number of delay cells rather than the amount of delay, this technique raises the digital

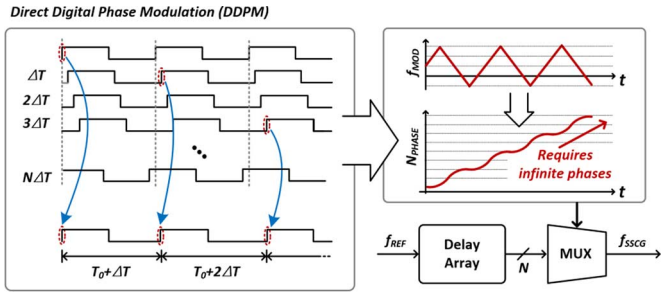

Fig. 9. Operating principle of DDPM scheme.

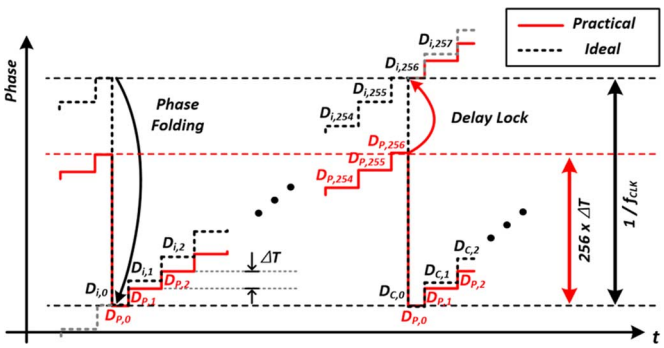

Fig. 10. Conceptual timing diagram of the proposed delay calibration algorithm.

processing complexity as well as requires additional peripheral circuits such as clock edge monitoring modules and delay compensators. In [6], we proposed a DLL-based phase-calibration technique that adjusts the amount of the unit cell delay allowing spread-spectrum function with a limited number of delay cells. In the proposed technique, the digital processing complexity can be alleviated by deciding the number of delay cells in a binary manner, 2^N. Moreover, it does not require any clock monitoring circuit due to its inherent recursive phase properties. Fig. 10 shows the conceptual timing diagram of the proposed DLL-based delay calibration algorithm. As seen in Fig. 4, in case of using an 8-bit delay, the last phase (D_{256}) is folded to the first phase (D_0) by maintaining the total delay equal to the clock period. In the proposed DLL, D_0 and D_{256} are compared to make an order to control the subsequent 8-bit digital logic. Thus, the delay amount, ΔT, is calibrated to $T_{\mathrm{CLK}}/256$ and leads to seamless phase continuity in spite of PVT variation and different operating conditions.

V. Implementation of DLL-Based SSCG

Fig. 11 shows a block diagram of the proposed DLL-based SSCG. The proposed SSCG can be separated into three blocks; i.e., delay cell array (DCA), DLL, and modulator profile generator (MPG). While the DCA generates a total of 256 phases by using 128 differential delay cells, the DLL accurately aligns the phase from D_0 and D_{256}. After the calibration in the DLL is completed, the MPG begins to generate an 8-bit modulation code (P_{MOD}). In order to achieve better EMI reduction, the MPG generates an H-K modulation profile by utilizing the slope-modulation technique [5]. An 8-bit MUX in the DCA then finally synthesizes the output spread-spectrum clock (f_{SSC}) by shuffling the phases in accordance with P_{MOD}.

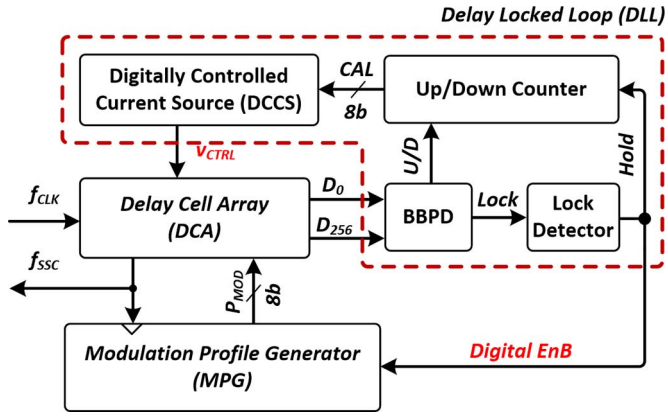

Fig. 11. Block diagram of the proposed DLL-based SSCG.

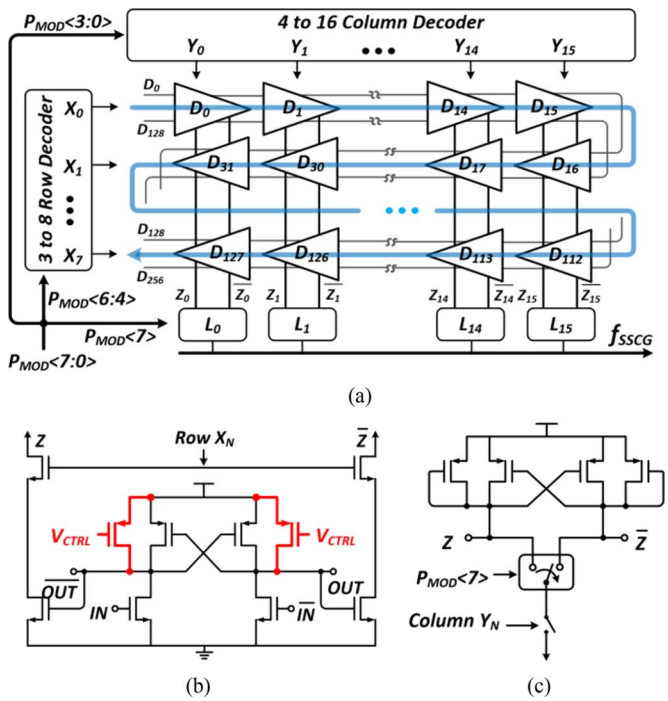

Fig. 12. (a) Block diagram of DCA, (b) UDC, and (c) load cell.

A. DCA

Fig. 12 describes the block diagram of the DCA, its unit delay cell (UDC), and the load cell. As seen in Fig. 12(a), the DCA is composed of 16×8 UDCs and 16 load cells along with logic decoders. In the DCA, the UDCs are arranged in a zigzag manner to minimize an abrupt delay change between delay cells in a row-switching operation. The 8-bit phase-modulation code, $P_{\mathrm{MOD}}\langle 7:0\rangle$, is divided into three components ($P_{\mathrm{MOD}}\langle 7\rangle$, $P_{\mathrm{MOD}}\langle 6:4\rangle$, $P_{\mathrm{MOD}}\langle 3:0\rangle$) and utilized to drive the differential switch in the load cell, 3-bit row decoder, and 4-bit column decoder, respectively. As shown in Fig. 12(b), the UDC is designed with two nMOS transistors driven with a differential signal from the previous cell where the load consists of a pair of cross-coupled pMOS along with another pair of current driven pMOS whose current is adjusted by V_{CTRL}. The outputs of each UDC are connected to a subsequent nMOS transistor that is accompanied by a cascode switch for the row selection

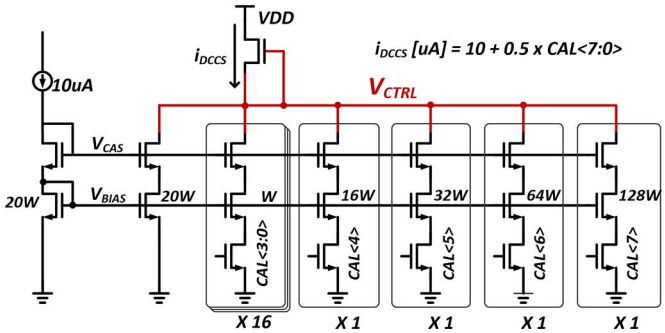

Fig. 13. Schematic of DCCS.

of the DCA. Thus, each UDC drives the same load despite the change in the MUX. As can be seen in Fig. 12(c), the same configuration of the load as that of the DCA is connected to the nodes, Z and $\overline{Z}$, for the column selection. The DCA consumes 23.5 mW of average power from a 1.8-V supply.

B. DLL

The DLL in Fig. 11 is composed of a bang–bang phase detector (BBPD), an 8-bit up/down counter, a lock detector, and a digitally controlled current source (DCCS). Similar to the conventional digital DLL, the BBPD compares D_0 and D_{256} and then delivers an up/down order sign to the subsequent 8-bit counter. The up/down counter generates an 8-bit calibration code to the DCCS and eventually produces the control voltage, V_{CTRL}. Fig. 13 describes the schematic of the DCCS. As seen in Fig. 13, the DCCS consists of switch-controlled nMOS cascade current sources with a pMOS diode load. It is noted that the 4-bit least significant bit (LSB) is converted into a thermometer code to improve the monotonicity by driving the identical current cell while the 4-bit MSB sustains its intrinsic binary format. The DCCS-controlled current is set as $i_{\mathrm{DCCS}}\ [\mu\mathrm{A}] = 10 + 0.5 \cdot \mathrm{CAL}\langle 7:0\rangle$, where $\mathrm{CAL}\langle 7:0\rangle$ is an 8-bit code of the up/down counter. Moreover, a lock detector is used to eliminate the voltage-sensitive jitter by preserving the value after delay calibration. Once the difference between D_0 and D_{256} is small enough not to differentiate, the BBPD produces a lock signal and then the subsequent lock detector generates a hold flag to cut the calibration loop in the case where four lock signals are generated in series. The DLL consumes 210 μW from 1.8-V supply.

C. Modulation Profile Generator

As shown in Fig. 14(a), the MPG consists of a triangular generator, a 20-bit accumulator, a DSM, and a 8-bit accumulator. The MPG in Fig. 11 starts to generate the modulation code in accordance with the enable signal from the lock detector after the delay calibration is completed. In order to alleviate the edge concentrated spectrum power in a triangular profile, a nonlinear modulation profile called an H-K [9] is utilized. The H-K modulation profile is well known as an optimal modulation profile for spread-spectrum clock generation when the modulation frequency is below the resolution bandwidth (RBW) of the spectrum analyzer [10]. Fig. 14(b) shows the corresponding timing

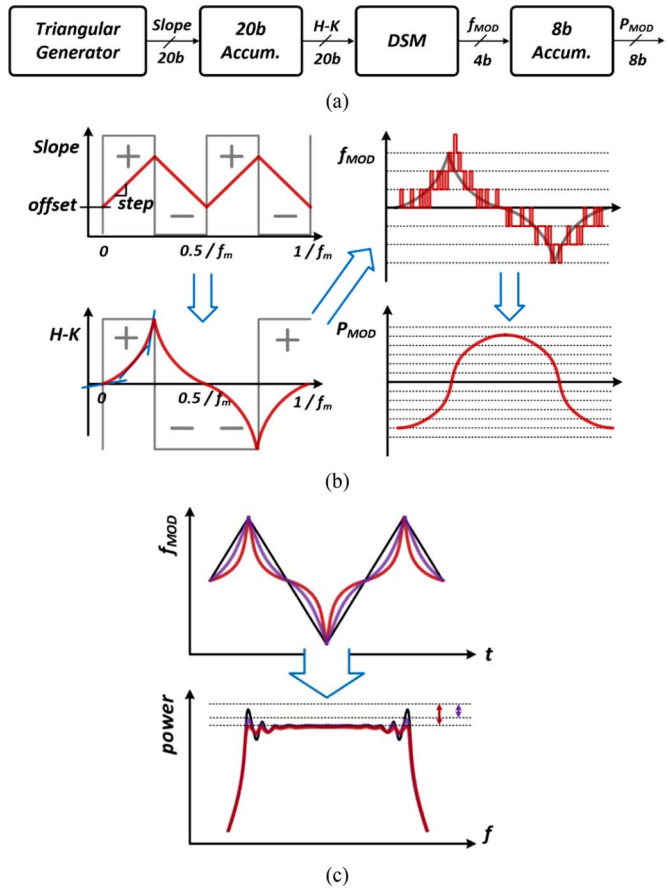

Fig. 14. (a) Block diagram of MPG, (b) timing diagram of MPG, and (c) effect of H-K profile.

diagram of each constituting block in the MPG for H-K profile generation. As can be seen in Fig. 14(b), the triangular generator first produces a slope profile with a double modulation frequency $2f_0$ that is constrained to the starting point, *offset*, and the unit incremental size, *step*. A subsequent 20-bit accumulator then generates the H-K profile by integrating the output of the slope generator with a modulation frequency of f_0. The two design constraints in the slope generator (*offset* and *step*) are utilized to adjust the instantaneous slope of the H-K modulation profile, which affects the edge-concentrated spectrum power. As shown in Fig. 14(c), the edge-concentrated power is more reduced while the instantaneous slope of the H-K profile changes more radically. Following the 20-bit accumulator, the DSM is utilized to quantize the 20-bit H-K modulation profile into a 4-bit length frequency profile. Thereafter, an 8-bit accumulator, whose number of bits corresponds to the number of phases in the DCA, converts the frequency profile (f_{MOD}) to a direct phase profile (P_{MOD}). This P_{MOD} is fed back to the DCA and finally the spread-spectrum clock, f_{SSC}, is achieved.

VI. Experimental Results

Fig. 15 shows the measured waveform and timing diagram of the MPG, the measured peak power reduction from the H-K modulation profile, and frequency spread modes of the proposed SSCG. As seen in Fig. 15(a) and (b), each block in the MPG generates the expected results, as explained in Section V-C, while the phase calibration completes within

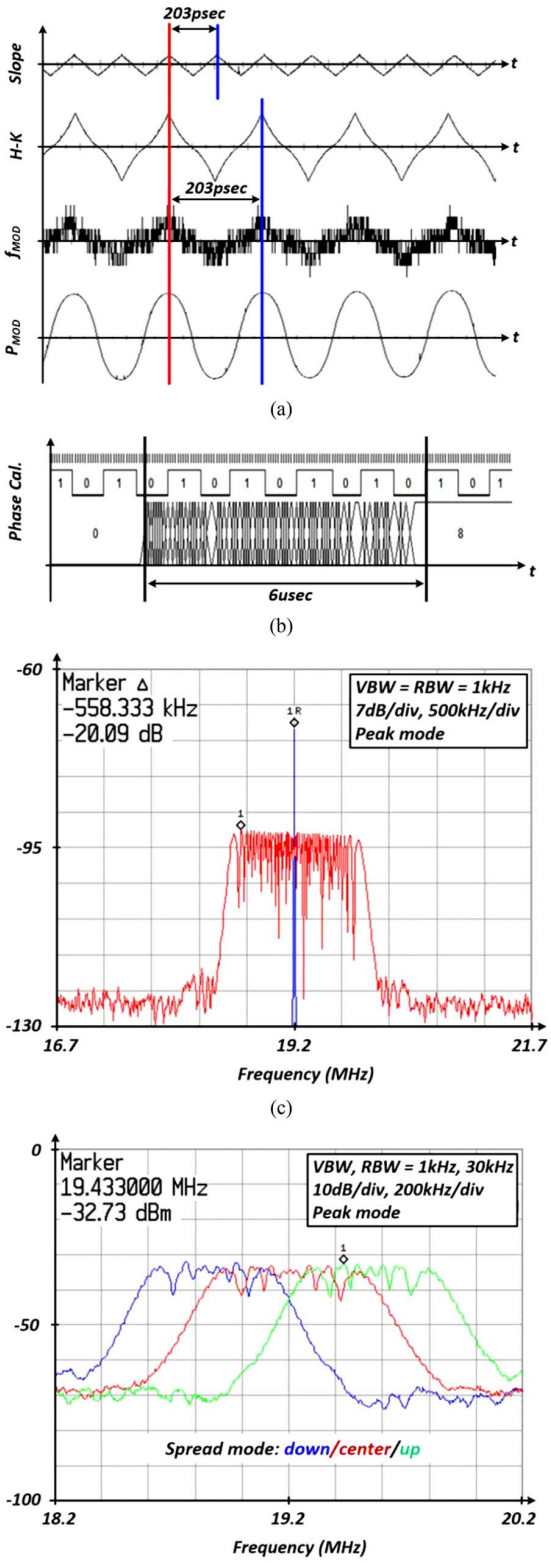

Fig. 15. Measured: (a) waveform and (b) timing diagram of MPG, (c) peak power reduction from H-K modulation profile, and (d) frequency spread modes of SSCG.

6 μs. After calibration, ΔT is set to $1/19.2\ \text{MHz}/256 = 203$ ps at 19.2-MHz operating frequency. The measured peak power reduction in Fig. 15(c) reaches more than 20 dB in 7% deviation setup at 19.2-MHz operating frequency. Fig. 15(d) proves that the proposed SSCG offers an up/center/down spread mode.

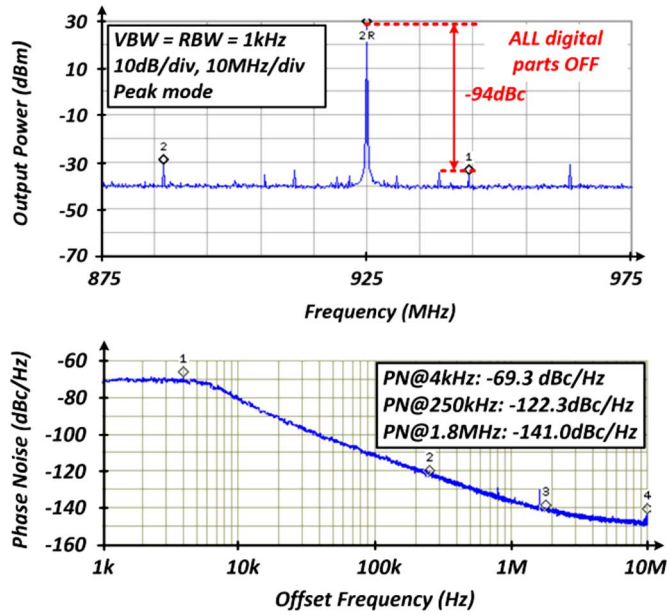

Fig. 16. Measured reference spur rejection (digital off) at 29-dBm Tx output power and phase noise in PLL.

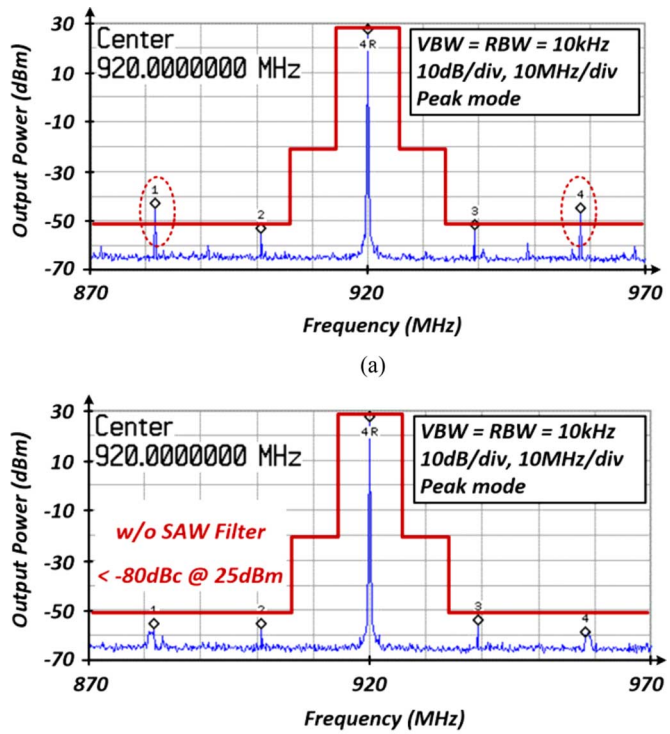

Fig. 17. Measured: (a) spur rejection without SSCG and (b) with SSCG in TX.

As for spur rejection, we measured three cases: the reference spur rejection when all digital part turns off and spur rejection when the analog and digital parts turn on with SSCG-off and SSCG-on. The purpose for three cases of spur measurement is to identify the source of spurs up to frequency as well as distinguish the spur-rejection contributions of the proposed SC-CMFB PLL and DLL-based SSCG. Fig. 16 shows the measured reference spur rejection in the PLL at 925-MHz operating frequency when only the analog part of the SoC turns on. As seen in the figure, the reference spur rejection at f_0 (19.2

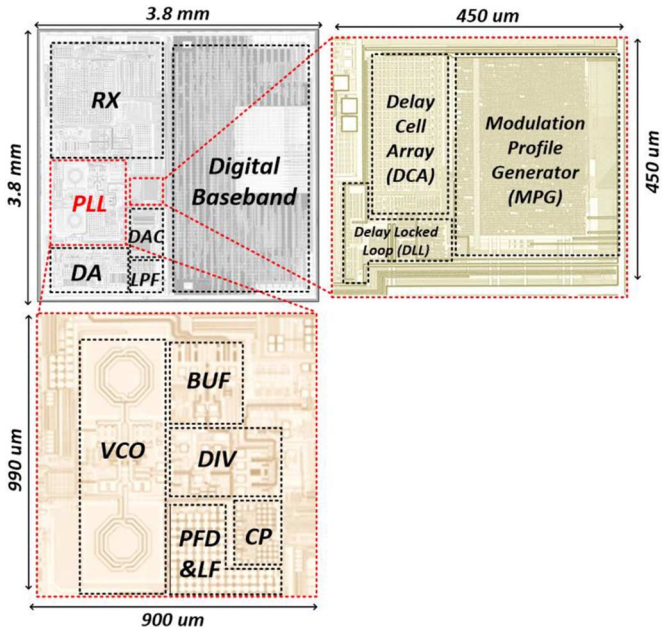

Fig. 18. Micrographs of TX, SC-CMFB PLL, and DLL-based SSCG.

MHz) is measured down to -94 dBc, while the rejection at $2f_0$ reaches down to -87 dBc at 29-dBm TX output power. This proves that the proposed DPLL suppresses the reference spurs enough to satisfy the spur specification in ARIB-T107. When all digital parts, except the SSCG, turns on in Fig. 17(a), both spurs at f_0 and $2f_0$ are raised. Especially for the $2f_0$ spur, spur rejection performance is more degraded. Finally, when all parts of the SoC including the proposed SSCG turn on, all the spurs are mitigated down to < -80 dBc at 25-dBm TX output power, which satisfies ARIB-T107 spur specification. As can be seen in Fig. 17(b), it is intuitively noted that the spectrum of the spurs at $2f_0$ is spread around and its peak power reduced more than 10 dB. From these three measurements, we can recognize that the DPLL dominantly contributes the spur rejection at f_0, while the SSCG does at $2f_0$. The proposed UHF-band RFID TX is implemented in a 0.18-μm CMOS process. The proposed PLL dissipates 40 mA from 2.5-V supply while all digital part including the SSCG operates at 1.8-V supply. The reason for using a higher supply in the PLL is due to the tight phase-noise specification in the ARIB-T107 specification that is not discussed in this paper. Besides, the VCO and CP use separate voltage regulators in order to avoid the spur transfer through the supply path. Fig. 18 shows a micrograph of the fabricated chip. The single-chip RFID SoC including the TX, RX, modem, and processor occupies 3.8 mm $\times$ 3.8 mm, while the proposed DPLL and SSCG occupy 990 μm $\times$ 900 μm and 450 μm $\times$ 450 μm, respectively.

VII. Conclusion

This paper has presented a spur reduction technique for a UHF-band RFID TX using an SC-CMFB-based DPLL and a DLL-based SSCG. The proposed DPLL is characterized by adopting the SC-CMFB and distributed varactor biasing scheme to the differential CP and VCO designs, respectively. The analog parts of the SoC show down to -94 dBc in reference spur rejection performance at 29-dBm TX output power when all digital part turns off. Additionally, the proposed DLL-based SSCG reduces the spurious harmonic of the reference clock f_0 due to the suppression of EMI from digital circuits. By adopting an 8-bit DLL and H-K modulated profile together, the SSCG shows more than 20-dB EMI reduction while providing the up/down/center spreading mode. Implemented in a 0.18-μm CMOS process, the proposed spur rejection technique allows to achieves < -80-dBc spur suppression with 25-dBm transmit power at 920 MHz in the TX, which complies with the most stringent regulatory spectral mask without a SAW filter.

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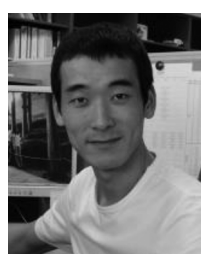

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