A 24 GHz Highly Linear Up-Conversion Mixer in CMOS 0.13 μm Technology

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***Abstract*—This letter reports a 24 GHz linear up-conversion mixer for high-power IF signal. In the proposed mixer, the double-balanced Gilbert-cell topology is employed with a low-distortion transconductance stage which combines voltage feedback and adaptive biasing schemes. The proposed adaptive biasing circuit improves the linearity of the transconductance stage by providing an additional bias current when IF input signals exceed the current-limited linear input range. Implemented in a 0.13 μm CMOS technology, the mixer showed a conversion gain of -1.9 dB and output 1 dB compression point of 0.3 dBm for the IF, LO, and RF frequency ranges of 10.0–314.7 MHz, 18.9–29.0 GHz, and 23.4–29.2 GHz, respectively, while dissipating 22.8 and 16.5 mW for the mixer and the LO buffer, respectively, from a 1.5 V supply.**

***Index Terms*—Adaptive biasing, linear circuits, mixers, on-chip transformers, transconductance, voltage feedback.**

I. Introduction

THE ever increasing markets for wireless communication and radar technologies continue to drive extensive efforts to implement transceivers in CMOS technologies. In particular, demand for short-range radars has led to the active development of 24 GHz radar transceivers. However, to make the most of the maximum transmit power (20 dBm) in the 24 GHz industrial, scientific, and medical (ISM) band [1], SiGe BiCMOS or GaAs pHEMPT power amplifiers are usually used, rather than CMOS power amplifiers [2], while the rest of the radio is implemented in CMOS. As a result, a CMOS up-conversion mixer is often needed to drive an external power amplifier with a 50 Ω load, and must be designed to accommodate the required maximum power at the input of the power amplifier. The low output impedance of the up-conversion mixer leads to low conversion gain (CG), and often conversion loss, unless power consumption is very high. To satisfy the required output power under the low CG, large amplitude signals tend to be applied at the input of the up-conversion mixer, requiring high linearity. Many 24 GHz CMOS up-conversion mixers have been reported [3]–[7] whose linearity can still be improved.

In this work, a high-linearity up-conversion mixer for 24 GHz ISM band radar transceivers is reported. To increase linearity, focus was placed on improving the linearity of the transconductance stage as it tends to dominate the mixer linearity when the amplitude of the LO signal is sufficiently large [8]. Section II describes the design details of the proposed mixer, and Section III shows the measurement results. Section IV concludes.

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II. Mixer Design

Fig. 1 shows the schematic of the proposed up-conversion mixer including an LO buffer. The up-conversion mixer employs a double-balanced Gilbert-cell topology, which consists of transconductance, switching, and load stages. The transconductance stage adopts voltage feedback loops ($M_1 - M_6$) [9] in combination with the proposed adaptive biasing (AB) circuit ($M_{A1} - M_{A4}$). By adopting of the proposed AB circuit, currents (i_1 and i_2) flowing through M_1 and M_2 can be linear to the input voltage (v_{in}) for a wider input range than the original range limited by $I_{SS}/2$. As shown in Fig. 1, i_1 and i_2 are mirrored to M_7 and M_8 with a current ratio of N. The output currents (N_{i_1} and N_{i_2}) of the transconductance stage are injected into the switching stage ($M_9 - M_{12}$), and steered by the LO signal that comes from the LO buffer. The load part of the proposed mixer consists of an on-chip 1.6:1 transformer (T_1), a resonating capacitor (C_1), and a shunt resistor (R_1). $C_2 - R_2$ in the LO buffer is implemented in the same way with an inductor (L_B). The CG of the proposed mixer is given by

$$CG = \frac{2\alpha}{\pi}\frac{N_P}{N_S}\frac{2N}{R_{SS}}R_L \tag{1}$$

where α is the conversion efficiency including the on-chip transformer loss, N_P/N_S is the turn ratio of the primary and secondary parts of T_1, R_{SS} is the source resistor, and R_L is the output impedance. By setting the proper values of N and R_{SS}, a desired CG can be achieved within the linear input range.

In the transconductance stage shown in Fig. 1, the current sources (I_{B1} and $I_{SS}/2$) determine the dc gate-source voltages of $M_1 - M_6$ that form the feedback loops. Since the gate-source voltages of M_3 and M_4 are fixed by $I_{SS}/2$, v_{in} is forced to appear across R_{SS} by the feedback loop [9]. Therefore, a linear current (v_{in}/R_{SS}) is generated and flows through M_1 and M_2. However, for the linear $V - I$ conversion, M_1 and M_2 have to operate in the saturation region, assuming that $I_{SS}/2$ is sufficiently large. When the increase in v_{in} causes M_2 to enter triode mode operation, the gate voltage of M_2 has to be increased significantly to flow a large current in the triode region, thereby increasing the gate voltage of M_6; as a result, a bias current flowing through M_4 is reduced. Since the gate-source voltage of M_4 is decreased, the voltage across R_{SS} becomes different from v_{in} and the currents flowing through M_1 and M_2 are no

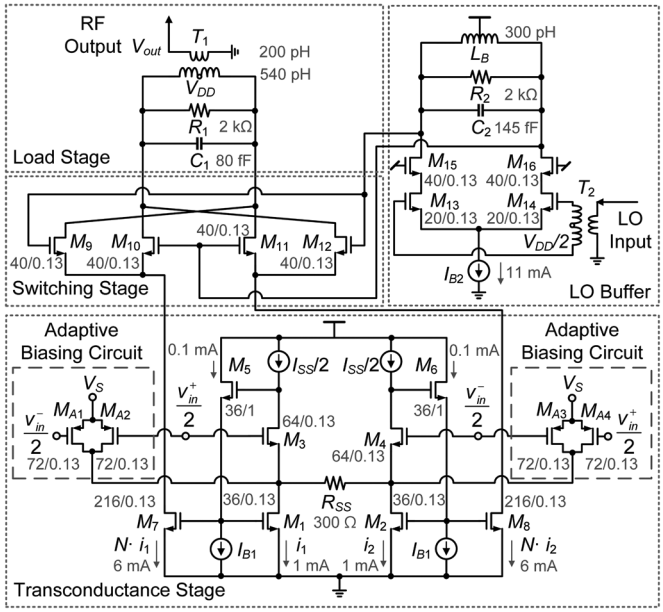

Fig. 1. Proposed up-conversion mixer.

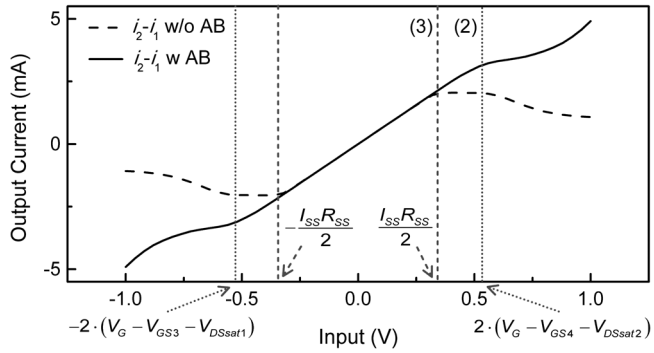

Fig. 2. Simulated differential currents $(i_2 - i_1)$ of transconductance stages.

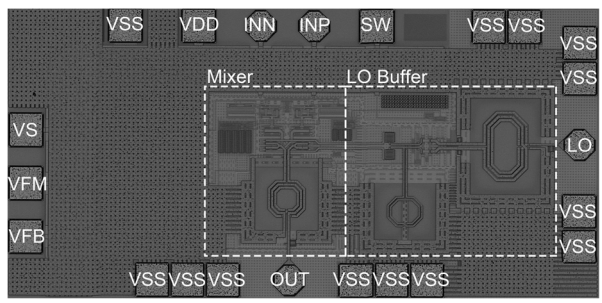

Fig. 3. Microphotograph.

longer proportional to v_{in}. Therefore, the linear input range is given by

$$-2(V_G - V_{GS3} - V_{DSsat1}) \le v_{in} \le 2(V_G - V_{GS4} - V_{DSsat2}) \tag{2}$$

where V_G is the gate bias voltage of $M_3 - M_4$ and $M_{A1} - M_{A4}$, and V_{GS3} and V_{GS4} are the gate-source voltages of $M_3$and M_4, and V_{DSsat1} and V_{DSsat2} are the overdrive voltages of M_1 and M_2.

However, in most cases, $I_{SS}/2$ is usually not enough to satisfy the range (2) for acceptable current consumption. Since the current flowing through R_{SS} is limited by $I_{SS}/2$, the voltage across R_{SS} cannot exceed $I_{SS}R_{SS}/2$. Therefore, the current-limited linear input range is given by

$$-\frac{I_{SS}R_{SS}}{2} \le v_{in} \le \frac{I_{SS}R_{SS}}{2}. \tag{3}$$

To improve the linear input range (3) without increasing $I_{SS}/2$, the proposed AB circuit was adopted in the feedback loop. Note that the linear input range can be improved by increasing R_{SS} as well, but then the CG given by (1) will be decreased.

As shown in Fig. 1, the proposed AB circuit $(M_{A1} - M_{A4})$ provides an additional current at the drain nodes of M_1 and M_2 when v_{in} exceeds the range shown in (3). In Fig. 1, the source voltages (V_S) of $M_{A1} - M_{A4}$ are set to

$$V_S = V_G + |V_{THP}| - \frac{1}{2}\frac{I_{SS}R_{SS}}{2} \tag{4}$$

where V_{THP} is the threshold voltages of $M_{A1} - M_{A4}$. Note that $I_{SS}R_{SS}/2$ in (4) represents the maximum linear input voltage shown in (3). If v_{in} is larger than $I_{SS}R_{SS}/2$, the source-gate voltages of M_{A1} and M_{A3} exceed $|V_{THP}|$, and M_{A1} and M_{A3} start to turn on with their drain currents given by

$$i_{A1} = i_{A3} = \frac{\mu_p C_{ox}}{8}\left(\frac{W}{L}\right)\left(v_{in} - \frac{I_{SS}R_{SS}}{2}\right)^2 \tag{5}$$

where μ_p is the hole mobility, C_{ox} is the gate oxide capacitance, W is the width of M_{A1} and M_{A3}, and L is the channel length of M_{A1} and M_{A3}. Then, due to the fixed gate-source voltages of M_3 and M_4 by $I_{SS}/2$, $(v_{in}/R_{SS} - I_{SS}/2)$ of i_{A1} in (5) flows through R_{SS} and the remainder of i_{A1} flows through M_1, while i_{A3} flows through M_2. The additional current flowing through R_{SS} enables v_{in} to appear across R_{SS}, even if v_{in} exceeds the range shown in (3). Thus, the linear input range with the AB circuit becomes wider than the value given in (3). However, when $|v_{in}|$ is large enough to drive M_1 or M_2 into the triode region, the differential current $(i_2 - i_1)$ starts to be distorted as mentioned earlier. Therefore, the linear input range of the transconductance shown in Fig. 1 is determined by the value shown in (2). Fig. 2 shows the simulated differential currents versus the amplitude of the input voltage for the transconductance stages with and without the AB circuit. As shown in Fig. 2, by adopting the AB circuit, the linear input range given by (3) is widened to that of (2) without increasing $I_{SS}/2$. Therefore, the overall mixer linearity can be improved by using the proposed transconductance stage.

III. Measurement Results

The proposed up-conversion mixer shown in Fig. 1 was implemented in a 0.13 μm CMOS technology. Fig. 3 shows the chip microphotograph; the core part of the mixer including the LO buffer occupies 1.32 mm $\times$ 0.65 mm. The mixer core and LO buffer consume 22.8 and 16.5 mW, respectively, from a 1.5 V supply. To compare the mixer performances with and without the AB circuit, V_S was connected to an external power supply. By setting V_S as a calculated value from (4) or 0 V, the AB circuit operates correctly or always off, respectively.

Measurements were obtained by a chip-on-board test, and capacitors of 0.2 pF were placed in series with bonding-wires at the RF and LO pads to cancel the inductance of the bonding-

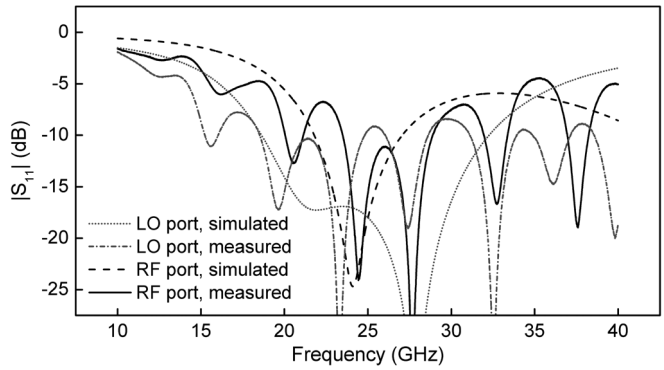

Fig. 4. Simulated and measured $|S_{11}|$ of RF and LO ports.

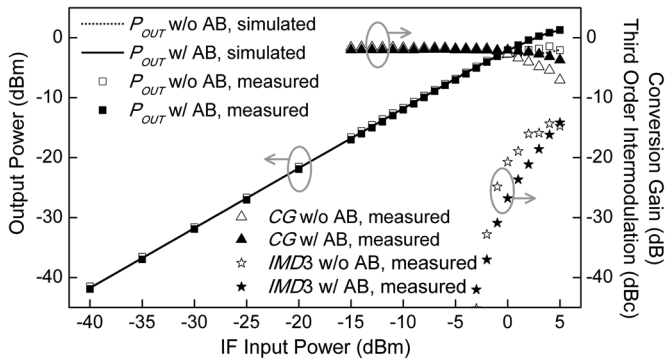

Fig. 5. RF output power, conversion gain, and third order intermodulation as a function of IF input power.

wire. Fig. 4 shows the simulated and measured $|S_{11}|$ of the LO and RF ports. As shown in Fig. 4, the measured results are below -10 dB over the frequency ranges of 18.9–29.0 GHz and 23.4–29.2 GHz for the LO and RF ports, respectively. For the IF input ports, the measured return loss is better than 10 dB over the frequency range of 10.0–314.7 MHz, whereas the measured 3 dB gain reduction bandwidth is 0.01–1.2 GHz. The measured LO-RF- and LO-IF-isolations are 28.9 and 68.9 dB, respectively.

Fig. 5 shows the RF output power (P_{OUT}), CG, and third order intermodulation $(IMD3)$ as a function of IF input power. For the P_{OUT} measurement, 24.125 GHz/0 dBm LO and 30 MHz IF signals were chosen, while for the $IMD3$ measurement, 20 and 30 MHz IF signals were utilized. The CG is saturated when the LO input power is around 0 dBm, which is increased to 4.7 dBm by the LO buffer. As shown in Fig. 5, the output 1 dB compression point (OP_{1dB}) and the CG of the mixer with the AB circuit are 0.3 dBm and -1.9 dB, respectively. With the AB circuit, the amount of OP_{1dB} improvement is 3.0 dB and $IMD3$ can be reduced at high power input (-2.5 to 5 dBm).

Table I summarizes the measured performance of the proposed up-conversion mixer in comparison with other recently reported up-conversion mixers [3]–[7]. For a fair comparison, the FoM in [10] is included, which is given by

$$FoM(dB) = 10\log\left(\frac{10^{\left(\frac{CG}{20}\right)}\cdot 10^{\left(\frac{OP_{1dB}}{20}\right)}}{\frac{P_{DC}}{1\text{ mW}}}\right) \qquad (6)$$

TABLE I
THE MEASUREMENT SUMMARY AND COMPARISON WITH PREVIOUS WORKS

Ref	Tech (CMOS)	P_{LO} (dBm)	RF Freq. (GHz)	CG (dB)	OP_{1dB} (dBm)	P_{DC} (mW)	FoM (dB)
[3]	0.13-μm	3	18 – 28	0.7	-5.2	8	-11.3[b]
[4]	0.13-μm	-	25 – 27.5	1.3	-21.7	3.9	-16.1
[5]	0.13-μm	-	16.6 – 19.6	4[a]	4.2[a]	93[a]	-15.6[b]
[6]	90-nm	5	20 – 26	2	-12.8	11.1	-15.9
[7]	0.18-μm	10	15 – 50	-13	-8.0	-	-
This Work	0.13-μm	0[c]	23.4 – 29.2	-1.9	0.3	22.8[c]	-14.4

[a] Include pre-power amplifier
[b] Performance that does not include on-chip transformer
[c] External LO power (P_{LO}) of 0 dBm is increased to 4.7 dBm by the LO buffer that consumes 16.5 mW from a 1.5 V supply.

where P_{DC} represents the dc power consumption. As shown in Table I, the proposed up-conversion mixer exhibits the highest OP_{1dB} (0.3 dBm) and FoM (-14.4 dB), except for the mixers reported in [5] and [3], respectively. The mixer in [5] includes a pre-power amplifier, while the mixer in [3] does not include the on-chip transformer that requires for the single-ended output. The on-chip transformer causes insertion loss of 5–7 dB [6], [7].

IV. CONCLUSION

In this letter, a highly-linear 24 GHz ISM band up-conversion mixer is reported. Improvement of mixer linearity was achieved by adopting the proposed transconductance stage, which combines voltage feedback and adaptive biasing techniques. Implemented in a 0.13 μm CMOS, the proposed up-conversion mixer exhibited a CG of -1.9 dB and an OP_{1dB} of 0.3 dBm while dissipating 22.8 mW from a 1.5 V supply.

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