This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2499540, IEEE Transactions on Power Electronics

A 200V 98.16%-Efficiency Buck LED Driver Using Integrated Current Control to Improve Current Accuracy for Large Scale Single-String LED Backlighting Applications

Baek-Min Lim, Young-Hun Ko, Yeong-Shin Jang, Ok-Hwan Kwon, Sok-Kyun Han, and Sang-Gug Lee, *Member, IEEE*

***Abstract*—This paper presents an average current mode buck dimmable light-emitting diode (LED) driver for large scale single-string LED backlighting applications. The proposed integrated current control technique can provide exact current control signals by using an auto-zeroed integrator to enhance the accuracy of the average current of LEDs while driving a large number of LEDs. Adoption of discontinuous low-side current sensing leads to power loss reduction. Adoption of a fast-settling technique allows the LED driver to enter into the steady-state within 3 switching cycles after the dimming signal is triggered. Implemented in a 0.35-µm HV CMOS process, the proposed LED driver achieves 1.7% LED current error and 98.16% peak efficiency over an input voltage range of 110 to 200V while driving 30 to 50 LEDs.**

***Index Terms*— Buck LED driver, peak current control (PCC), hysteretic current control (HCC), pulse width modulation (PWM) dimming, discontinuous low-side current sensing.**

I. Introduction

SINCE the introduction of light emitting diodes (LEDs), the LED market has been growing on the basis of advantages such as longer lifetime, low power consumption, robustness, eco-friendly parts, smooth-dimming, and outstanding luminous efficacy [1]–[6]. Accordingly, cold cathode fluorescent lamps (CCFLs), the traditional backlight sources for liquid crystal displays (LCDs) have been gradually substituted with LEDs in flat panel display (FPD) systems [7]–[13]. Backlight based FPDs have been adopted in LCD TVs, monitors, and notebooks. The luminance of LEDs depends on the average current flowing through them, and as such it is essential to control the LED current precisely and efficiently for accurate luminance control and power efficiency. A DC-DC converter-based buck LED driver, which is an essential current regulating circuit in typical LED backlighting systems, as shown in Fig. 1, provides a regulated output current through LEDs regardless of their input and forward voltage variations [14]–[22]. In large scale FPDs,

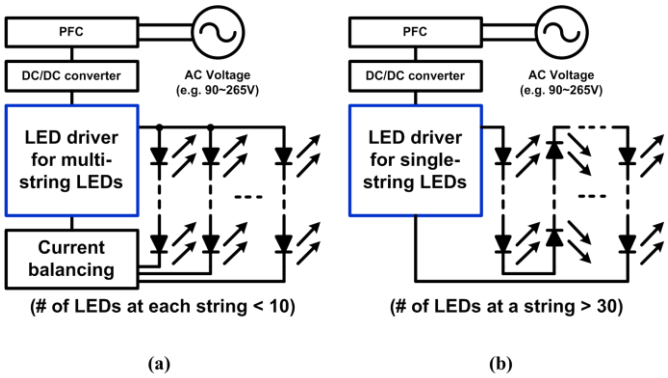

Fig. 1. Structure of typical LED backlighting systems for (a) multi- and (b) single-string LEDs.

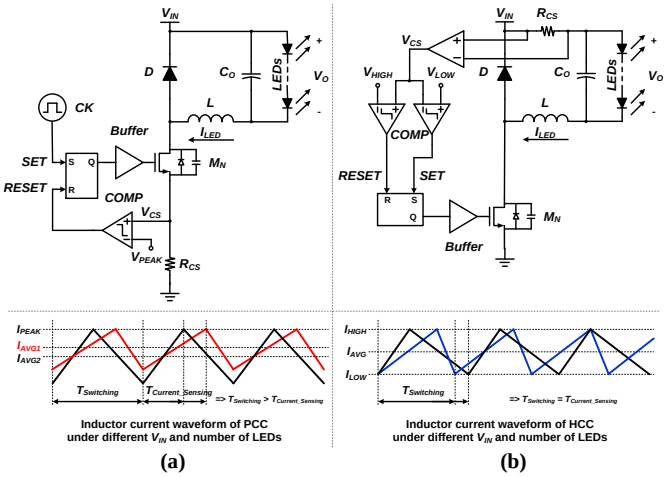

Fig. 2. Structures of traditional inverse buck LED drivers and inductor current waveforms.
(a) Peak current control. (b) Hysteretic current control.

This work is financially supported by the Ministry of Science, ICT & Future Planning and National Research Foundation of Korea (NRF) through the Human Resource Training Project for Regional Innovation.

B.-M. Lim, Y.-H. Ko, Y.-S. Jang, S.-K. Han, and S.-G. Lee are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-338, Korea (e-mail: lbmin1352@kaist.ac.kr).

O.-H Kwon was with the Department of Electrical Engineering, Kyungpook National University, Daegu 702-701, Korea. He is now with Silicon Works Co., Ltd., Daejeon 305-510, Korea (e-mail: kwonoh@siliconworks.co.kr).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2499540, IEEE Transactions on Power Electronics

the LED backlighting systems need a lot of LEDs to provide sufficient brightness. Fig. 1(a) shows the system topology for driving multi-string LEDs which is the general solution for large scale FPDs. The LED driver for multi-string LEDs requires additional current balancing circuits to control each LED array for uniform brightness resulting in increase of the bill of the material (BOM) cost [23]–[26]. Recently, the system topology for driving single-string LEDs (Fig. 1(b)) has been considered to be the alternative solution. The LED driver for single-string LEDs does not need current balancing so that can reduce the BOM cost at the price of increase of the number of LEDs at a string. The LED driver should maintain high current accuracy by precisely regulating the average current flowing through LEDs and realize high power efficiency to lower the power consumption. In general, however, there is a tradeoff between current accuracy and power efficiency in conventional LED driver structures.

There are two traditional LED driver structures, peak current control (PCC) and hysteretic current control (HCC). Fig. 2 shows the fundamental structures of these two driver structures in an inverse buck topology. The PCC scheme (Fig. 2(a)) has a current sensing resistor R_{CS} connected between the source node of the power NMOSFET M_N and ground; this is known as a discontinuous low-side current sensing topology. While M_N turns on, the driver can sense the LED current value I_{LED} by monitoring V_{CS} assuming I_{LED} is equal to the current through the inductor under steady-state condition. The driver generates a switch-off signal *RESET* by comparing V_{CS} with a peak reference voltage V_{PEAK}. Since I_{LED} flows through R_{CS} only during the on-time period, power dissipation can be reduced. However, I_{LED} cannot be sensed during the switch-off period. The average LED current value I_{AVG} consequently varies under different input and forward voltages of LED, which leads to LED current accuracy degradation. To increase the current accuracy, HCC (Fig. 2(b)) is proposed, where R_{CS} is connected in series with LEDs for continuous I_{LED} sensing. From the current sensing amp, the driver can monitor V_{CS} and regulate the peak and valley values of I_{LED} by using two reference voltages, V_{LOW} and V_{HIGH}. Consequently, the current accuracy of HCC becomes much better than that of PCC. Due to continuous high-side current sensing, however, at every switching period, large LED current flows into R_{CS} leading to high power dissipation [27]. Recent studies have suggested adaptive off-time control to provide an exact switch-on signal to enhance the current accuracy based on a PCC structure [28]–[29]. This can improve both accuracy and efficiency while driving a small number of series-connected LEDs (LED output voltage < 40V) under the assumption that the LED current slope does not change. In reality, however, the slope varies during each switching period. When the number of series-connected LEDs is large (LED output voltage ≈ 170V [15]), the slope variation becomes significant due to the large variations in the total LED forward voltages.

To resolve the issues noted above, this paper proposes a new current control technique. Based on a PCC discontinuous low-side current sensing topology to reduce power dissipation, the current control technique using an auto-zeroed integrator is adopted to generate a switch-off signal with exact timing for high average current accuracy. This paper is organized as follows. Section II analyzes the accuracy limit in prior arts and introduces the operational principle of the proposed control technique that overcomes the limit. The control scheme and the system implementation details are provided in Section III. The experimental results are presented in Section IV. Finally, conclusions are given in Section V.

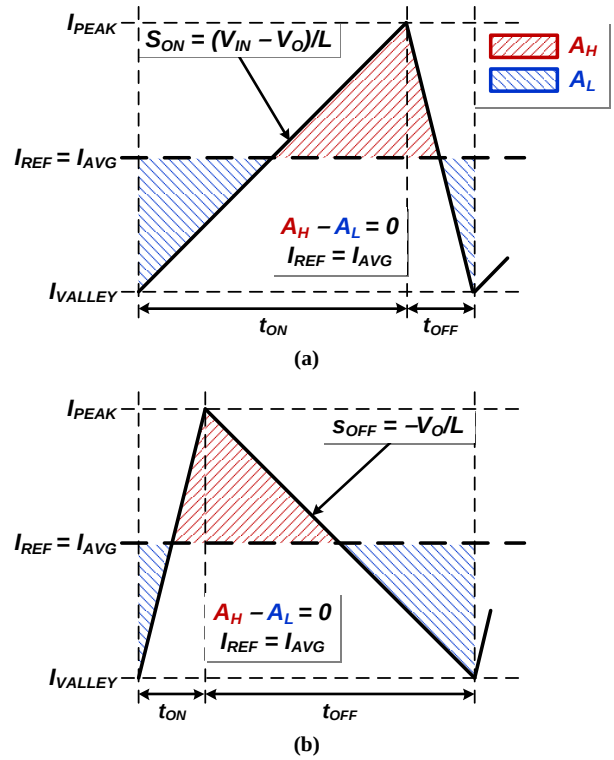

Fig. 3. Inductor current waveform of PCC and HCC that the average current becomes equal to the reference current for an ideal case (V_O is constant). (a) on-time > off-time. (b) on-time < off-time.

II. Operation Principle

A. Current Accuracy Limit Analysis

PCC and HCC have been widely used as the main current control schemes in recent average current mode controlled LED driver designs. In particular, PCC is a widely used topology due to its high power efficiency, intermediate current accuracy, and simple operation. The average LED current $I_{AVG,\,PCC}$ in PCC is given by

$$I_{AVG,PCC} = I_{PEAK} - \frac{\Delta I}{2} = I_{PEAK} - \frac{V_O}{2L} t_{OFF} = I_{PEAK} - \frac{V_O T_S}{2L}\left(1 - \frac{V_O}{V_{IN}}\right) \quad (1)$$

where I_{PEAK} and ΔI are the peak and ripple currents of the LED, respectively, V_{IN} is the input voltage of the LED, V_O is the output voltage of LED, t_{OFF} is the switch-off period, and T_S is the switching period. Since I_{PEAK} and L do not change, $I_{AVG,PCC}$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2499540, IEEE Transactions on Power Electronics

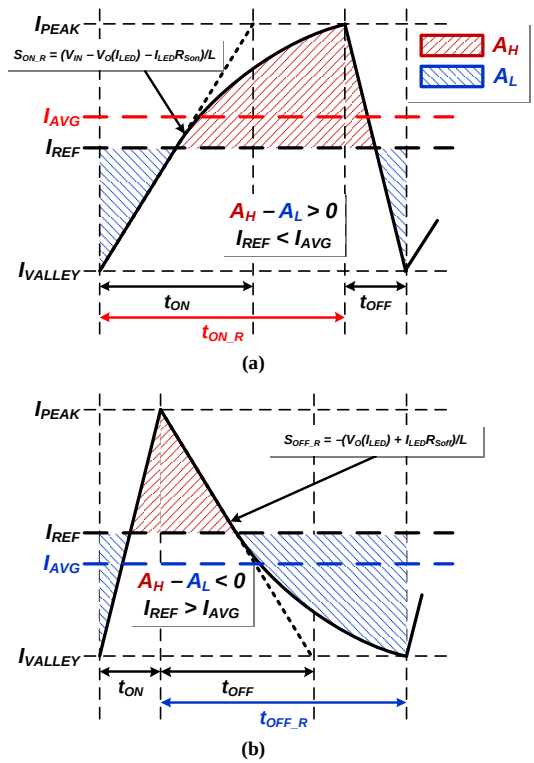

Fig. 4. Inductor current waveform of PCC and HCC when LED current error occurs for a real case (V_O is the function of I_{LED}).
(a) on-time > off-time. (b) on-time < off-time.

depends on V_O and V_{IN} [30]. Due to the variation in V_O and V_{IN}, PCC cannot ensure high current accuracy under process and temperature variations and different input voltage conditions. The accuracy limit in PCC, however, can be reduced by introducing an adaptive off-time technique [28]–[29] or replacing PCC with HCC, thereby sacrificing power efficiency.

As mentioned above, HCC can solve the accuracy limitation problem. The average LED current $I_{AVG,HCC}$ in HCC is given by

$$I_{AVG,HCC} = \frac{I_{HIGH} + I_{LOW}}{2} \tag{2}$$

where I_{HIGH} and I_{LOW} are the upper and lower reference current, respectively. In contrast with PCC, HCC does not appear to show any environment dependent terms.

In reality, HCC and even PCC have another limiting factor in current accuracy. Normally, V_O is considered as a constant value during the switching period since the V-I curve of LEDs is similar to that of a regular diode [30]. However, the actual output voltage of the LED varies during each switching period, which leads to LED current error. In this section, the limiting factor in current accuracy due to the variation of V_O is analyzed by comparing the ideal case where V_O is constant with the real case where V_O varies during operation.

First, assuming that V_O is constant, the steady-state inductor current waveform of PCC and HCC where the average current I_{AVG} becomes equal to the reference current I_{REF} is shown in Fig. 3. In Fig. 3, the relationship between the LED current error and the shaded area, A_H and A_L, is given by

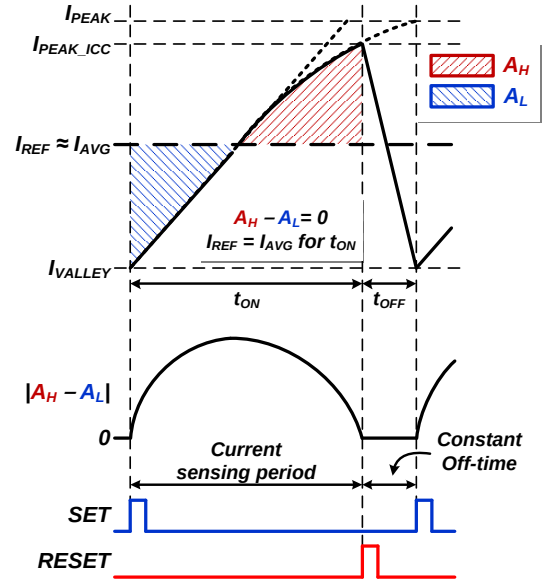

Fig. 5. Concept of the proposed integrated current control.

$$\begin{aligned} error &= I_{AVG} - I_{REF} \\ &= \frac{1}{T_S} \cdot \int_0^{T_S} I_{LED}(t)\, dt - I_{REF} \quad \because (T_S = t_{ON} + t_{OFF}) \\ &= \frac{1}{T_S} \cdot \int_0^{T_S} \left[I_{LED}(t) - I_{REF} \right] dt \\ &= \frac{A_H - A_L}{T_S} \end{aligned} \tag{3}$$

where t_{ON} and t_{OFF} are the switch-on and switch-off period, respectively, and A_H and A_L are the red-colored (one upper triangle) and blue-colored (two lower triangles) area in Fig. 3, respectively. According to (3), it is possible to obtain the LED current error by integrating the difference between I_{LED} and I_{REF}. In this case, since A_H and A_L are identical there is no current error. The slope of the LED current during on- and off-time are given by

$$s_{ON} = \frac{V_{IN} - V_O}{L} \tag{4}$$

$$s_{OFF} = -\frac{V_O}{L}. \tag{5}$$

It is assumed that the forward bias voltage of the freewheeling diode D, the series resistance of the LEDs and inductor L, and the on-resistance of M_N are negligible in Fig. 2. Because V_O and L are fixed and V_{IN} is chosen to satisfy $I_{REF} = I_{AVG}$, s_{ON} and s_{OFF} may appear not to change during the switching period.

However, the variation of the output voltage of the LED during each switching period affects the current slopes in the case where a large number of series-connected LEDs are driven. The real equations for the slope of the LED current during on-

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2499540, IEEE Transactions on Power Electronics

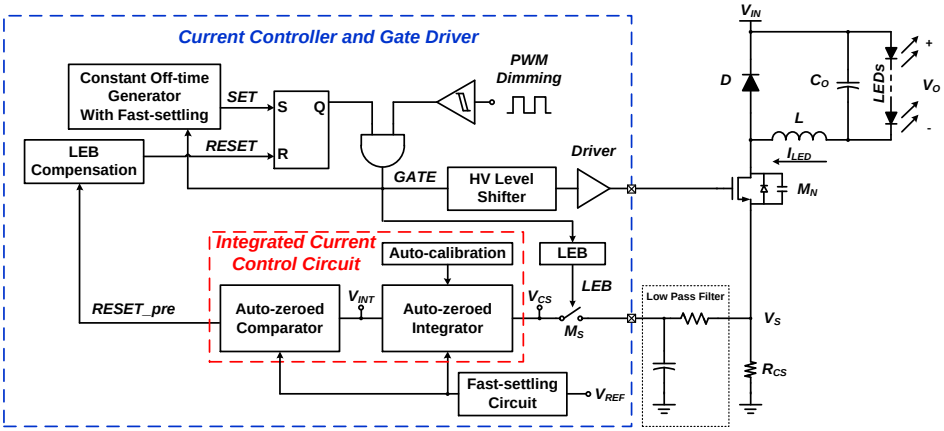

Fig. 6. Structure of the proposed integrated current controlled Buck LED driver.

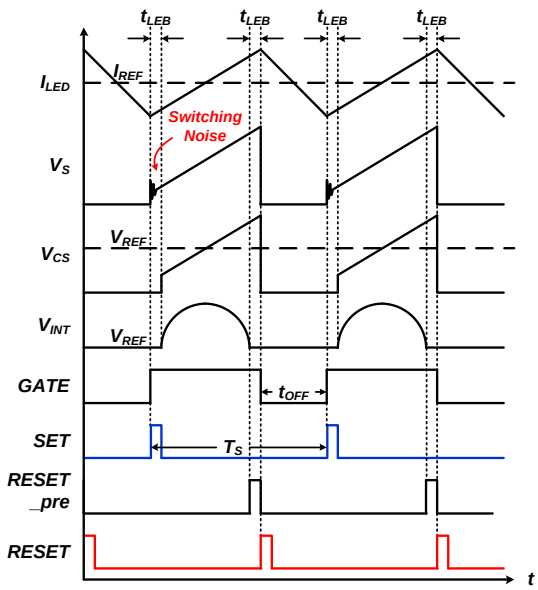

Fig. 7. Timing diagram of the LED current and corresponding control signals in the proposed LED driver.

and off-time are given by

$$s_{ON\_R} = \frac{V_{IN} - V_O\left(I_{LED}\right) - I_{LED} \cdot R_{Son}}{L} \tag{6}$$

$$s_{OFF\_R} = -\frac{V_O\left(I_{LED}\right) + I_{LED} \cdot R_{Soff}}{L} \tag{7}$$

where $V_O(I_{LED})$ represents V_O, which is a function of I_{LED}, and R_{Son} and R_{Soff} are the total series resistances on the LED current path during on- and off-time, respectively. Because $V_O(I_{LED})$ increases as a logarithmic function of I_{LED}, s_{ON_R} and s_{OFF_R} decrease as I_{LED} rises. For a small number of series -connected LEDs, in general, the slope variation can be neglected. In the case of a large number of LEDs, the variation of V_O during switching transient becomes large since $V_O \approx nV_F$, where V_F is the forward voltage of one LED. Hence, the slope variation can be significant, which introduces another source of LED current error. The steady-state inductor current waveform for the real case current slope is shown in Fig. 4. If the on-time is longer than the off-time (Fig. 4 (a)), s_{ON_R} continuously decreases as I_{LED} rises. Although the values of I_{PEAK} and I_{VALLEY} can be set to make I_{AVG} equal to I_{REF}, the difference of integrated area $A_H - A_L$ is still larger than zero because the on-time of the real case t_{ON_R} is longer than that of the ideal case t_{ON}, as shown in Fig. 4 (a). Consequently, LED current error occurs. Similarly, when the on-time is shorter than the off-time (Fig. 4 (b)), s_{OFF_R} continuously increases as I_{LED} falls. Due to the variation of s_{OFF_R}, the off-time of the real case t_{OFF_R} becomes longer than that of the ideal case t_{OFF}, as shown in Fig. 4 (b). Consequently, $A_H - A_L$ becomes smaller than zero, leading to current error. In the analysis, it is assumed that the increase in the on- and off-time can be neglected if the LED current slopes are sufficiently steep.

B. *Principle of Proposed Integrated Current Control*

To solve the LED current accuracy limit, this paper proposes an integrated current control technique. According to (3), the current error can be predicted by integrating the difference between I_{LED} and I_{REF}. In summary, if the integrated value $A_H - A_L$ is larger than zero, I_{AVG} becomes larger than I_{REF}. Similarly, if $A_H - A_L$ is smaller than zero, I_{AVG} becomes smaller than I_{REF}. This implies that the integrated value should be zero to make I_{AVG} equal to I_{REF} under the current slope variation. The integrated value contains all information for non-idealities including the input and forward voltage variations of the LED and even the slope variations during the switching period. Therefore, using the integrated current information can be a solution for high current accuracy. Fig. 5 shows the concept of the proposed integrated current control technique based on discontinuous low-side current sensing considering efficiency. In Fig. 5, instead of using the peak and valley currents as a reference or a similar concept to generate a switch-off signal, a *RESET* signal is generated when the integrated value $A_H - A_L$ reaches zero. Therefore, the average current becomes equal to the desired reference current even if the current slope varies. To generate a *SET* signal, the constant off-time control technique is applied [18]. Although the LED current is sensed only during t_{ON}, the current error induced by the current slope variation during the off-time can be neglected because the off-time is fixed and the output voltage of the LED is large enough that the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2499540, IEEE Transactions on Power Electronics

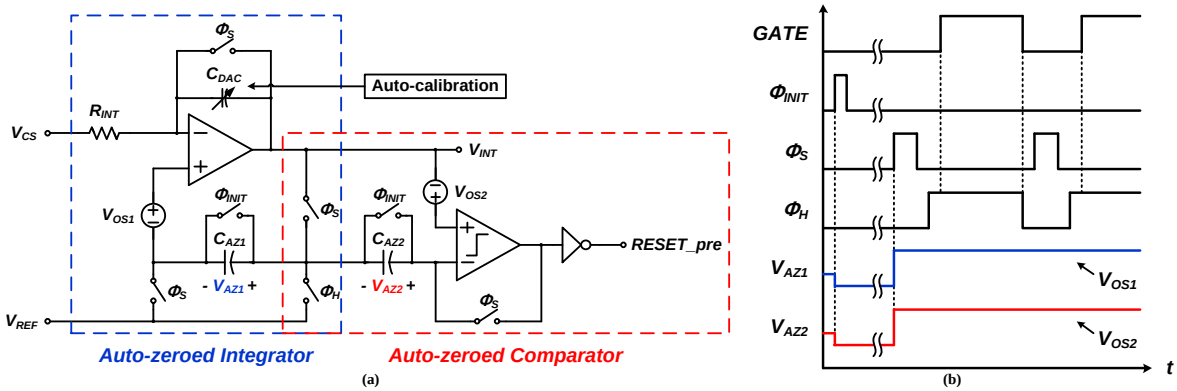

Fig. 8. (a) Schematic and (b) timing diagram of the auto-zeroed integrator and comparator.

LED current slope during t_{OFF} is sufficiently steep.

III. Implementations

The structure of the proposed Buck LED driver using integrated current control technique is shown in Fig. 6. In Fig. 6, the typical inverse Buck topology is applied for the off-chip current regulator, which includes an LED string, a freewheeling diode D, an inductor L, an N-type power MOSFET M_N, a low-pass filter, and a current sensing resistor R_{CS}. The on-chip part consists of the proposed current controller and the gate driver circuits that provide a driving signal to M_N. To handle large input voltage levels of over 200 V, a 400 V high voltage power MOSFET is adopted for M_N. The current controller contains the current control loop and the PWM dimming block. The control loop incorporates the current sampling switch M_S, the proposed integrated current control circuit, the leading edge blanking (LEB) compensation block, and the constant off-time generator. The proposed control circuit generates a switch-off signal with exact timing, and the constant off-time generator generates a switch-on signal. The gate driver circuits consist of a high-voltage level shifter and a gate driver to drive M_N.

During the time that M_N is on, the LED current flows through R_{CS} and is converted into the current sensing signal V_S. V_S is then filtered by the RC low-pass filter to eliminate a reverse recovery current. Due to the reverse recovery effect of the freewheeling diode, a high value of peak-reverse recovery current can be induced when the MOSFET turns on [31]–[32]. If this peak high-frequency spike current noise is sent directly to the internal current regulating circuits, it may cause additional current error. Therefore, LEB are applied to prevent the error from the noise. When M_N turns on, the LEB block turns on M_S after the time delay of t_{LEB} and starts current sensing, as shown in Fig. 7. V_{CS} represents the sensed signal after t_{LEB} and is the input signal of the proposed integrated current control circuit shown in Fig. 7 that consists of an integrator, a comparator, and the auto-calibration block. The integrator and comparator are designed to be auto-zeroed to cancel their offsets. The integrator integrates the difference between V_{CS} and the target average voltage V_{REF}, and the comparator compares the output of the integrator V_{INT} with V_{REF} again. V_{INT} continues to increase until $V_{CS} = V_{REF}$, and then begins to decrease. When V_{INT} reaches V_{REF}, *RESET_pre* becomes high. Because the integrator produces *RESET_pre* without sensing the current during t_{LEB}, the LEB compensation block adds the same time delay t_{LEB} to *RESET_pre* for compensation of the information loss (inductor current during t_{LEB}), which prevents accuracy degradation. Then, the switch-off signal *RESET* is generated after t_{LEB} from the rising edge of *RESET_pre*. Consequently, the difference of the integrated current value $A_H - A_L$ becomes zero. As a result, the average current during the switch-on period is equal to the target average current I_{REF}. During the switch-off period, the constant off-time generator counts the time after *RESET* becomes high and generates the switch-on signal *SET* at t_{OFF}. Once *SET* is generated, *GATE* becomes high and M_N turns on by the high-voltage level shifter and the gate driver. Within a few cycles, the driver finds the exact on-time duty, leading to the condition of $I_{AVG} = I_{REF}$.

A. Auto-zeroed Integrator and Comparator

The schematic and timing diagram of the auto-zeroed integrator and comparator in the proposed integrated current control circuit is shown in Fig. 8. To minimize the LED current error factors inside the circuits, the integrator and comparator offsets must be cancelled. Hence, the auto-zero technique is adopted as an offset cancellation technique because its sample and hold signals can simply be generated by the existing control signals. In Fig. 8, before the operation begins, the auto-zeroing capacitors C_{AZ1} and C_{AZ2} are initialized by Φ_{INIT}. When *GATE* is low, the non-overlapped sampling signal Φ_S switches to high, which corresponds to the sampling phase. During this phase, the integrator and comparator become unit gain buffers and the integrator and comparator offset voltages V_{OS1} and V_{OS2} are stored in C_{AZ1} and C_{AZ2}, respectively. After Φ_S switches to low and the sampling phase is over, the non-overlapped holding signal Φ_H switches to high, leading to the holding phase. During the holding phase, the integrator and comparator offsets are cancelled by the stored offsets. Consequently, there is no additional current error induced by the proposed control circuit.

B. Auto-calibration Block

A block diagram of the auto-calibration block in the proposed integrated current control circuit is shown in Fig. 9. The auto-zeroed integrator consists of an offset-cancelled opamp, a resistor R_{INT}, and a 2-bit capacitor DAC. Because V_{INT} has a

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2499540, IEEE Transactions on Power Electronics

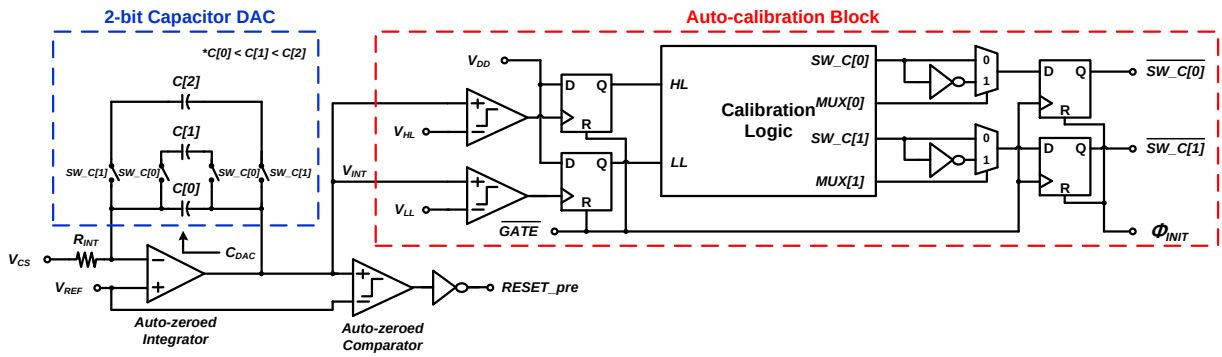

Fig. 9. Block diagram of the auto-calibration block in the proposed integrated current control circuit.

Input Data				Output Data		Note
HL	LL	SW_C[0]	SW_C[1]	MUX[0]	MUX[1]	
0	0	0	0	0	0	Invalid Range
0	0	0	1	0	1	Proceeding toward Valid Range
0	0	1	0	1	1	
0	0	1	1	0	1	
0	1	X	X	0	0	Valid Range
1	0	X	X	0	0	Forbidden
1	1	0	0	0	1	Proceeding toward Valid Range
1	1	0	1	1	1	
1	1	1	0	0	1	
1	1	1	1	0	0	Invalid Range

Fig. 10. Truth table of the calibration logic.

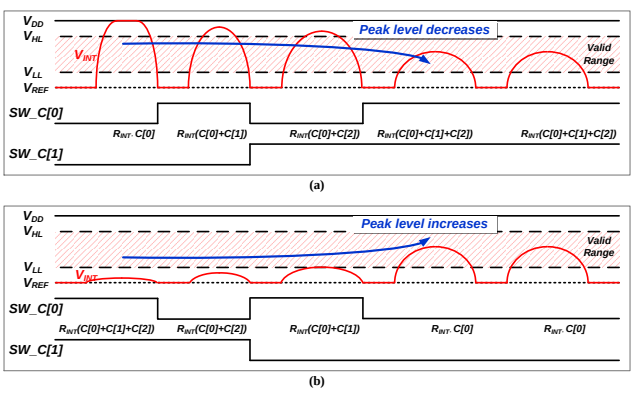

Fig. 11. Operation examples of the auto-calibration block.
(a) total DAC cap increases. (b) total DAC cap decreases.

voltage headroom of V_{DD}, V_{INT} may be clamped by V_{DD}. If so, it will result in loss of the information of the integrated current. V_{INT} and its peak level are given by

$$V_{INT}(t) = V_{REF} + \frac{\int \left(V_{REF} - V_{CS}(t)\right) dt}{R_{INT} C_{DAC}}$$
$$V_{INT}\big|_{PEAK} \approx V_{INT}\left(\frac{t_{ON}}{2}\right) = V_{REF} + \frac{\int_0^{\frac{t_{ON}}{2}} \left(V_{REF} - V_{CS}(t)\right) dt}{R_{INT} C_{DAC}} \quad (8)$$

where C_{DAC} is the total capacitance of the 2-bit capacitor DAC and the term with integration represents the amount of integrated current. According to (8), the peak level of V_{INT} depends on V_{REF}, $R_{INT}C_{DAC}$, and the integrated current. Because V_{REF} and the amount of integrated current are variables that depend on operation conditions, the peak level of V_{INT} varies and can even exceed the V_{DD} limit. To prevent V_{INT} from exceeding V_{DD}, C_{DAC} is controlled by the auto-calibration block such that the peak level of V_{INT} will remain in the valid range without requiring trimming. The valid range is from the lower-limit voltage of V_{LL} to the higher-limit voltage of V_{HL}. The auto-calibration block monitors V_{INT} and *SW_C*[0:1], which is the switching bit of the 2-bit capacitor DAC. *SW_C*[0:1] is initialized by Φ_{INIT}. When *GATE* is high, V_{INT} continuously increases until it reaches its peak level. The two comparators with D flip-flops then determine whether V_{INT} has reached its peak level and convert it into a combination of the digital codes of *HL* and *LL*. The main logic of the auto-calibration block gathers the input data of *HL* and *LL* and controls the two 1-bit MUXs. The truth table of the calibration logic in the auto-calibration block is shown in Fig. 10. For example, when *HL* = 0 and *LL* = 1, the peak level of V_{INT} is in the valid range, and thus the MUX control bit *MUX*[0:1] = 00 and *SW_C*[0:1] maintains the previous bit. When *HL* = *LL* = 1 or *HL* = *LL* = 0, the peak level of V_{INT} is out of the valid range, and hence *MUX*[0:1] ≠ 00 and *SW_C*[0:1] bit continues changing until the peak level of V_{INT} remains in the valid range. Operational examples of the auto-calibration block are shown in Fig. 11. In Fig. 11, when the peak level of V_{INT} is higher than V_{HL}, *SW_C*[0:1] bit increases in each switching period. Consequently, $R_{INT}C_{DAC}$ increases and the peak level of V_{INT} decreases. Similarly, when the peak level of V_{INT} is lower than V_{LL}, *SW_C*[0:1] bit decreases in each switching period. Finally, $R_{INT}C_{DAC}$ decreases and the peak level of V_{INT} increases. The case of *HL* = 1 and *LL* = 0 cannot happen under normal operation.

C. LEB Compensation and Fast Settling

The basic function of the LEB and LEB compensation blocks is to delay the *GATE* and *RESET_pre* signals by adding the same time delay of t_{LEB} and to generate *LEB* and *RESET* signals from *GATE* and *RESET_pre*, respectively. The LEB and LEB compensation blocks with their timing diagram are schematically illustrated in Fig. 12. The structures of the LEB and LEB compensation blocks are identical and consist of a

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2499540, IEEE Transactions on Power Electronics

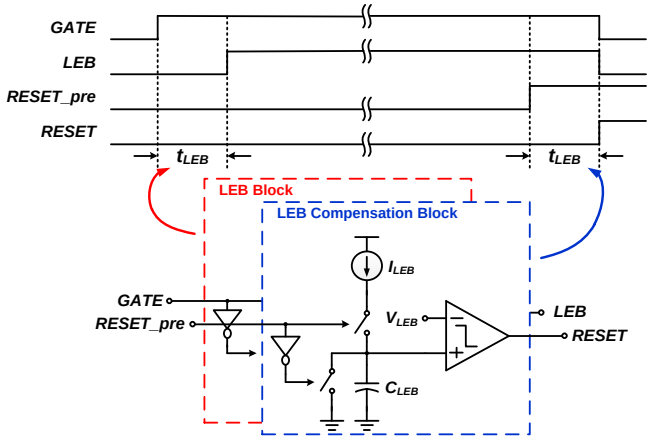

Fig. 12. Block and timing diagram of LEB and LEB compensation block.

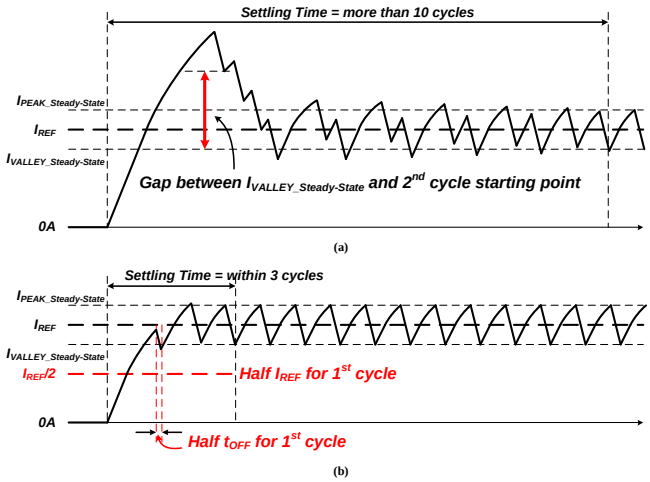

Fig. 13. Inductor current waveform during settling operation.

simple delay adder that includes a current source, two switches, an inverter, a comparator, and a capacitor. In Fig. 12, when the input signal of the LEB or LEB compensation block switches to high, the current source charges the capacitor C_{LEB} with I_{LEB}. The charged voltage then increases and is compared with V_{LEB} by the comparator. After t_{LEB}, the charged voltage level exceeds V_{LEB} and the output signal becomes high. t_{LEB} is then given by

$$t_{LEB} = C_{LEB} \frac{V_{LEB}}{I_{LEB}}. \tag{9}$$

Although the proposed LED driver can achieve high current accuracy, the settling time issue must still be resolved. Long settling time may introduce LED current error if the PWM duty is sufficiently low or the PWM frequency is sufficiently high. Therefore, the PWM operating range may be restricted for high current accuracy. To circumvent the limitation of the PWM operating range, the settling time should be sufficiently short. Because the proposed driver operates in a continuous conduction mode (CCM), the value of the integrated current before the inductor current reaches I_{REF} during the 1st cycle is larger than that of the integrated current before the inductor current reaches I_{REF} during each switching period in the steady-state, resulting in a large amount of current ripple during the 1st cycle, as shown in Fig. 13(a). Hence, the value of the inductor current at the starting point of the 2nd cycle deviates from the steady-state valley current $I_{VALLEY\_Steady\text{-}State}$, and it takes more than 10 cycles to enter into the steady-state operation. Fig. 13(b) shows the waveform of the inductor current that adopts a fast-settling technique. The technique is to make the 1st cycle current reference and off-time half so that the value of the inductor current at the starting point of the 2nd cycle becomes $I_{VALLEY\_Steady\text{-}State}$. Consequently, the gap between $I_{VALLEY\_Steady\text{-}State}$ and 2nd cycle starting point becomes sufficiently small and the inductor current settles within 3 cycles.

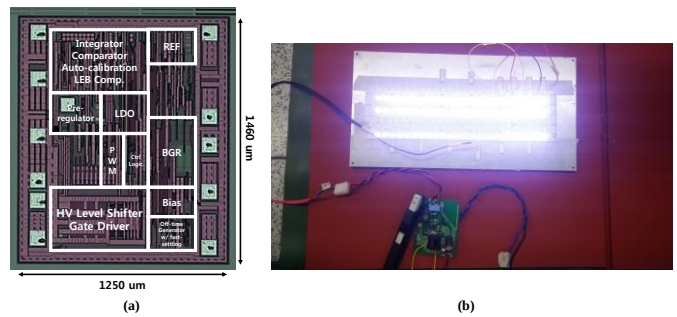

Fig. 14. (a) Micrograph and (b) test setting of the proposed LED driver.

TABLE I
DESIGN SPECIFICATION OF THE PROPOSED LED DRIVER

Process	0.35-um HV CMOS
Chip area	1250um*1460um
DC input voltage	110V – 200V
Supply voltage	5V
Off time	1us
LEB time	210ns
Max. switching freq.	500kHz
Sensing resistor	1Ω (1% variation)
Inductor	1mH
Output capacitor	0.15uF
Power MOSFET	N-channel, 600V, 1.2A (STD5NK60Z)
LED forward voltage	3.1V @500mA

IV. EXPERIMENTAL RESULTS

The proposed LED driver is implemented in a 0.35-μm high voltage CMOS technology. The chip micrograph and its test setting are shown in Fig. 14. The chip area including the bonding pad is about 1250 μm x 1460 μm. The LED driver can support input voltage V_{IN} of up to 600 V, which is the maximum rating of the high voltage power MOSFET, and the maximum switching frequency is 500 kHz. Because the operating conditions can vary depending on the application set-up, this

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2499540, IEEE Transactions on Power Electronics

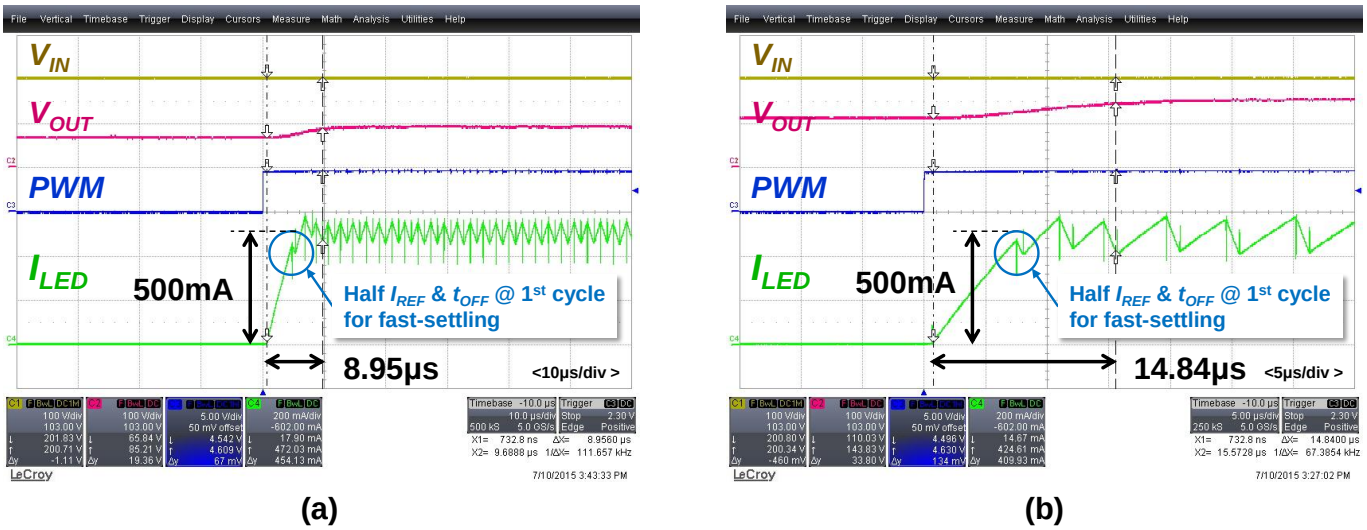

Fig. 15. Measured waveforms of the proposed LED driver during PWM start-up period. (a) 30 LEDs. (b) 50 LEDs.

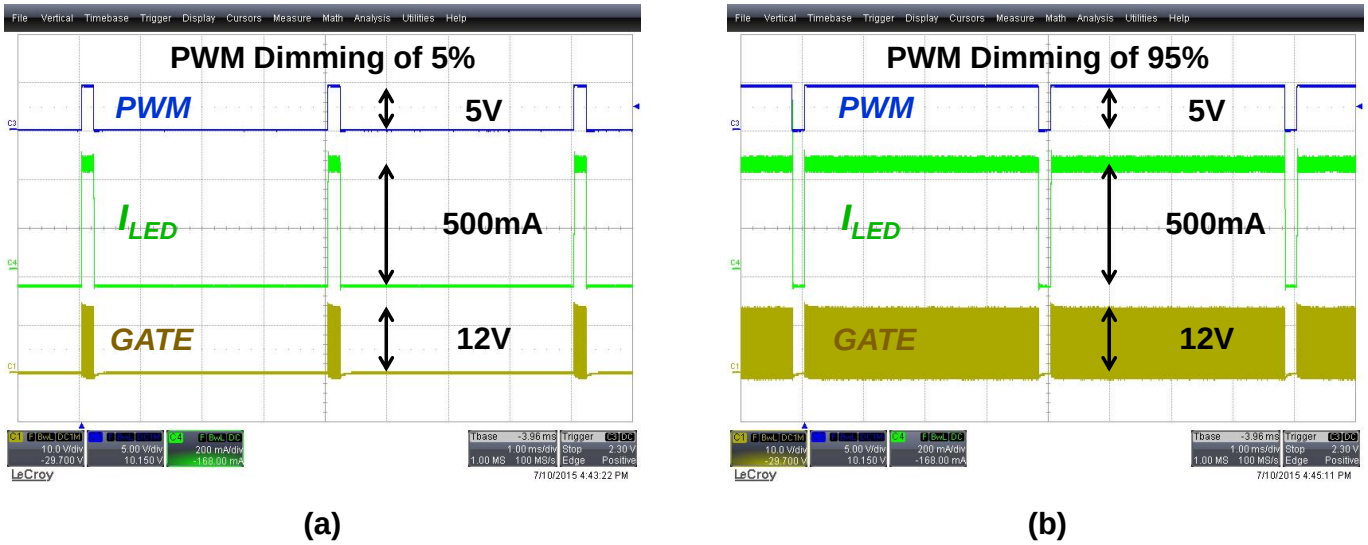

Fig. 16. Measured waveforms of the proposed LED driver under PWM dimming control. (a) duty = 5%. (b) duty = 95%.

paper presents specific measured results at I_{REF} = 500 mA with t_{OFF} = 1 μs and L = 1 mH, and C_O = 0.15 uF while driving 30 to 50 LEDs. The inductor and the capacitor values are chosen to achieve the ripple factor of the LED current being below 30% and the output ripple voltage being less than 4.5V, respectively. To meet the above operating conditions, the V_{IN} range is from 110 to 200 V. The detailed design specification of the proposed LED driver is in Table I.

The measured waveforms of the proposed LED driver during the PWM start-up period are shown in Fig. 15. In Fig. 15, the fast-settling technique is applied so that the inductor current settles in 3 cycles. After the *PWM* signal switches to high, the inductor current increases until it reaches I_{REF} in its 1st cycle and then decreases within a half period of t_{OFF}. Consequently, the inductor current enters into the steady-state operation in its 3rd cycle, similar to the waveform shown in Fig. 13(b). The settling times are 8.95 and 14.84 μs for 30 LEDs and 50 LEDs when V_{IN} = 200 V, respectively. The settling times are short enough and only 0.22 to 0.37% of one PWM period. The measured waveforms of the proposed LED driver under PWM dimming control are shown in Fig. 16. The test frequency of PWM dimming is 250 Hz and the duty ratios are 5 and 95%. The measured waveforms of the line regulation characteristic of the proposed LED driver are shown in Fig. 17. When V_{IN} is switched from 110 to 200 V and vice versa over one PWM cycle, the on-time slope changes smoothly. Because the off-time is generated by the constant off-time generator, t_{OFF} remains constant even if V_{IN} changes. On the other hand, according to (6), the LED current slope during the on-time depends on V_{IN} and hence varies when V_{IN} changes, and the corresponding on-time also changes. Figure 17 shows that the regulated currents does not change and the ripple factor of the LED current maintains within 20% even though the slope and on-time change. Measured steady-state operation of the proposed LED driver under different number of LEDs is shown in Fig. 18. When V_{IN} = 160 V, the output voltage variation ΔV_O increases

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2499540, IEEE Transactions on Power Electronics

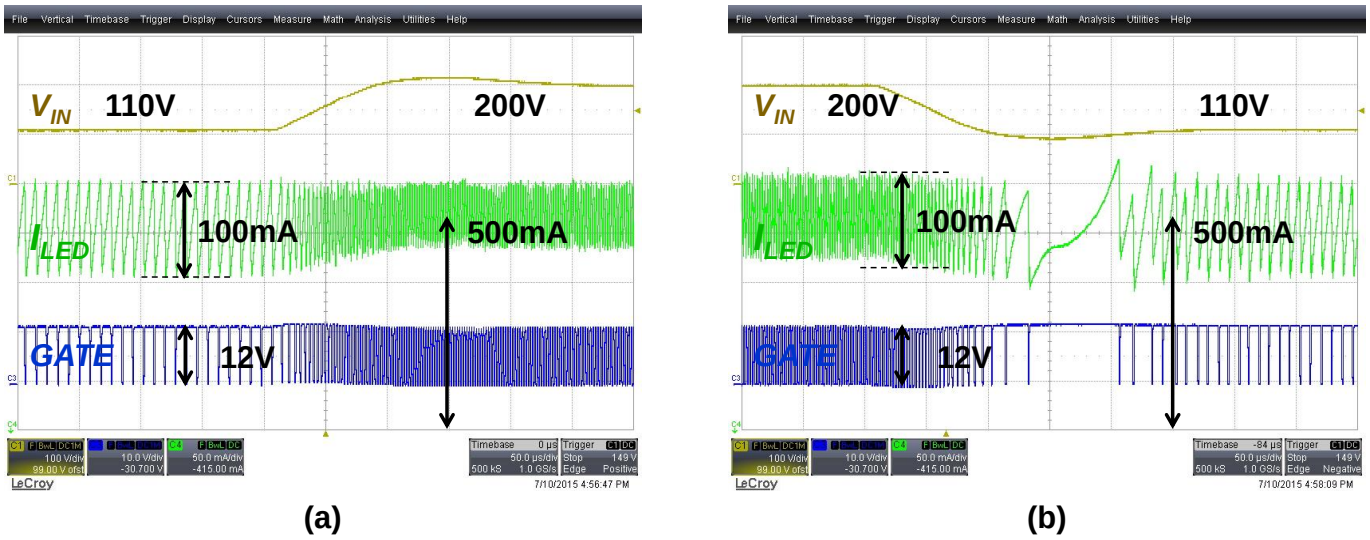

Fig. 17. Measured waveforms of V_{IN} line regulation in the proposed LED driver. (a) 110 V => 200 V. (b) 200 V => 110 V.

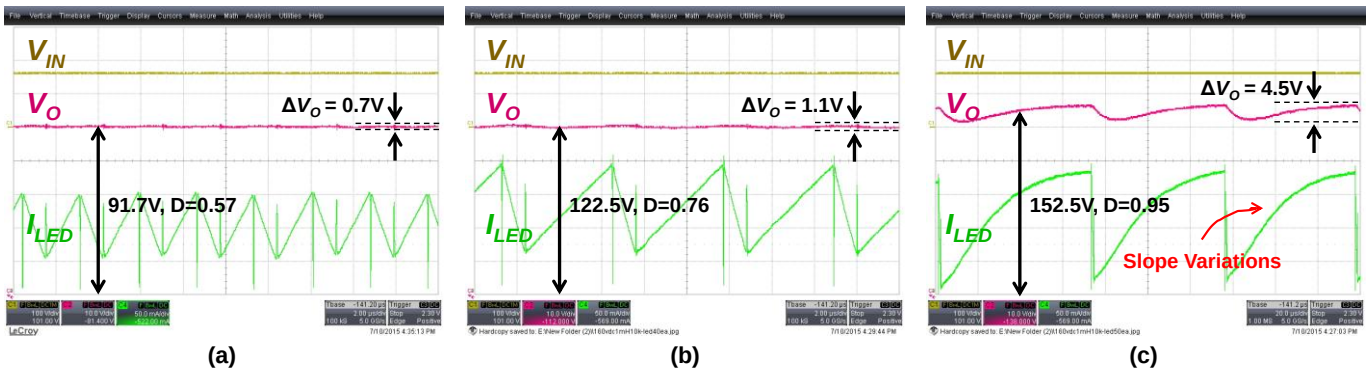

Fig. 18. Measured steady-state operation of the proposed LED driver when V_{IN} = 160V while driving (a) 30 LEDs, (b) 40 LEDs, and (c) 50 LEDs.

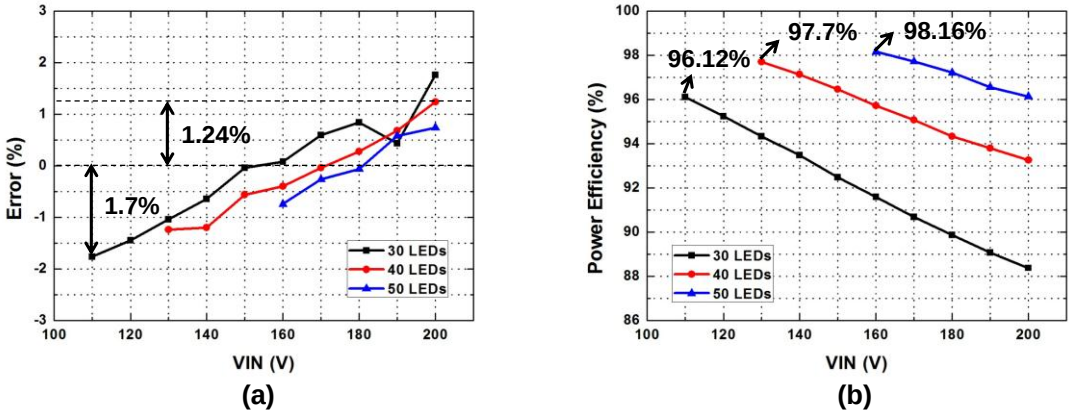

Fig. 19. Measured (a) LED current error and (b) power efficiency under different input voltages and number of LEDs in the proposed LED driver.

as the number of LEDs increases. As a result, large slope variations in I_{LED} while driving 50 LEDs can be observed in Fig. 18(c) and the LED current behavior is the same as the LED current characteristic shown in Fig. 5. On the contrary, the slope variations in I_{LED} during while driving 30 LEDs are negligible because the current slopes of I_{LED} are sufficiently steep, as shown in Fig. 18(a). In spite of good line regulation and steady-state operation for various number of LEDs, switching frequency variation under different input and output voltages is inevitable due to the constant off-time operation.

The measured LED current error and power efficiency versus input voltages in the proposed LED driver while driving 30, 40, and 50 LEDs are plotted in Fig. 19. The worst-case current error is 1.7% for 30 LEDs. Even under large slope variations of I_{LED},

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2499540, IEEE Transactions on Power Electronics

TABLE II
PERFORMANCE SUMMARY OF THE PROPOSED LED DRIVER IN COMPARISON WITH PRIOR WORKS

	TCAS I 2010 [28]	**JSSC 2014 [29]**	**JSSC 2015 [33]**	**BM0152HV 2014 [34]**	**This work**
Process	UMC 0.35-um HV CMOS	AMS 0.35-um 50V CMOS	0.35-um 50V CMOS	N. A.	**0.35-um HV CMOS**
Input Voltage (V)	8 – 40	10 – 40	5 – 45	7 – 60	**110 – 200**
Topology (# of Power MOSFETs)	Asynchronous Inverse Buck (2)	Synchronous Inverse Buck (2)	Synchronous Buck (2)	Asynchronous Inverse Buck (1)	**Asynchronous Inverse Buck (1)**
Control Scheme	Adaptive Off-time	Adaptive Timing Difference Compensation	Glitch-Tolerant Synchronous Current Control	Hysteretic Current Control	**Integrated Current Control**
Typ. Average Current (mA)	720	345	700	Up to 1000	**500**
Current Error (%) (# of LEDs)	±2.01 (1 – 8)	±2.8 (2 – 10)	±3.3 (1 – 12)	5 (~30 for 1W LEDs)	**±1.7 (30 – 50)**
Peak Efficiency (%)	94.3	92.5	97.2	97	**98.16**
Switching Frequency (kHz)	~188	≤ 1000	≤ 4000	≤ 1000	**≤ 500**
PWM Dimming Frequency (Hz) (Duty Ratio)	500	10k (0.2 – 1)	20k (0.1 – 1)	100 – 20k	**250 (0.05 – 1)**
*Settling Time (us)	120 (8 cycles)	8.5 (5 cycles)	3.2 (1 cycle)	N. A.	**14.84 (3 cycles)**
Inductor (uH)	33	10 – 39	8.2 – 39	100	**1000**

as shown in Fig. 18, the LED current error of the proposed driver does not exceed ±1.7%. The power efficiency increases continuously as V_{IN} approaches the output voltage of the LED because the wasted power is reduced. The final peak efficiency of the proposed driver is 98.16% under the given test conditions.

Table II summarizes the performance of the proposed driver in comparison with prior works. Compare to recently reported works [28]–[29] and [33]–[34], the proposed LED driver that adopts the integrated current control scheme requires larger inductor value to meet the ripple factor requirement due to the large number of LEDs. However, the proposed driver shows state-of-the-art performance in current accuracy and peak efficiency over wide input and output voltage ranges. The discontinuous low-side current sensing scheme and large number of LEDs allow to achieve high peak efficiency.

V. CONCLUSIONS

In this paper, an average current mode controlled inverse buck dimmable LED driver with an integrated current control technique is proposed and implemented. To achieve high efficiency, discontinuous low-side current sensing is adopted. The newly proposed control scheme mitigates the current accuracy limit of PCC and HCC such that the proposed LED driver achieves high accuracy while driving a large number of LEDs. The adoption of a fast-settling technique allows the driver to enter into the steady-state within 3 cycles. Implemented in a 0.35-μm HV CMOS technology, the proposed LED driver achieves current error of ±1.7% and power efficiency of 98.16% while driving 30 to 50 LEDs under 110 to 200V input voltage. The PWM dimming range is 5 to 95%. The proposed dimmable LED driver can be used for large scale single-string LED backlighting applications.

REFERENCES

[1] D. A. Steigerwald, J. C. Bhat, D. Collins, R. M. Fletcher, M. O. Holcomb, M. J. Ludowise, P. S. Martin, and S. L. Rudaz, "Illumination with Solid State Lighting Technology," *IEEE J. of Selected Topics In Quantum Electronics*, vol. 8, no. 2, pp. 310-320, Mar. 2002.

[2] M. S. Shur and A. Zukauskas, "Solid state lighting: toward superior illumination," *IEEE Proc.* vol. 93, pp. 1691-1703, Oct. 2005.

[3] J. Brodrick, "Next-generation lighting initiative at the U.S. department of energy catalyzing science into the marketplace," *IEEE Journal of Display Technology*, vol. 3, no 2, Jun. 2007.

[4] C. L. Kuo, T. J. Liang, K. H. Chen, and J. F. Chen, "Design and implementation of high frequency AC-LED driver with digital dimming," *in Proc. IEEE Int. Symp. Circuit Syst*., 2010, pp. 3713–3716.

[5] J. W. Yang and H. L. Do, "High-Efficiency ZVS AC-DC LED Driver Using a Self-Driven Synchronous Rectifier," *IEEE Trans. on Circuits & Syst., Part I*, vol. 61, no. 8, pp. 2505-2512, Aug. 2014.

[6] H. J. Chiu, Y. K. Lo, J. T. Chen, S. J. Cheng, C. Y. Lin, and S. C. Mou, " A high-efficiency dimmable LED driver for low-power lightning applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 735–743, Feb. 2010.

[7] E. C. Kang, D. Kwon, J. E. Yeon, D. S. Kim, and W. Oh, "A New Low Voltage Detecting Method for Multi-string LED BLU Circuit," *in Proc. Eur. Conf. Power Electron. Appl.*, Sep. 8–10, 2009, pp. 1–6.

[8] T. J. Oh, A. Cho, S. L. Ki, and I. C. Hwang, "A low-power and low-cost digitally-controlled boost LED driver IC for backlights," *in IEEE Asian Solid-State Circuits Conference*, Kobe, Japan, Nov. 2012, pp. 237-240.

[9] Y. T. Hsieh, B. D. Liu, J. F. Wu, C. L. Fang, H. H. Tsai, and Y. Z. Juang, " A high current accuracy boost white LED driver based on offset calibration technique," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 4, pp. 244–248, Apr. 2011.

[10] C. Wu, T. Wu, J. Tsai, Y. Chen, and C. Chen, "Multistring LED backlight driving system for LCD panels with color sequential display and area control," *IEEE Trans. Ind. Electron.*, vol. 55, no. 10, pp. 3791–3800, Oct. 2008.

[11] S. I. Hong, J. W. Han, D. H. Kim, and O. K. Kwon, "A double-loop control LED backlight driver IC for medium-sized LCDs," *in Proc. IEEE Int. Solid-State Circuit Conf. Digest Tech. Papers*, San Francisco, CA, USA, Feb. 2010, pp. 238–240.

[12] S. Y. Lee, J. W. Kwon, H. S. Kim, M. S. Choi, and S. Byun, "New design and application of high efficiency LED driving system for RGB-LED backlight in LCD display," *in Proc. 37th IEEE Power Electron. Spec. Conf.*, Jun. 2006, pp. 1–5.

[13] S. Y. Yseng, S. C. Lin, and H. C. Lin, "LED Backlight Power System with Auto-tuning Regulation Voltage for LCD Panel," *in Proc. IEEE Appl. Power Electron. Conf.(APEC)*, pp. 551-557, 2008.
[14] C. C. Chen, C. Y. Wu, and T. F. Wu, "LED back-light driving system for LCD panels," *in Proc. IEEE APEC*, Mar. 2006, pp. 381–385.
[15] S. H. Cho, S. H. Lee, S. S. Hong, D. S. Oh, and S. K. Han, "High-accuracy and cost-effective current-balanced multichannel LED backlight driver using single-transformer," *in Proc. 8th Int. IEEE ICPE ECCE*, 2011, pp. 520–527.
[16] H. J. Chiu and S. J. Cheng, "LED backlight driving system for large-scale LCD panels," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2751–2760, Oct. 2007.
[17] P. Malcovati, M. Belloni, F. Gozzini, C. Bazzani, and A. Baschirotto, "A 0.18-um CMOS, 91%-Efficiency, 2-A Scalable Buck-Boost DC-DC Converter for LED Drivers," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5392–5398, 2014.
[18] S. Moon, G. Koo, and G. Moon, "A New Control Method of Interleaved Single-Stage Flyback AC-DC Converter for Outdoor LED Lighting Systems," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4051–4062, 2013.
[19] H. Chou, Y. Hwang, and J. Chen, "An Adaptive Output Current Estimation Circuit for a Primary-Side Controlled LED Driver," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4811–4819, 2013.
[20] M. Kim, "Error Amplifier Design of Peak Current Controlled (PCC) Buck LED Driver," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6789–6795, 2014.
[21] C. Cheng, C. Chang, T. Chung, and F. Yang, "Design and Implementation of a Single-Stage Driver for Supplying an LED Street-Lighting Module With Power Factor Corrections," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 956–966, 2015.
[22] Y. Hu, L. Huber, and M. M. Jovanovic, "Single-Stage, Universal-Input AC/DC LED Driver With Current-Controlled Variable PFC Boost Inductor," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1579–1588, 2012.
[23] Q. Luo, S. Zhi, C. Zou, W. Lu, and L. Zhou, "An LED Driver With Dynamic High-Frequency Sinusoidal Bus Voltage Regulation for Multistring Applications," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 491–500, 2014.
[24] C. Zhao, X. Xie, and S. Liu, "Multioutput LED Drivers With Precise Passive Current Balancing," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1438–1448, 2013.
[25] X. Qu, S. Wong, and C. K. Tse, "An Improved *LCLC* Current-Source-Output Multistring LED Driver With Capacitive Current Balancing," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5783–5791, 2015.
[26] J. Zhang, L. Xu, X. Wu, and Z. Qian, "A Precise Passive Current Balancing Method for Multioutput LED Drivers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2149–2159, 2011.
[27] S. Uprety, H. Chen, and D. Ma, "Quasi-Hysteretic Floating Buck LED Driver with Adaptive Off-Time for Accurate Average Current Control in High Brightness Lighting," *IEEE International Symposium on Circuits & Systems*, pp. 2893-2896, May. 2011.
[28] C. H. Liu, C. Y. Hsieh, Y. C. Hsieh, T. J. Tai, and K. H. Chen, "SAR-Controlled Adaptive Off-Time Technique without Sensing Resistor for Achieving High Efficiency and Accuracy LED Lighting System," *IEEE Trans. on Circuits & Syst., Part I*, vol. 57, no. 6, pp. 1384-1394, Jun. 2010.
[29] D. K. Park, Z. Liu, and H. Lee, "A 40 V 10 W 93%-Efficiency Current-Accuracy-Enhanced Dimmable LED Driver with Adaptive Timing Difference Compensation for Solid-State Lighting Applications," *IEEE J. Solid State Circuits*, vol. 49, no. 8, pp. 1848-1860, Aug. 2014.
[30] I. H. Oh, "An analysis of current accuracies in peak and hysteretic current controlled power LED drivers," *in Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2008, pp. 572–577.
[31] M. Mezaroba, D. C. Martins, and I. Barbi, "A ZVS PWM inverter with active voltage clamping using the reverse recovery energy of the diodes," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 10, pp. 2219–2226, Oct. 2005.
[32] P. Haaf and J. Harper, "Understanding Diode Reverse Recovery and its Effect on Switching Losses," *Fairchild Power Seminar 2007*, pp. A23–A33.
[33] Z. Liu and H. Lee, "A 26W 97%-Efficiency Fast-Settling Dimmable LED Driver with Dual-nMOS-Sensing Based Glitch-Tolerant Synchronous Current Control for High-Brightness Solid-State Lighting Applications," *IEEE J. Solid State Circuits*, 2015, DOI: 10.1109/JSSC.2015.2424375, to be published.
[34] Bookly Micro Inc., "BM0152HV: Buck LED driver with 5000:1 dimming," Datasheet 2014.

Baek-Min Lim received the B.S. degree from the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2012, and the M.S. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2014, where he is currently working towards the Ph.D. degree. His research interest is the field of analog circuit designs including design and analysis of LED driver IC, automotive IC, and power management IC (PMIC).

Younghun Ko received the B.S. degree in information and communications engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2010, and the M.S. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2012, where he is currently working the Ph.D. degree. His research interests include design and analysis of power management IC (PMIC), automotive IC and LED driver IC.

Yeongshin Jang was born in Pohang, Korea, in 1983. He received the B.S. degree in information and communications engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2005, and the M.S. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2007, where he is currently working the Ph.D. degree. His research interests include design and analysis of touch controller IC.

Ok-Hwan Kwon received the B.S. degree in electronics engineering from Gyeongsang National University, Korea, in 2005, and the M.S. degrees in electrical engineering from Gyungbook National University, Korea, in 2010. From 2004 to 2010, he was with the LG Electronics Inc., Gumi, Korea, as an junior researcher. Since 2010, he has been with the Silicon Works Inc., Daejeon, Korea, as an senior researcher. His research interests are the integrated circuit designs such as display semiconductors, power management ICs, and automotive ICs.

Sok-Kyun Han received the B.S. degree in electronics engineering from Kwangju University, Korea, in 1995, and the M.S. and Ph.D. degrees in electrical engineering from Mokpo University and Mokpo Maritime University, Korea, in 1998 and 2004, respectively. From 1995 to 1998, he was with Information and Communications University,

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2499540, IEEE Transactions on Power Electronics

Daejeon, Korea, as a research assistant professor. Since 2010, he has been with the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in the Department of Electrical Engineering as a Research Associate Professor. His research interests are the CMOS-based RFIC and Microwave circuit designs. Lately, his research interests extend to extreme high-frequency (THz) circuit designs.

Sang-Gug Lee was born in Gyungnam, Korea in 1958. He received the B.S. degree in electronic engineering from the Gyungbook National University, Daegue, Korea, in 1981, and the M.S. and Ph.D. degrees in electrical engineering from University of Florida, Gainesville, Florida, in 1989 and 1992, respectively. In 1992, he joined Harris Semiconductor, Melbourne, Florida, USA, where he was engaged in silicon-based RF IC designs. From 1995 to 1998, he was with Handong University, Pohang, Korea, as an assistant professor in the school of computer and electrical engineering. From 1998 to 2009, he was with Information and Communications University, Daejeon, Korea as an assistant, associate, and professor in the school of engineering. Since March 2009, he is with KAIST, Daejeon, Korea, as a professor in the department of electrical engineering. His research interest is the silicon technology-based (especially in CMOS) radio transceiver designs, lately focusing on ultra-low power and extreme high frequencies (that is, Tera Hertz) implementations. In the past few years, his research interests also include other analog integrated circuit designs such as display semiconductors, power management ICs, and automotive ICs. From 2005 to 2009, he served as a technical committee member of IEEE ISSCC in the wireless communication technology committee. From 2005 to 2010, he served as a research director of Auto-ID Lab Korea. In 2007, his laboratory was selected as a National Research Laboratory. Since 2012, he is serving as a director of Future Promising Fusion Technology Pioneer Center, leading a research group in the area of silicon technology based THz IC design.