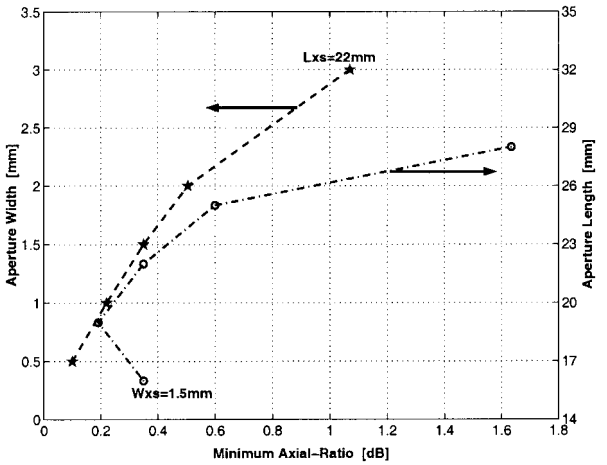

Figure 9 The minimum achievable axial-ratio versus aperture width and length

chamber for antenna measurements. This work was carried out at UTS under the Cooperative Research Centre (CRC) for Satellite Systems with financial support from the Commonwealth of Australia through the CRC Program.

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LINEARITY VS. Q-FACTOR OF LOADS FOR RF AMPLIFIERS

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ABSTRACT: *This paper analyzes and verifies that RF amplifier linearity as well as gain depend significantly on the quality of the output matching components or the loads (especially the inductor). Two amplifiers with off- and on-chip matching circuits are built and compared. Measurement results show that a driver amplifier with off-chip reactive output matching provides better linearity and gain of 3.6 dB and 1.6 dB, respectively, as compared to that of the amplifier with on-chip matching. The amplifiers are implemented for 2.4-GHz operation based on 0.35-μm CMOS technology.* © 2003 Wiley Periodicals, Inc. Microwave Opt Technol Lett 37: 286–288, 2003; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.10896

Key words: *quality factor; driver amplifier; Bluetooth; linearity; RF*

1. INTRODUCTION

Linearity is one of the key parameters that determine the performance of radio transceivers. Various techniques and approaches to improve the linearity of high-frequency amplifiers have been developed, such as increasing bias currents or voltages of the amplifier [1], optimizing the bias circuits [2], etc. This paper introduces another factor to determine the linearity of high-frequency amplifiers: the quality of the components used for output matching or loading. The discussions on linearity are based on CMOS technology but the basic principles are not technology dependent. The relation between the amplifier linearity and the output impedance are investigated in section 2 and the driver amplifier design and measurement results are discussed in section 3. A summary is presented in section 4.

2. AMPLIFIER LINEARITY VS. OUTPUT IMPEDANCE

Figure 1 shows a common-source amplifier with output matching circuit. The impedance Z_X in Figure 1 represents the overall impedances at node X, which are composed of the impedance looking into the drain of transistor M_1 and the output matching circuit along with the load resistance R_L.

The linearity of a common-source amplifier can be analyzed by viewing the relation between the drain current and the input voltage v_i at the gate of M_1. From [3], the drain current of M_1 can be given by

$$i_d = g_m v_i + \frac{g'_m}{2!}\cdot v_i^2 + \frac{g''_m}{3!}\cdot v_i^3 + \cdots, \tag{1}$$

where g_m represents the transconductance of M_1, g'_m the derivative of g_m, g''_m the derivative of g'_m. If the concepts of intercept point and power relations are applied to Eq. (1), the output 3rd-order intercept point OIP_3 of the given amplifier can be expressed as [1]:

$$OIP_3 = 10\log\left\{2\frac{(g_m)^3}{|g''_m|}\mathrm{Re}[Z_X]\right\} + 30, \tag{2}$$

where the $\mathrm{Re}[Z_X]$ is the real value of output impedance Z_X. From Eq. (2), with CMOS technology, the OIP_3 can be improved by

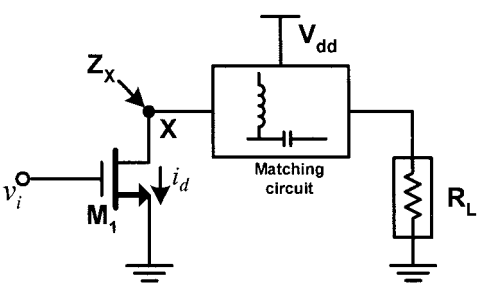

Figure 1 Common-source amplifier with output matching circuit

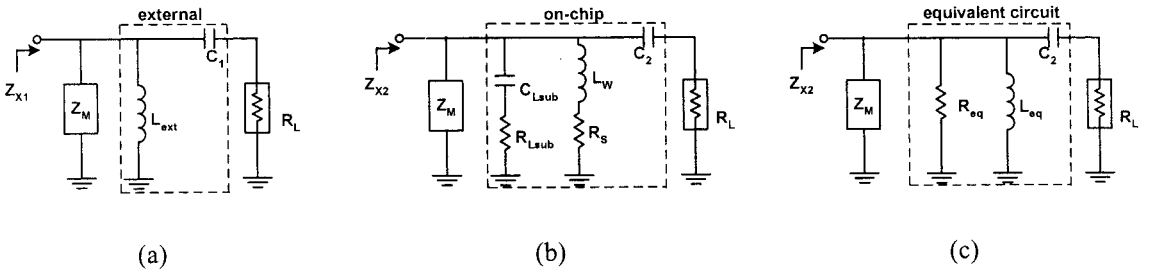

Figure 2 The small-signal equivalent representation of Z_X at node X in Fig. 1: (a) external matching; (b) on-chip matching; (c) the equivalent circuit of (b)

increasing the bias current of the amplifier such that as g_m increases, g_m'' decreases [3]. However, increasing the bias current can be in conflict with the low power requirements of a portable system.

Note that in Eq. (2) the OIP_3 of the amplifier is also a function of Re$[Z_X]$, which can be changed without additional power dissipation. Figure 2 shows the small-signal equivalent representation of Z_X at node X of Figure 1 for the off- and on-chip implementation, Figure 2(a) and (b) shows the respective matching components. In Figure 2 the impedance Z_M represents output impedance looking into the drain of transistor M_1 of Figure 1, which tends to be dominated by the drain-body capacitance with the substrate resistance. In Figure 2(a), the off-chip matching inductor L_{ext} is represented as an ideal inductor, while in Figure 2(b), the capacitor C_{Lsub}, the resistors R_{Lsub} and R_s and the inductor L_W represent the on-chip spiral inductor. Typically, the quality factor of the matching components are dominated by the inductors so that, in Figure 2, the on- and off-chip matching capacitors C_1 and C_2 are represented by ideal capacitors.

Figure 3(c) shows the equivalent circuit of Figure 3(b). In Figure 3(c), the equivalent resistor R_{eq} and inductor L_{eq} can be given by

$$R_{eq} = \frac{R_{Lsub}(Q_1^2 + 1) \cdot R_s(Q_2^2 + 1)}{R_{Lsub}(Q_1^2 + 1) + R_s(Q_2^2 + 1)}, \tag{3}$$

$$L_{eq} = L_w \cdot \frac{Q_2^2 + 1}{Q_2^2} \cdot \left(1 - \frac{R_s Q_2}{R_{Lsub} Q_1}\right)^{-1}, \tag{4}$$

where Q_1 is the quality factor for $C_{Lsub} - R_{Lsub}$ and Q_2 the quality factor for $L_w - R_s$. If $Q_1 \gg Q_2$ and $R_{Lsub} \gg R_s$, which is typically the case, Eqs. (3) and (4) can be approximated as

$$R_{eq} \approx R_s(Q_2^2 + 1), \tag{5}$$

$$L_{eq} \approx L_w. \tag{6}$$

From Eq. (5), the real values of Z_{x1} and Z_{x2} can be expressed as

$$\text{Re}[Z_{x1}] = \text{Re}[Z_M], \tag{7}$$

$$\text{Re}[Z_{x2}] = \frac{\text{Re}[Z_M] \cdot R_s(Q_2^2 + 1)}{\text{Re}[Z_M] + R_s(Q_2^2 + 1)}. \tag{8}$$

From Eqs. (7) and (8), it can be seen that Re$[Z_{x1}]$ is always larger than Re$[Z_{x2}]$, and the reduction in Re$[Z_{x2}]$ is caused by the poor quality factor of the on-chip inductor. Although Eqs. (3) and (4) are simplified to provides more intuitive understanding through Eqs. (7) and (8), the condition Re$[Z_{x1}] >$ Re$[Z_{x2}]$ is true regardless of the simplification. Note that in Figure 2(c), the poor quality factor of the on-chip inductor effectively adds an extra shunt resistor at the output node X of the amplifier shown in Figure 1. Therefore, the voltage gain as well as the linearity of the amplifier, based on Eq. (2), is reduced. Therefore, it can be said that the linearity of the amplifier, such as the one shown in Figure 1, depends significantly on the quality factor of the output matching and/or loading components. Based on above discussion, comparing Figure 2(a) and (c), the values of the impedance matching components $L_{ext} - C_1$ and $L_{eq} - C_2$ are expected to be different because they are transforming different output impedances to R_L.

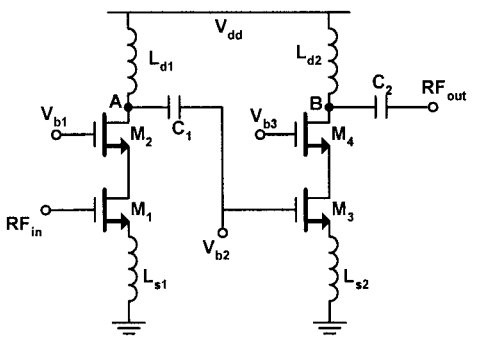

Figure 3 Driver amplifier schematic

3. DRIVER AMPLIFIER DESIGN

As a verification of the arguments discussed in the previous section, the amplifiers were built based on 0.35-μm CMOS technology. Figure 3 shows a 2.4-GHz driver amplifier schematic designed for Bluetooth application. The driver amplifier is implemented as a single-ended configuration, composed of two-stage cascode topology for higher gain. The discussion in the previous section can be applied to the given circuit without losing generality.

In Figure 3, L_{s1} and L_{s2} are bonding-wire inductors that work as degeneration components in order to improve linearity and gain

TABLE 1 Measurement Result of the Two Driver Amplifiers

	Off-Chip Matching	On-Chip Matching
Supply voltage (V)	3	3
Gain @ 2.4 GHz (dB)	17.8	16.2
Output P_{-1dB} (dBm)	6.8	3.2
NF @ 2.4 GHz (dB)	5	5.4
Total current (mA)	15	15

matching. For maximum gain, the inductor L_{d1} in Figure 3 is resonated in parallel with parasitic capacitance at the drain node of M_2. Capacitors C_1 and C_2 are used for matching and dc-blocking purposes. Inductor L_{d2} is the inductor used for the output matching. Since the overall linearity of an amplifier tends to be dominated by the linearity of the 2nd-stage [4], the effect of the quality factor of the output matching components are experimented with the 2nd-stage of the amplifier. From Figure 3, the $P_{1\text{-dB}}$ (1-dB compression point) of the driver amplifier is evaluated for the two different output matching solutions, on-chip and off-chip components. Table 1 summarizes the measured results.

As can be seen from Table 1, for the equal power dissipation of 45 mW, the driver amplifier with off-chip output matching provides better linearity and gain of 3.6 dB and 1.6 dB, respectively, as compared to that of the same amplifier with on-chip matching. In Table 1, the linearity of the amplifiers is evaluated and compared based on $P_{1\text{-dB}}$ because that is the representative linearity parameter in driver amplifiers. Typically, the IP_3 and $P_{1\text{-dB}}$ of an amplifier shows a linear relationship [4].

Figure 4 shows measured results of the input versus output response of the two driver amplifiers with on- and off-chip matching. Figure 5 shows the microphotograph of the driver amplifiers fabricated for on-chip and off-chip output matching.

4. SUMMARY

Linearity is one of the key parameters that determines the sensitivity and power efficiency of amplifiers for wireless communication transceivers. In this paper, the significant effects of the quality of the output matching and/or loading components are analyzed. This work suggest that, as a way to improve the linearity of an amplifier, the quality of the matching and/or loading components at the output of the amplifier should be maximized. As a verification of the suggested design technique, a 2.4-GHz driver amplifier is designed and fabricated based on 0.35-μm CMOS technology. The $P_{1\text{-dB}}$ of the driver amplifier is measured with on- and off-chip matching. The higher quality factor of the off-chip matching components leads to an improvement in linearity and amplifier gain of 3.6 dB and 1.6 dB, respectively. The two-stage driver amplifier dissipates 15 mA of current from a 3-V supply.

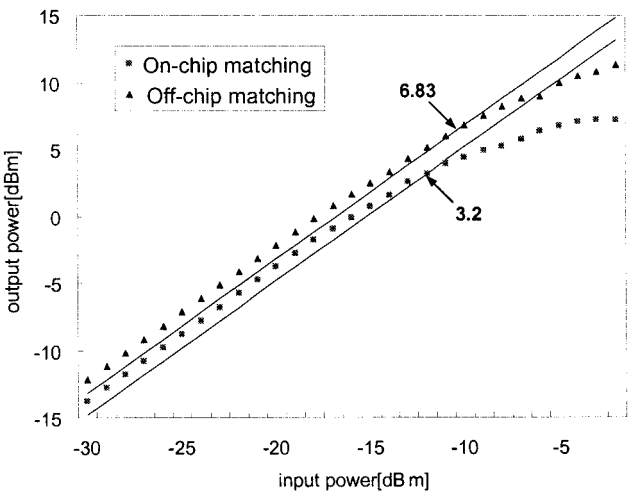

Figure 4 Measured input vs. output response of the two driver amplifiers with on- and off-chip matching

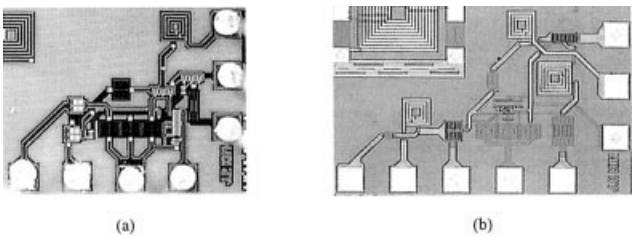

Figure 5 Microphotograph of driver amplifiers designed for (a) off-chip matching and (b) on-chip matching

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ELECTRICALLY TUNABLE DISPERSION COMPENSATOR BASED ON NONLINEARLY CHIRPED FIBER BRAGG GRATING

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ABSTRACT: *A new prototype of a compact and power-efficient tunable dispersion compensator is demonstrated. To our acknowledge, this is the first time a tunable dispersion compensator using nonlinearly chirped fiber Bragg grating, coated with on-fiber uniform metal heater, has been realized. A remarkable degree of dispersion tunability, as much as approximately 800 ps/nm, has been demonstrated.* © 2003 Wiley Periodicals, Inc.
Microwave Opt Technol Lett 37: 288–292, 2003; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.10897

Key words: *dispersion compensation; optical fiber communication; nonlinearly chirped fiber Bragg grating; optical fiber dispersion*

1. INTRODUCTION

As the speed of lightwave systems is increasing from 10 Gb/s to 40 Gb/s and beyond, tunable dispersion compensation technologies are becoming particularly important. The main reason is that, at higher bit rates, dispersion tolerances reduce dramatically (as the square of the bit rate). For example, in systems operating at bit rates of 40 Gb/s, dispersion maps will need to be accurate to within less than 50 ps/nm, and at bit rates of 160 Gb/s, less than 5 ps/nm. This means that providing systems is enormously difficult because

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