

On-Chip Interconnect Lines with Patterned Ground Shields

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Abstract—Measurements of on-chip interconnect lines with a patterned ground shield (PGS) are analyzed and compared to lines with no ground shield (NGS). At frequencies at and below 7 GHz, the PGS lines have about one fifth the dissipative loss of that of the NGS lines. By using a doped layer in the silicon for the shield, as opposed to other metal layers which are closer to the line, a reasonably high characteristic impedance is maintained. The transmission line characteristics are also analyzed.

I. INTRODUCTION

COUPLING of on-chip interconnect to the silicon substrate is a major parasitic affecting both loss and isolation in RF circuits. Substrate resistivity is fairly high in a typical RF circuit ($10 \Omega\text{-cm}$ is used here) but not high enough to prevent lossy current generated from capacitive coupling to the interconnect. In addition, the charge pushed into the substrate can flow to other parts of the circuit that may be extremely sensitive to coupling. The idea behind a ground shield is to capture that charge with a conductive layer and to provide a very low impedance path from there to ground. By allowing this alternate path, currents through the lossy and noisy substrate path are greatly reduced. To prevent the shield itself from becoming a path for parasitic current, it is patterned to allow current to flow only in the direction perpendicular to the line. (Inductively induced return or image current, antiparallel to the line, would otherwise flow in the shield.)

Coplanar waveguides with a cross-tie pattern of conductors have been used on GaAs to reduce the wavelength for practical application [1], [2] and to reduce loss [1]. This work has the first measurement known to the authors of a patterned doped layer in the silicon for which the emphasis is primarily on loss and isolation. In this sense, these PGS lines have more in common with PGS spiral inductors which have gotten much recent attention [3], [4].

II. TEST STRUCTURES

Fig. 1(a) is a layout of one of the test devices, and Fig. 1(b) is a cross-sectional plot along the cut line from “A” to “B” in Fig. 1(a). Ground straps carry the return current which actually makes this a coplanar transmission line. The line shown here

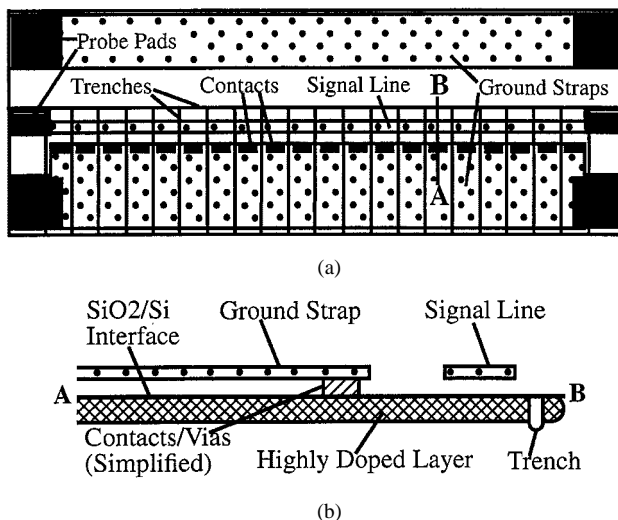


Fig. 1. (a) A plan view of the measured structure. (b) A cross-sectional view along a cut from “A” to “B.” This signal line is $1000 \mu\text{m}$ long, $25 \mu\text{m}$ wide, $3 \mu\text{m}$ thick, and is separated from the nearest ground strap by $25 \mu\text{m}$.

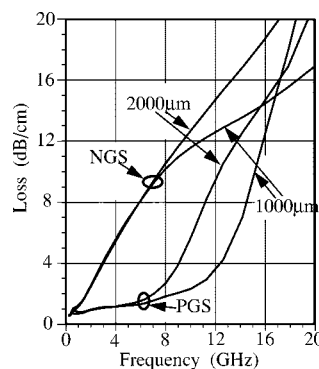


Fig. 2. Dissipative loss, $\text{loss} = -10 \log_{10} [|S_{21}|^2 / (1 - |S_{11}|^2)]$, in dB/cm versus frequency (GHz) for both PGS and NGS lines and lengths of 1000 and $2000 \mu\text{m}$.

is $1000 \mu\text{m}$ long, $25 \mu\text{m}$ wide, $3 \mu\text{m}$ thick, and is separated from the nearest ground strap by $25 \mu\text{m}$. The metal layer used for both the line and the ground straps is embedded in oxide $4 \mu\text{m}$ above the silicon and has a sheet resistance of $10 \text{ m}\Omega/\text{sq}$. In the silicon below the line and the nearest ground strap (and between) is a layer doped to $8 \Omega/\text{sq}$. This doped layer, consisting of n-type buried and sinker layers, is the capacitive shield; and it is electrically connected to one ground strap by a series of contacts as shown in Fig. 1(a). In the other direction, this doped layer extends $5 \mu\text{m}$ beyond the signal line only, and does not connect to the other ground strap. Dividing the doped layer into “tabs” is a series of trenches, transverse to the signal line, that

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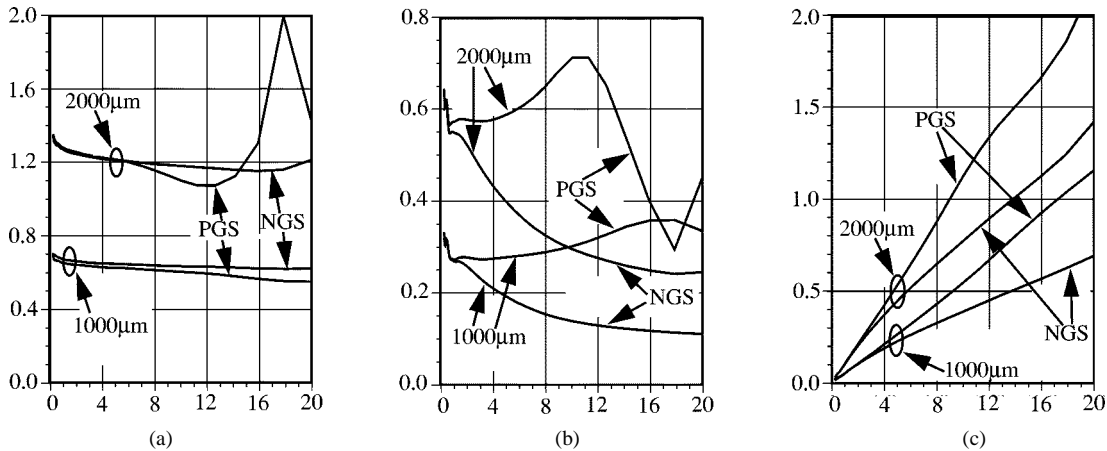


Fig. 3. (a) Inductances-per-length times the length, lL , in nH. (b) Capacitances-per-length times the length, lC , in pF. (c) The electrical lengths, $l_E = l \text{Im}(\gamma)$, in units of quarter-wavelengths versus frequency in GHz for both PGS and NGS lines with lengths of 1000 and 2000 μm . The “glitches” in the 2000- μm PGS curves are a result of the last two points spanning the resonance frequency.

prevents the lossy longitudinal parasitic return, or image, current in the doped layer. (For isolation between other devices, a p-type channel-stop implant is also used to dope the silicon below the bottom of the trenches.) Measurements were made on lines with the Patterned Ground Shields (PGS) and without (NGS) and lengths of 1000 and 2000 μm .

III. RESULTS

Fig. 2 is a plot of dissipative loss, $-10 \log_{10}(\text{power transferred to port 2 divided by the power entering from port 1}) = -10 \log_{10} 0 [|S_{21}|^2 / (1 - |S_{11}|^2)]$, versus frequency for the four devices. As expected, the PGS lines have a much lower loss than the NGS lines. For the 1000- μm lines at 6 GHz this is 1.4 dB/cm for PGS versus 8.3 dB/cm for NGS. The sharp upturn in loss at higher frequencies for the PGS lines is apparently due to an incomplete blocking of the image current by the trenches through the substrate. Experiments varying the dose of the p-type channel-stop implant, which appears below the trench bottom, show a significant decrease in loss as the implant dose is increased. This suggests that this implant helps to prevent some residual current from running under the trenches.

IV. TRANSMISSION LINE CHARACTERISTICS

The complex propagation constant (γ) and complex characteristic impedance (Z_0) are extracted using the formulas in [5]. The inductance per length, L , and capacitance per length, C , are then easily obtained from Z_0 and γ [5]. Fig. 3(a) and (b) plots lL and lC versus frequency where l is the line length (lL and lC are not exactly equal to the total inductance and capacitance because the lines are not in complete phase with themselves throughout their lengths), and Fig. 3(c) plots the electrical length. The patterned shield increases the electrical length [$l_E = l \text{Im}(\gamma)$] or decreases the wavelength of the transmission lines by significantly increasing C while keeping L nearly unchanged (at least at significant frequencies where the NGS line is in the “quasi-TEM mode”). The 1000- and 2000- μm PGS

lines reach a quarter wavelength at 17.4 and 8.8 GHz, respectively. As in [1] and [2], a metal layer could be used to perform the shielding (instead of a doping layer). With an adjacent metal layer, C could be increased by about an extra factor of 4 which would reduce Z_0 and increase the electrical length by another factor of 2. In fact, by alternating between two shielding layers on successive tabs, Z_0 or l_E could be tuned within the range bounded by using either layer alone.

With the lower losses and larger electrical lengths obtained with PGS lines, it is tempting to try to use them as on-chip transmission lines. The biggest problem with that idea is the poor quality of the ground return which is limited by series inductance to the true, off-chip ground. In a differential circuit approach, this problem is circumvented since ground can be considered to be the plane of symmetry between the two halves of the transmission line. With differential circuits, it should be noted that each “side” has half the voltage to ground (as opposed to its mirror image) but the same current. This gives differential transmission lines half the L , R , and Z_0 ; and twice the C and G as that of ordinary transmission lines.

V. CONCLUSIONS

On-chip signal lines over a doped patterned ground shield at frequencies above 1 GHz are shown to have significantly lower loss than an otherwise identical unshielded signal line. It has not been shown directly that this will also result in greatly improved isolation, but this should also be true since both the losses and substrate coupling originate from capacitively induced current pushed through the substrate. The advantage of using a doped silicon layer for the shield versus one of the closer metal layers is that the capacitance is less and the characteristic impedance is higher. PGS lines have already been used in several of our RF layouts, and although reduced loss is always desired, the primary reason in most of these cases was to reduce coupling.

Patterned shields also allow for shorter on-chip transmission lines. In spite of this, problems with ground quality (in single-ended circuits) or low characteristic impedance (in differential circuits) still hinder practical use of transmission lines on silicon with present technology.

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