ave_NACKList is not long, the NACKList is quite a long list because of the large number of slightly lossy links simulated. This may render algorithm (i) less scalable for a large multicast group.

Conclusion: We have shown that the criteria for selecting representatives based on the packet loss probability observed at the receivers is better in terms of the feedback returned. It can also differentiate receivers from different IP networks and select the optimal set of representatives.

© IEE 2001 I November 2000 Electronics Letters Online No: 20010044 DOI: 10.1049/el:20010044

Cheng Liang, Ng Chee Hock and Zhang Liren (School of Electrical and Electronic Engineering, Nanyang Technological University, Nanyang Avenue, 639798 Singapore)

E-mail: echng@ntu.edu.sg

References

- GROSSGLAUSER, M.: 'Optimal deterministic timeouts for reliable scalable multicast', *IEEE J. Sel. Areas Commun.*, 1997, SAC-15, (3), pp. 422–433
- 2 DELUCIA, D., and OBRACZKA, K.: 'Multicast feedback suppression using representatives'. Proc. INFOCOM'97, 1997, pp. 463–470

High-Q poly-to-poly capacitor for RF integrated circuits

Sang-Gug Lee, Jin-Taek Lee and Jeong-Ki Choi

A very high-Q poly-to-poly capacitor structure is proposed and measurement results are presented. The poly-to-poly capacitor is designed using a conventional $0.35\mu m$ CMOS process. By optimising the design a Q-factor of > 120 is obtained at 2GHz.

Introduction: The use of CMOS technology in wireless applications is becoming increasingly competitive. For low-power highperformance RF IC design, the availability of high-Q passive components plays a key role. Ideally, integrated capacitors should be cheap, area-efficient, linear, and have a low parasitic capacitance, especially with respect to the series resistance. In conventional silicon processes, MOS and poly-to-poly capacitors are generally provided. MOS capacitors are usually the more area efficient, although their high parasitic series resistance, strong voltage dependence, and high n^+ -silicon-to-substrate parasitic capacitances limit their usefulness for RF applications. Poly-to-poly capacitors are commendable, except for their high series parasitic resistance. Metal-to-metal (MIM) capacitors perform best, but are not available in conventional CMOS processes or require additional process steps. In this Letter, we report a significant improvement in the quality factor of poly-to-poly capacitors through layout optimisation.



Fig. 1 Small-signal equivalent circuit of practical capacitor

Capacitor design: To illustrate the capacitor design, the small-signal equivalent circuit of a practical integrated-capacitor is shown in Fig. 1. In Fig. 1, R_c represents the series spreading resistance

ELECTRONICS LETTERS 4th January 2001 Vol. 37 No. 1

of the top and bottom capacitor plate, C_c the poly-to-poly capacitance, C_{ox} the parasitic capacitance between the bottom poly and the silicon substrate, and R_{sub} the substrate resistance.



Fig. 2 Structure of high-Q poly-to-poly capacitor

a Cross-section

b Simplified three-dimensional structure Metal-2 layer is not shown

Fig. 2 shows (*a*) the cross-section and (*b*) the simplified (the metal-2 layer is not shown) 3D structure of the proposed high-Q poly-to-poly capacitor structure. In Fig. 2, the long rectangular shape poly-2 plates are used as a top capacitor plate, which covers most of the bottom poly area, except the long, narrow openings for connecting the metal-1 to the bottom plate (poly-1). Each top poly-plate is covered by the same size metal-1, and the respective poly-2 and the covering metal-1 plates are connected through multiple contacts. Therefore, the overall parasitic series resistance of the top capacitor plate becomes, effectively and approximately, the same as the spreading resistance of one rectangular metal-1 plate of the overall capacitor size. In Fig. 2, the bottom plate is effectively composed of multiple rectangular plates connected in parallel. Considering the poly-1 plate alone, the parasitic series resistance of the bottom plate is approximately equal to

$$R_{c\text{-bottom}} \simeq \frac{1}{12} R_{sh\text{-poly-1}} \frac{W_U}{L_U} \frac{1}{n} \tag{1}$$

where $R_{sh-poly-1}$ is the sheet resistance of poly-1, W_U and L_U are the width and length of the unit poly-1 rectangle, respectively, and *n* is the number of unit rectangles. In eqn. 1, the I/12 factor comes from the spreading characteristic of the poly-1 plate with metal contacts on both sides of each rectangle [1]. There is a trade-off between $R_{c-bntom}$ and the parasitic capacitance C_{ax} (see Fig. 1). Increasing the overall aspect ratio $(n \cdot W_U/L_U)$ of the bottom plate makes the bottom plate larger than the top plate, leading to higher C_{ax} .

As shown in Fig. 2b, the respective rectangular bottom plates are initially accessed through the narrow metal-1 from the outside. These narrow interconnects can introduce a significant amount of series resistance and inductance. As the capacitor size increases, the Q-factor can be limited by this interconnect parasitic. In this design, as shown in Fig. 2a, another metal layer (metal-2) is placed on top of metal-1 and connected with the bottom plate interconnect lines through a multiple via. Therefore, effectively, the one square metal-2 plate replaces the bottom plate interconnect parasitic.

So that the bottom poly has a sufficient aspect ratio, the overall series resistance of the proposed poly-to-poly capacitor can be reduced to a small value, leading to a very high quality factor.

Measurement results and discussions: The proposed high-Q capacitor was implemented using a 0.35µm CMOS process. The poly-topoly capacitor had a value of 1 fF/µm². The thickness of poly-1, poly-2, and the inter-poly oxide were 0.275, 0.18, and 0.037µm, respectively. The sheet resistances of poly-1, poly-2, metal-1, and metal-2 were 7.49, 7.78, 0.085, and 0.085Ω/□, respectively.



Fig. 3 Measured Q-factor of poly-poly capacitors as function of freauencv

- based on Y_{11} (with metal-2) based on Y_{11} (without metal-2) based on Y_{22}

The two-port S-parameters of the fabricated capacitors were measured on-wafer and the one-port O-factor was extracted from Y_{11} and Y_{22} . The bond-pad parasities were Y-parameter deembedded. Fig. 3 shows the Q-factor of a 1pF poly-to-poly capacitor as a function of frequency. In Fig. 3, the top curve represents the Q-factor based on Y_{11} , which represents the Q-factor when the signal is applied on the top plate port and the bottom plate port is grounded (see Fig. 1). As can be seen from Fig. 3, the Q-factor is higher than 120 at 2GHz, and the extrapolated Qfactor at 1 GHz is 266. This corresponds to a series resistance of 0.66Ω . Note that, considering the small series resistance of the fabricated capacitor, it is critical to ensure that the contact resistance between the probe-tip and the test structure is negligible. In Fig. 3, the middle curve represents the Q-factor based on Y_{11} when the metal-2 (see Fig. 2) is not used. At 2GHz, the Q-factor is > 80, which is respectable, although this curve demonstrates the degradation in Q-factor by the interconnect parasitic. The bottom curve of Fig. 3 shows the Q-factor based on Y_{22} , meaning the signal is applied at the bottom plate port with the top plate grounded. The Q-factor at 2GHz is less than 30. The degradation in the Q-factor reflects the effect of the substrate resistance R_{sub} (see Fig. 1).

Table 1: Q-factor comparison, published and this work

References	Capacitor type	Frequency	Q-factor
		GHz	
[2]	MOS	0.9	> 100
[3]	poly-to-poly	1	185
[4]	poly-to-poly	2	> 100
[5]	MIM	2	> 100
[6]	MIM	2	60
[7]	MIM	2.5	80
This work	poly-to-poly	2	> 120

Table 1 summarises the Q-factors of recently published high-Q capacitors [2 - 7]. As shown in Table 1, the Q-factor reported in this Letter is better than that of MIM capacitors [5 - 7].

The capacitances were extracted for the small-signal equivalent circuit shown in Fig. 1. The C_{ox} of the fabricated capacitor was approximately 20% of C_c .

Conclusions: A very high-Q poly-to-poly capacitor structure has been proposed and implemented using a conventional 0.35µm CMOS process. Based on the on-wafer measurement, a quality factor of > 120 was obtained at 2GHz from a 1pF capacitor. To the authors' knowledge, this is the highest quality factor ever reported which has been realised using conventional silicon technology. The design and the measurement details have been described.

Acknowledgment: This work is supported by the Ministry of Information and Communications, Korea, Grant # 99-S-016.

© IEE 2001 Electronics Letters Online No: 20010016

DOI: 10.1049/el:20010016

24 October 2000

Sang-Gug Lee, Jin-Taek Lee and Jeong-Ki Choi (School of Engineering, Information and Communications University, 58-4, Hwaam-dong, Yuseong-gu, Daejeon, 305-348, Korea) E-mail: sglee@icu.ac.kr

References

- ROULSTON, D.J.: 'Bipolar semiconductor devices' (McGraw Hill, 1 New York, 1990)
- HUNG, C.-M., HO, YO-CHUOL, WU, I-CHANG, and O, K.: 'High-Q capacitors implemented in a CMOS process for low-power wireless applications', IEEE Trans. Microw. Theory Tech., 1998, 46, (5), pp. 505-511
- MEGAHED, M., BENTON, R., STUBER, M., LO, L., BURGENER, M., WU, X., and CANYON, J.: 'High Q on-chip passive components for UTSi® CMOS technology'. Tech. Dig. IEEE MTT-S 1998, pp. 793-796
- STUBER, M., MEGAHED, M., LEE, J.J., KOBAYASHI, T., and DOMYO, H.: 'SOI CMOS with high-performance passive components for analog, RF, and mixed signal design'. Proc. 1998 IEEE Int. SOI Conf., 1998, pp. 99-100
- SUN, Y., VAN ZEJL, H., TAURITZ, J.L., and BAETS, R.G.F.: 'Suspended membrane inductors and capacitors for application in silicon MMIC's'. IEEE 1996 Microwave and Millimeter-Wave Monolithic Circuits Symp., 1996, pp. 99-102
- BURGHARTZ, J.N., SOYUER, M., JENKINS, K.A., KIES, M., DOLAN, M., STEIN, K.J., MALINOWSKI, J., and HARAME, D.L.: 'Integrated RF components in a SiGe bipolar technology', IEEE J. Solid-State Circuits, 1997, 32, (9), pp. 1440-1445
- BURGHARTZ, J.N., SOYUER, M., and JENKINS, K.A.: 'Microwave 7 inductors and capacitors in standard multilevel interconnect silicon technology', IEEE Trans. Microw. Theory Tech., 1996, 44, (1), pp. 100-104

Highly efficient photon-pair source using periodically poled lithium niobate waveguide

- S. Tanzilli, H. De Riedmatten, W. Tittel, H. Zbinden,
- P. Baldi, M. De Micheli, D.B. Ostrowsky and N. Gisin

A new kind of correlated photon-pair source based on a waveguide integrated on a periodically poled lithium niobate substrate is reported. Using a pump laser of a few µW at 657nm, photon-pairs are generated/degenerated at 1314nm. Detecting ~1500 coincidences per second, a conversion rate of 10-6 pairs per pump photon can be inferred, which is four orders of magnitude higher than that obtained with previous bulk sources. These results are very promising for the realisation of sources for quantum communication and quantum metrology experiments requiring a high signal-to-noise ratio or working with more than one photon-pair at a time.

Introduction: In the beginning of the 1980s, Aspect [1] performed his famous tests of Bell-inequalities to verify quantum non-locality [2], using a complicated two-photon source based on a double atomic cascade transition. Since then, more and more Bell-tests have been reported [3 - 5], taking advantage of more efficient and handy sources exploiting spontaneous parametric down-conversion (PDC) in second-order $(\chi^{(2)})$ nonlinear bulk crystals. Such sources have become an essential tool for fundamental quantum