# Load-Balance-Independent High Efficiency Single-Inductor Multiple-Output (SIMO) DC-DC Converters

Younghun Ko, Yeongshin Jang, Sok-Kyun Han, and Sang-Gug Lee

Abstract—A single-inductor multiple-output (SIMO) DC-DC converter providing buck and boost outputs with a new switching sequence is presented. In the proposed switching sequence, which does not require any additional blocks, input energy is delivered to outputs continuously by flowing current through the inductor, which leads to high conversion efficiency regardless of the balance between the buck and boost output loads. Furthermore, instead of multiple output loop compensation, only the freewheeling current feedback loop is compensated, which minimizes the number of off-chip components and nullifies the need for the equivalent series resistance (ESR) of the output capacitor for loop compensation. Therefore, power conversion efficiency and output voltage ripples can be improved and minimized, respectively. Implemented in a 0.35-µm CMOS, the proposed SIMO DC-DC converter achieves high conversion efficiency regardless of the load balance between the two outputs with maximum efficiency reaching up to 82% under heavy loads.

*Index Terms*—Single-inductor multiple-output (SIMO) DC-DC converter, switching sequence, DC-DC converter, PMIC

#### I. INTRODUCTION

Along with the growth of the battery-powered portable device market, the development of efficient power management integrated circuits (PMIC) is a popular and active research area. A DC-DC converter, which is a core block in PMIC, provides a regulated output voltage from a linearly discharging battery voltage in portable devices. In many portable devices which require multiple regulated output voltages from a single battery, implementing separate DC-DC converters can be a viable means of generating multiple output voltages. However, the separate DC-DC converter approaches lead to increase in cost and size due to the required multiple offchip inductors, which is not desirable in portable devices. To circumvent this issue, single-inductor multiple-output (SIMO) DC-DC converters have been proposed, which require only one inductor in regulating multiple output voltages [1-6]. With all DC-DC converters, achieving high conversion efficiency is critically important and SIMO DC-DC converters are no exception; furthermore, there are several design issues such as cross regulation, system stability, etc. Addressing these issues, various SIMO DC-DC converters [1-6] have been reported, which can be categorized based on the energizing methods. The works reported in [1] and [2], which adopt multiple energizing cycles per switching period, introduced time-multiplexing control and freewheel switching in discontinuous conduction mode (DCM) and pseudo-continuous conduction mode (PCCM), respectively. They have shown good cross-regulation performances by the adoption of decoupling time among multiple outputs. On the other hand, [3-6] reported SIMO DC-DC converters that adopt single energizing cycle per switching period, respectively. The former shows greater accuracy characterized by the smaller output voltage ripples and faster control loops than the latter. [3-5] have proposed control schemes, each with its own advantages, However, the applications of the proposed control

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Fig. 1. Control sequence of a previously reported SIMO DC-DC converter [6].

schemes are limited due to the difficulties in implementing buck and boost outputs simultaneously. In [6], the converter provides both buck and boost outputs simultaneously with smaller number of power switches while adopting hysteresis mode, overcoming the stability problem that arises during unbalanced output loads. However, implementing the hysteresis mode in [6] not only requires additional blocks such as a power comparator and a delta-voltage generator circuits, but it also degrades the power conversion efficiency. This paper proposes a new switching sequence to generate multiple buck and boost outputs without requiring additional blocks while achieving high conversion efficiency.

This paper is organized as follows. Section II and III introduce the newly proposed switching sequence and peak-current control scheme, respectively. Then, the design details of a DC-DC converter that adopts the proposed control sequence are described in Section IV and the measurement results are given in Section V. The conclusions are given in Section VI.

# II. PRINCIPLE OF THE PROPOSED CONTROL TOPOLOGY

Fig. 1 shows the control sequence of a previously reported SIMO DC-DC converter [6]. It can generate multiple buck and boost outputs in two modes, the PWM or the hysteresis mode, depending on the load balance condition. The PWM mode is enabled when the total current of the boost output is larger than that of the buck output. Otherwise, the buck and boost outputs are regulated under the hysteresis mode. In the hysteresis mode, the conversion efficiency is degraded because the current flows not through the inductor but the resistive freewheeling switch as the buck output is charged. The power loss by the hysteresis mode is given by,

$$I_{OA} \cdot T_S = (I_R + I_L) \cdot T_A \approx I_R \cdot T_A \tag{1}$$

$$= (V_N - V_{OA}) \cdot I_{OA}, \tag{2}$$

where  $V_{IN}$  is the input voltage,  $V_{OA}$  the buck output voltage,  $V_{OB}$  the boost output voltage,  $V_R$  the voltage drop between the freewheeling switch,  $I_{OA}$  the buck load current,  $I_{OB}$  the boost load current,  $I_R$  the



Fig. 2. Control sequence of a proposed SIMO DC-DC converter.

current through the resistive freewheeling switch,  $T_S$  the switching period,  $T_A$  the time of phase-(1-2) and  $P_{LOSS}$  the power loss during the hysteresis mode. The conduction loss in the hysteresis mode leads to the drops in conversion efficiency at the load balance boundary. Furthermore, to determine the mode of proper operation, a power comparator and a delta-voltage generator are required.

Fig. 2 shows a control sequence that is proposed to resolve aforementioned problems. In Fig. 2, during phase-(1), the switches SW1 and SW4 are turned on to charge the buck output. The inductor current  $I_L$  then ramps up by the rate of  $(V_{IN} - V_{OA})/L$ . The next phase is then determined as either phase-(2-1) or phase-(2-2) depending on the output load condition. When the buck output finishes charging to a desired voltage level before the inductor current reaches a peak-current  $I_p$ , which can be controlled by the previously reported techniques [4] or [6], phase-(2-1) is selected. Then, the switches SW1 and SW3 are turned on to energize the inductor during phase-(2-1), which makes  $I_L$  increase with a slope of  $V_{IN}/L$  until  $I_L$  reaches  $I_p$ . On the other

hand, phase-(2-2) is chosen if more energy is required to regulate the buck output when  $I_L$  reaches  $I_p$ . During phase-(2-2), switches SW2 and SW4 are turned on to deliver more charges to the buck output while  $I_L$  ramps down at a rate of  $-V_{OA}/L$ . After phase-(2-1) or phase-(2-2) is finished, phase-(3) begins and then  $I_L$  ramps down at a rate of  $(V_{IN} - V_{OB})/L$  with switches SW1 and SW5 turned on. As soon as the boost output reaches the desired voltage, phase-(3) transfers to phase-(4) which is a freewheeling period. In phase-(4), switches SW2 and SW3 are turned on to hold  $I_L$  constant. At the end of the switching period, the cycle returns to phase-(1). In summary, in Fig. 2, two types of control sequences are used to regulate the buck and the boost outputs depending on output load condition, as shown in Table 1. Note that, high conversion efficiency can be achieved as the energy delivery is made continuously by flowing energy through the inductor. Moreover, the decision process between phase-(2-1) and phase-(2-2) can be implemented digitally without requiring additional blocks and the cross regulation problem can be minimized due to the freewheeling period [2].

Load condition	Control sequences	
IBuck < IBoost	$1 \rightarrow 2\text{-}1 \rightarrow 3 \rightarrow 4$	
IBuck > IBoost	$1 \rightarrow 2-1 \rightarrow 3 \rightarrow 4 \rightarrow 1 \rightarrow 2-2 \rightarrow 3 \rightarrow 4$	

Table 1. Control sequences depending on the load condition

# **III. PEAK-CURRENT CONTROL SCHEME**

The peak-current  $I_p$ , which is one of the factors that determines the duty-cycle for each phase, can be controlled by various schemes such as the loaddependent peak-current control [6], the freewheeling current feedback control [4], etc. In order to adopt the load-dependent peak-current control scheme, all output voltages including both the buck and boost output should be sensed by error amplifiers. The error signals between the output voltages and their reference voltages are used to control the peak current level. Generally, this scheme requires off-chip components for a feedback loop compensation of each output because the required capacitor values are too large to be integrated. The number of off-chip components is proportional to the number of outputs of the SIMO DC-DC converter, which debases the usefulness of the SIMO DC-DC converter. On the other hand, in the freewheeling current feedback control scheme, the output voltages are regulated directly by comparators. A single compensation is sufficient for a freewheeling feedback loop. Thus, both cost and chip area can be reduced simultaneously. Furthermore, the equivalent series resistance (ESR) of the output capacitor, which makes a negative zero for loop compensation, is unnecessary. Therefore, by adopting a capacitor with a small ESR (ESR of a ceramic capacitor is smaller than that of a tantal capacitor), not only the output voltage ripples can be reduced but also the power conversion efficiency can be improved. Considering aforementioned advantages, the freewheeling current feedback control scheme [4] is adopted to implement the SIMO DC-DC converter with the proposed control sequence. The concept of the freewheeling current feedback control scheme is to control the peak current by comparing the average of the freewheeling current with a reference current. Due to the differences in control sequence, the DC and AC characteristics of the proposed SIMO DC-DC converter are different from those of [4] even though the same concept of the freewheeling current feedback

control is used. Depending of the load condition, there are two cases of operational DC and AC characteristics. Each case is analyzed in the following.

#### 1. Case-I : Buck load current < Boost load current

Fig. 3 shows the waveform of the inductor current when the current of boost output is larger than that of buck output where  $i_{k1}$  is the inductor current at the point where phase-(1) ends and  $i_{fw1}$  the freewheeling current during phase-(4). The duration of each phase, shown in Fig. 3, is given by

$$d_{k1} = \frac{f_s}{m_K} \cdot (i_{k1} - i_{fw1})$$
(3)

$$d_{n1} = \frac{J_s}{m_{N1}} \cdot (i_p - i_{k1}) \tag{4}$$

$$d_{t1} = \frac{J_s}{m_T} \cdot (i_p - i_{fw1}) \tag{5}$$

$$d_{f1} = 1 - d_{k1} - d_{n1} - d_{t1}, (6)$$



Fig. 3. Inductor current waveform for case-I (Buck < Boost).



Fig. 4. Inductor current waveform for case-II (Buck > Boost).

where  $f_s$ ,  $m_K$ ,  $m_{N1}$ , and  $m_T$  are the switching frequency,  $(V_{IN} - V_{OA})/L$ ,  $V_{IN}/L$ , and  $-(V_{IN} - V_{OB})/L$ , respectively. The average value of the freewheeling current, which should be regulated to the reference current  $(I_{ref})$ , is given by

$$\langle i_{f1} \rangle_T = d_{f1} \cdot i_{fw1}. \tag{7}$$

The average value of currents supplied to the buck and boost outputs are given by

$$\langle i_{ok} \rangle_T = \frac{1}{2} \cdot (i_{k1} + i_{fw1}) \cdot d_{k1}$$
 (8)

$$\langle i_{ot} \rangle_T = \frac{1}{2} \cdot (i_p + i_{fw1}) \cdot d_{t1}.$$
(9)

From (3)-(9), the DC operating point is determined. At the given DC operating point, the small signal gain  $(G_1(s))$  from the perturbation of the peak current  $(\hat{i}_p)$ to the perturbation of the averaged freewheeling current  $(\hat{i}_{f1})$  can be calculated by constructing perturbation variable matrices as shown in Table 2. The calculated  $G_1(s)$  is used for determining the loop gain of the freewheeling feedback loop as described in Section IV.

#### 2. Case-II : Buck load current > Boost load current

The inductor current waveform when the current of boost output is smaller than that of buck output is shown in Fig. 4 where  $i_{k2}$  is the inductor current at the end of phase-(1),  $i_{k3}$  the inductor current at the end of phase-(2-2),  $i_{fw2}$  the freewheeling current during  $d_{f2}$ , and  $i_{fw3}$  the freewheeling current during  $d_{f3}$ . The duration of each phase is given by

$$d_{k2} = \frac{f_s}{m_K} \cdot (i_{k2} - i_{fw3}) \tag{10}$$

$$d_{n2} = \frac{J_s}{m_{N1}} \cdot (i_p - i_{k2}) \tag{11}$$

$$d_{t2} = \frac{J_s}{m_T} \cdot (i_p - i_{fw2})$$
(12)

$$d_{f2} = 1 - d_{k2} - d_{n2} - d_{t2}$$
(13)  
$$d_{k3} = \frac{f_s}{f_s} \cdot (i_n - i_{fw2})$$
(14)

$$d = \frac{f_s}{m_K} \cdot (i - i_k)$$
(15)

$$d_{12} = \frac{f_s}{m_{N2}} \cdot (i_{12} - i_{522}) \tag{16}$$

$$d_{f3} = 1 - d_{k3} - d_{n3} - d_{t3}, \tag{10}$$

where  $m_{N2}$  is  $V_{OA}/L$ . The average freewheeling current, which should be equal to  $I_{ref}$ , is given by

$$\langle i_{f_2} \rangle_T = \frac{1}{2} \cdot (d_{f_2} \cdot i_{f_{W2}} + d_{f_3} \cdot i_{f_{W3}}).$$
 (18)

The average currents supplied to the buck and boost outputs are given by

$$\langle i_{ok} \rangle_T = \frac{1}{2} \cdot (i_{k2} + i_{fw3}) \cdot d_{k2}$$
 (19)

$$= \frac{1}{2} \cdot \{ (i_p + i_{fw2}) \cdot d_{k3} + (i_p + i_{k3}) \cdot d_{n3} \}$$
(20)

$$\langle i_{ot} \rangle_T = \frac{1}{2} \cdot (i_p + i_{fw2}) \cdot d_{t2} \tag{21}$$

$$= \frac{1}{2} \cdot (i_{k3} + i_{fw3}) \cdot d_{t3}.$$
(22)

(7)

Eqs. (12)-(24) determine the DC operating point. At the given DC operating point, the small signal gain  $(G_2(s))$  from  $\hat{i}_p$  to the perturbation of the averaged freewheeling current  $(\hat{i}_{f2})$  can be obtained using perturbation variable matrices shown in Table 2. The calculated  $G_2(s)$  is used for determining the loop gain of the freewheeling feedback loop as described in Section IV.

#### **IV. IMPLEMENTATION DETAILS**

Fig. 5 shows the block diagram of the proposed SIMO DC-DC converter that can achieve high efficiency



Fig. 5. Block diagram of the proposed SIMO DC-DC converter.

# Table 2. Perturbation variable matrices

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Case-I: Buck load current < Boost load current  

$$\begin{pmatrix} \frac{m_{K}}{f_{s}} & 0 & 0 & -1 & 1\\ 0 & \frac{m_{N1}}{f_{s}} & 0 & 1 & 0\\ 0 & 0 & \frac{m_{T}}{f_{s}} & 0 & 1\\ 0 & 0 & l_{p} + l_{fw1} & 0 & D_{t1}\\ l_{k1} + l_{fw1} & 0 & 0 & D_{k1} & D_{k1} \end{pmatrix} \begin{pmatrix} \hat{d}_{k1}\\ \hat{d}_{n1}\\ \hat{d}_{t1}\\ \hat{l}_{fw1} \end{pmatrix} = \begin{pmatrix} 0\\ 1\\ 1\\ -D_{t1} \end{pmatrix} \hat{l}_{p}$$

$$\hat{l}_{f1} = (-l_{fw1} & -l_{fw1} & 0 & D_{f1}) \begin{pmatrix} \hat{d}_{k1}\\ \hat{d}_{n1}\\ \hat{d}_{t1}\\ \hat{l}_{k1} \end{pmatrix}$$

$$G_{1}(s) = \frac{\hat{l}_{f1}}{\hat{l}_{p}} = G_{1,0} = \frac{l_{p} \cdot \left(\frac{fs \cdot (l_{fw1} - l_{k1})}{m_{K}} + \frac{fs \cdot (l_{fw1} - l_{p})}{m_{T}} + \frac{fs \cdot (l_{fw1} - l_{p})}{l_{k1} \cdot m_{K}} - \frac{l_{fw1} \cdot fs \cdot (l_{k1} - l_{p})}{l_{k1} \cdot m_{N1}} \end{pmatrix}$$
(23)

# Case-II : Buck load current > Boost load current

independent of the load balance. The design parameters are chosen as  $L = 10 \,\mu\text{H}$ ,  $V_{IN} = 3.7 \text{ V}$ ,  $V_{OK} = 1.8 \text{ V}$ ,  $V_{OT} = 5 \text{ V}, \quad f_s = 1 \text{ MHz}, \text{ and } I_{ref} = 30 \text{ mA}.$  The proposed control sequence, which was explained in the previous section, can be implemented by switch control logic shown in Fig. 6. The main purpose of the switch control logic is to determine whether the buck output voltage reaches the desired buck voltage before the inductor current reaches the peak current or not. Depending on the decision, the timing of switch control signals  $(V_{SWI}, V_{SWN1}, V_{SWN2}, V_{SWT}, \text{ and } V_{SWK})$  becomes different as shown in Fig. 2. The required input signals  $CM_K$ ,  $CM_T$ , and  $CM_R$  of the switch control logic represent whether the buck output voltage, the boost output voltage, and the inductor current reach the desired buck output voltage, the desired boost output voltage, and the peak inductor current or not, respectively. The design details of the sub-blocks, shown in Fig. 5, are described in the following sub-sections.

#### 1. Peak-Current Control Circuit

The peak-current control circuit which is an integrator with single pole, shown in Fig. 5, is shown in Fig. 7. In Fig. 7, for accurate operation, the value of  $I_{ref}$  is chosen to make the freewheeling durations ( $D_{f1}$ ,  $D_{f2}$ and  $D_{f3}$ ) to be larger than 10% of the switching period considering the transition time of the freewheeling current sensor from an OFF to ON-state. Adequate freewheeling durations also guarantee good cross-regulation performance. In Fig. 5,  $I_{lps} (= I_{lp} / N_1)$  and  $I_{fs} (= I_f / N_2)$  are the scaled-down current from the peak-current sensor and the freewheeling current sensor, respectively. In Fig. 5, the loop gain of the freewheeling feedback loop is given by

$$T(s) = \frac{N_1}{N_2 \cdot R_P} \cdot G(s) \cdot A(s)$$
  
=  $\frac{1}{R_P} \cdot \frac{G_0 \cdot R_c}{1 + s R_c \cdot C_c'}$  (25)

where  $N_1 = N_2 = N$ ,  $R_p$  is the value of a resistor in the I-V converter (I-V conversion ratio), and G(s) can be either  $G_1(s)$  or  $G_2(s)$  depending on the load condition. Since G(s) is a variable that depends on the load condition, the feedback loop should be compensated for the worst case. Fig. 8 shows the small signal gain  $G_0$ versus the buck and boost load currents. Generally, the unity gain frequency of a feedback loop, which should be sufficiently lower than the Nyquist rate, is set at one tenth of the switching frequency. Since the effective frequency of the inductor current waveform for case-II is one half of the switching frequency  $f_s$ , the unity gain frequency  $(f_u = G_0 / (2\pi \cdot R_p \cdot C_c))$  of the freewheeling feedback loop is adjusted to be about  $f_s/20$ . Fig. 9 shows the loop-gain of the freewheeling feedback loop for the worst case with  $I_{OK} = 20 \text{ mA} \text{ and } I_{OT} = 20 \text{ mA}$ .



Fig. 6. Switch control logic.



Fig. 7. Peak-current control circuit.



Fig. 8. Small signal gain  $G_0$  versus load currents  $I_{ok}$  and  $I_{ot}$ .



Fig. 9. Loop-gain of the freewheeling feedback loop.

# 2. Slope Compensation Circuit

The slope compensation for buck and boost output voltages is required to avoid sub-harmonic oscillation [4]. If the charging operations of buck and boost outputs for every cycle are not guaranteed, various inductor current waveforms can be generated with effective switching frequencies different from the desired value. This makes the DC and AC characteristics of the DC-DC converter unpredictable. For the slope compensation, a ramp signal is added to the buck and boost output voltages, typically in the form of current, which requires V-I converters and a ramp signal generator [4]. The proposed slope compensation circuit, shown in Fig. 10, does not need V-I converters and a ramp signal generator. In Fig. 10,  $V_{FK}(V_{FT})$  is the scaled-down output voltage of the buck (boost) while  $V_{IK}(V_{IT})$  is the sum of the ramp signal and  $V_{FK}(V_{FT})$ . The operational principle of the slope compensation circuit shown in Fig. 10 is described in Fig. 11. In Fig. 11, the ramp signal is added only when  $V_{SWK}(V_{SWT})$  is low. The slopes of the additive ramp signal are given by

$$m_{ram\ p,K} = \frac{I_b}{C_{K2}}$$
 and  $m_{ram\ p,T} = \frac{I_b}{C_{T2}}$ , (26)

respectively.  $m_{ramp,K}$  and  $m_{ramp,T}$  should be large enough to assure steady-state operation. Note that, however, excessive slope of the additive ramp signal degrades the load regulation performance.

#### 3. Current Sensor

Conventional current sensors [1] as shown in Fig. 12



Fig. 10. Slope compensation circuit.



Fig. 11. Timing diagram of the slope compensation circuit.



Fig. 12. Schematic of (a) peak-current, (b) freewheeling current sensors.

are adopted for the peak-current (Fig. 12(a)) and freewheeling current (Fig. 12(b)) sensors. In Fig. 12, the current sensors copy the voltage drop across a power switch into a scale-downed transistor with a scaling ratio of N. Then, the sensed currents ( $I_{lps}$  and  $I_{fs}$ ), which has been scale-downed, flow through the scale-downed transistor.

#### 4. Dead Time Control Logic

In Fig. 5, when more than two power switches are simultaneously turned on at a given node, a large shoot-through current can flow, which degrades the conversion efficiency. Thus, a dead time control logic, which secures the definite turn - OFF of all other switches when one of the switches is ON, is designed as the way shown in Fig. 13. In Fig. 13, over and reverse current protection circuits are also included to protect the DC-DC converter system and to prevent undesirable power loss. When the inductor current exceeds the maximum allowed current, SW1 and SW2 immediately turns OFF and ON, respectively, for the reduction of the inductor current. The maximum allowed inductor current is given by



Fig. 13. Dead time control logic.

$$I_{L,MAX} = \frac{N \cdot V_{REF}}{R_{OCP}},$$
(27)

where N is the current scaling ratio in the current sensor,  $R_{OCP}$  the value of a resistor in the I-V converter (I-V conversion ratio), and  $V_{OCP} = I_L \cdot R_{OCP} / N$ . There are two reverse current protection cases that can occur, which can be detected by monitoring the sign of the voltage drop across SW1 ( $V_{IN} - V_X$ ) or SW2 ( $V_X - GND$ ). During the buck operation of case-II (buck > boost),  $I_L$  ramps down with SW2 turned ON. If the charging operation of buck output is not finished even if  $I_L$  is reduced to zero, a sign change in the voltage drop across SW2 promptly turns OFF SW2 to stop the current loss from the buck output. The current protection mechanism is similar during the boost operation as well.

# V. MEASUREMENT RESULTS

The proposed SIMO DC-DC converter is implemented in a 0.35-  $\mu$ m single poly 4 metal CMOS technology. Fig. 14 shows the chip micrograph of the proposed SIMO DC-DC converter with a size of 1460  $\mu$ m x 1250  $\mu$ m including pads. The proposed SIMO DC-DC converter is implemented with the following design parameters :  $C_{OK} = C_{OT} = 22 \ \mu$ F,  $L = 10 \ \mu$ H,  $V_{IN} = 3.7 \ V$ ,  $V_{OK} = 1.8 \ V$ ,  $V_{OT} = 5 \ V$ , and  $f_s = 1 \ MHz$ . Fig. 15 shows the measured output voltage waveforms for the maximum output load currents showing both buck and boost output voltages simultaneously. Fig. 16 shows the measured output voltages and inductor current waveforms. Fig. 16(a) shows the waveform of the



Fig. 14. Micrograph of the proposed SIMO DC-DC converter.



Fig. 15. Output voltage settings.

inductor current when the boost load current is larger than the buck load current, while Fig. 16(b) shows for the other case. The operational mode change, shown in Fig. 16, depending on the output load condition proves that the output voltages can be regulated without inductor current accumulation by adopting the proposed control sequences regardless of the output load conditions. Note that, the inductor current stays constant ideally during the freewheeling phase. However, the measured inductor current decreases considerably during the freewheeling phase in Fig. 16 due to non-idealities such as the direct current resistance (DCR) of the inductor and the switch resistance. This conduction loss could degrade the power conversion efficiency. Fig. 17 shows the maximum



**Fig. 16.** Output voltages and inductor current waveforms for (a) case-I ( $I_{OK}$  =10 mA and  $I_{OT}$  =80 mA), (b) case-II ( $I_{OK}$  =80 mA and  $I_{OT}$  =10 mA).



Fig. 17. Maximum output ripples for  $I_{OK}$  =80 mA and  $I_{OT}$  =80 mA.

output ripples for the maximum output load currents. In Fig. 17, the maximum peak-to-peak output ripples of the buck and boost outputs are 5.6 and 4.8 mV without spike,

respectively.

Since the operation of the proposed scheme is stable even for a small value of ESR, the output voltage ripples could be minimized. Fig. 18 shows the measured load transient response for the change in the pulse loads of 10 to 80 mA. The load regulations of the buck and boost outputs over the load current variations are 10 and 32 mV, respectively. Fig. 19 shows the measured line transient response for the step line voltage change of 3 to 4 V. The line regulations of the buck and boost outputs for the given line voltage variations are 7 mV in both cases. The measured power conversion efficiency of the proposed SIMO DC-DC converter is shown in Fig. 20, verifying the high conversion efficiency regardless of the output load conditions. It can be seen that there is no drops in conversion efficiency with mode change at the boundary of load balance. In Fig. 20, the proposed control scheme





**Fig. 18.** Load transient response for (a)  $I_{OK}$  changes of 10 mA to 80 mA under  $I_{OT}$  =10 mA, (a)  $I_{OT}$  changes of 10 mA to 80 mA under  $I_{OK}$  =10 mA.



Fig. 19. Line transient response for line variations of 3 V to 4 V with  $I_{OK}$  =40 mA and  $I_{OT}$  =40 mA.



**Fig. 20.** The measured conversion efficiency of the proposed SIMO DC-DC converter.

Table 3. Performance summary

Process	0.35- μm CMOS	
Chip area	1460 μm x 1250 μm	
Input voltage	3.7 V (3 - 4 V)	
Switching frequency	1 MHz	
Inductor	$10 \ \mu H$ (400 mΩ DCR)	
Output capacitor	$22 \ \mu F$ (10 m $\Omega$ ESR)	
Converter type	Buck ( $V_{OK}$ )	Boost ( $V_{OT}$ )
Output voltage	1.8 V	5 V
Maximum load current	80 mA	80 mA
Output ripples	$5.6 mV_{pp}$	$4.8 mV_{pp}$
Load regulation	0.142 mV/mA	0.457 mV/mA
Line regulation	7 mV/V	7 mV/V

achieves the maximum conversion efficiency of 82 % under heavy load conditions. Table 3 summarizes the key performances of the proposed SIMO DC-DC converter.

# **VI.** CONCLUSION

In this paper, a single-inductor multiple-output (SIMO) DC-DC converter, capable of regulating buck and boost outputs with high efficiency independent of load balance, is proposed and implemented. By adopting a newly proposed control sequence, input energy can be delivered to the outputs continuously through a lossless inductor without current accumulation. Thus, the proposed SIMO DC-DC converter can achieve high efficiency independent of the load condition. The design details of several sub-blocks are described, which assist the operation of digital processing of the proposed control sequence. Implemented in a 0.35-  $\mu$ m CMOS technology. the measurement results of the proposed SIMO DC-DC converter show the maximum conversion efficiency of 82% under heavy load conditions.

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