A Fast Low Dropout Regulator with High Slew Rate and Large Unity-Gain Bandwidth

Younghun Ko, Yeongshin Jang, Sok-Kyun Han, and Sang-Gug Lee

Abstract—**A low dropout regulator (LDO) with fast transient responses is presented. The proposed LDO eliminates the trade-off between slew rate and unity gain bandwidth, which are the key parameters for fast transient responses. In the proposed buffer, by changing the slew current path, the slew rate and unity gain bandwidth can be controlled independently. Implemented in 0.18-μm high voltage CMOS, the proposed LDO shows up to 200 mA load current with 0.2 V dropout voltage for 1 μF output capacitance. The measured maximum transient output voltage variation, minimum quiescent current at no load condition, and maximum unity gain frequency are 24 mV, 7.5 μA , and higher than 1 MHz, respectively.**

Index Terms—**Low dropout regulator, LDO, load transient response, slew rate, unity gain bandwidth**

I. INTRODUCTION

The regulator is an essential block in battery powered mobile devices. In systems with linearly discharging battery voltage over time, regulators can provide constant voltage to the circuits. There are two types of regulators: the switching regulators, such as DC-DC converters, and linear regulators, such as LDO. Even though the power efficiency of linear regulators is lower than that of the switching regulators, linear regulators are still critically important for noise sensitive RF and analog circuits because of their low output voltage ripple. Moreover, linear regulators are inexpensive, reliable, and much simpler than switching regulators. LDO provides relatively high efficiency due to the small difference between its input and output voltages. The major design issues of LDO include low quiescent current, high maximum output current, low dropout voltage, small output voltage variation for abrupt load current changes, and stability [1].

A basic LDO topology consists of an error amplifier, band-gap reference, PMOS pass transistor, and two feedback resistors. The operation of an LDO is based on the feedback of an amplified error signal in order to control the load current by adjusting the gate voltage of a PMOS pass transistor. Generally, the size of a PMOS pass transistor is quite large in order to accommodate the high load current with small dropout voltage, which means that the parasitic capacitance of the PMOS pass transistor is large. Since the output resistance of the error amplifier is also high, the output node of the error amplifier develops a low frequency pole. If both the dominant pole generated by the output capacitor and the non-dominant pole caused by the error amplifier output resistance in combination with the input capacitance of the pass transistor are located at frequencies lower than the unity gain frequency of the LDO loop, the loop stability cannot be guaranteed.

In order to guarantee both the loop stability and fast transient response of LDO, the buffer impedance attenuation (BIA) technique is proposed in [1], which adopts a buffer with a dynamically biased shunt feedback to locate the non-dominant poles at frequencies higher than the unity gain frequency. However, both large loop bandwidth and high slew rate, which are necessary for the fast transient response of LDO, could not be achieved

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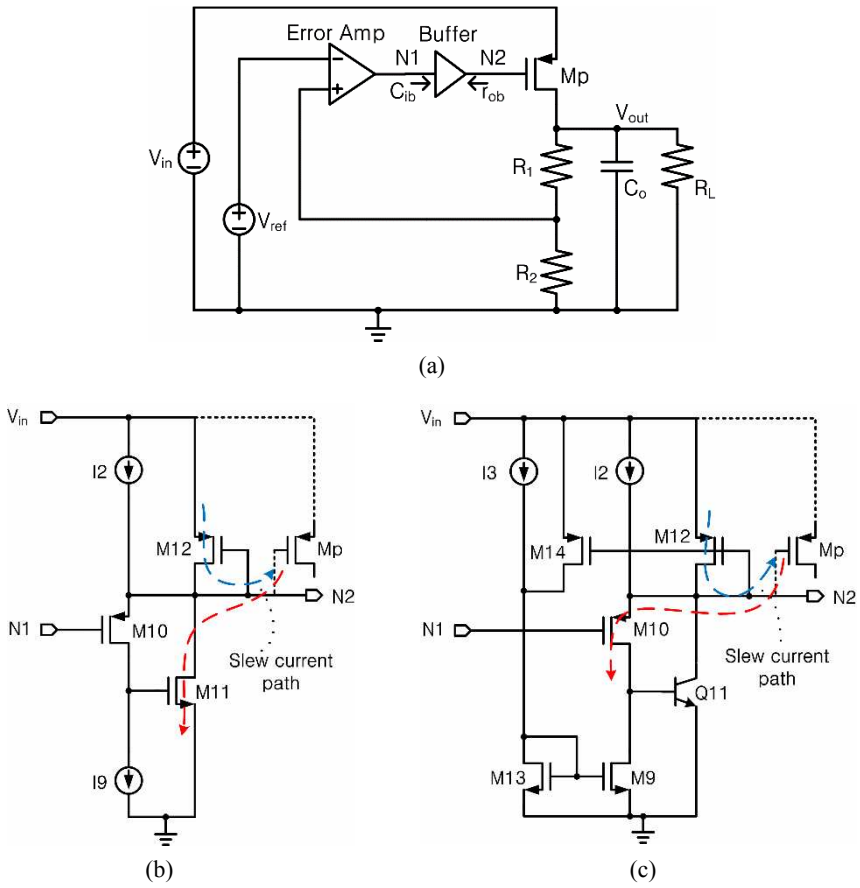

Fig. 1. Schematic of LDO (a) with a buffer, (b) proposed buffer circuit, (c) reported buffer circuit [1].

simultaneously in [1] due to the trade-off relation between the two. This work proposes a solution to the problem.

Section II introduces the newly proposed buffer schematic and its operational principle. Then, the design details of an LDO that adopts the newly proposed buffer and the measurement results are given in Section III. The conclusions are given in Section IV.

II. Principle of the Proposed LDO with Change in Slew Current Path

1. Operational Principle

Fig. 1(a) shows the LDO architecture with a buffer. In the LDO architecture shown in Fig. 1(a), there are three poles located at the outputs of error amplifier node (N1), buffer node (N2), and LDO output node (V_{out}), respectively, and the pole at the output of the LDO tends to be the dominant. If the input capacitance (C_{ib}) and output resistance (r_{ob}) of the buffer are small so that the non-dominant poles can be located at frequencies much higher than the unity gain frequency of the LDO loop, a single pole feedback loop can be achieved and the system becomes stable. In Fig. 1(b), in order to achieve a single pole feedback loop, a buffer with dynamically biased shunt feedback technique modified with slew current path change is proposed. In the buffer, a negative feedback loop is formed by M_{11} to reduce the output resistance of the buffer, which can be given by

$$r_{ob} \approx \frac{1}{g_{m11}(g_{m10} \cdot r_{o10}) + g_{m12}}, \quad (1)$$

where g_{m10}, g_{m11}, and g_{m12} are the transconductance of M_{10}, M_{11}, and M_{12}, respectively, and r_{o10} the output resistance of M_{10}. In Fig. 1(b), without the feedback loop, i.e, without M_{11}, a trade-off relation

exists among input capacitance, which is proportional to the size of M_{10}, the output resistance $(=1/g_{m10})$, and the bias current of the buffer. In (1), since $g_{m10} \cdot r_{o10}$ is inversely proportional to the square-root function of the drain current, the drain current of M_{10} should be minimized for small r_{ob}. Fig. 2 shows the circuit schematic of the proposed LDO, where M_b and $M_{1\sim8}$ constitute the error amplifier and the buffer consists of $M_{9\sim13}$. In Fig. 2, the output resistance of the LDO, which is approximately equal to the output resistance of the PMOS pass transistor M_P, decreases with an increase in load current; therefore the dominant output pole frequency increases with the load current. Thus, to secure the LDO stability, the frequency of all the non-dominant poles should also be increased with an increase in load current and should be located at frequencies higher than the unity gain frequency. In Fig. 2, under no load condition, M_{12} is almost turned off, but with an increase in load current, the voltage at node N2 decreases. Thus, the increase in the current flowing through M_{12} leads to the increase in the current in M_{11} but no current change in M_{10}. The current increase in M_{11} leads to the increase in g_{m11} such that the output resistance of the buffer is reduced. By adopting the technique, the non-dominant pole at the output of the buffer can be shifted to frequencies much higher than the unity gain frequency. The remaining non-dominant pole located at the input of the buffer can be shifted to high frequency by adopting the current buffer compensation technique [1]. The adopted cascode-Miller frequency compensation technique splits the two poles, the dominant pole at the output of the LDO and the non-dominant pole at the input node (N1) of the buffer. For

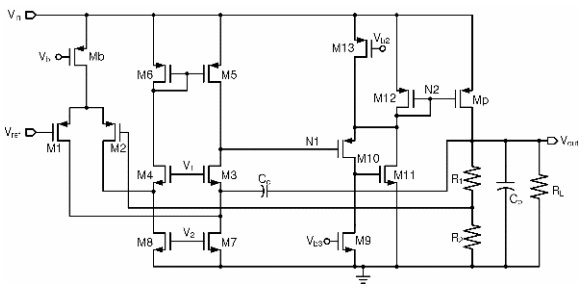

Fig. 2. Schematic of the newly proposed LDO.

sufficiently large value of compensation capacitor C_c, the non-dominant pole is pushed far beyond the unity gain frequency of the LDO feedback loop. If the input capacitance of the buffer is increased, the minimum value of C_c for a sufficient amount of phase margin should be increased as well, which reduces the unity gain bandwidth $(\omega_{GB,\max} = (B \cdot g_{m1})/C_c$, where $I_L \gg 0$ and $B(=R2/(R1+R2))$ is the feedback factor) of the LDO loop.

In order to minimize the maximum output voltage variation, both the unity gain bandwidth and the slew current should be maximized [2]. However, this could not be achieved in [1] due to the trade-off relation between the two. The slew current of the LDO with the reported buffer [1], shown in Fig. 1(c), is equal to the difference between the currents $I_{M10}+I_{Q11}$ and $I_{M12}+I_2$. The slew current of the buffer is not static but dynamic. Under the condition of regulated output voltage, the slew current stays at zero, but it increases when a step load current is applied. Then, the parasitic capacitance at node N2 is charged or discharged by the non-zero slew current. As the output voltage is regulated again, the slew current becomes zero. Since the maximum slew current is proportional to the initial slew current variation rate of the moment that the step load current is applied, in order to maximize the slew current, the initial slew current variation rate should be maximized. The initial slew current variation rate is given by

$$\begin{aligned} dI_{sl,init} &= d[I_{M12}+I_{M2}-(I_{M10}+I_{Q11})] \\ &= -d(I_{M10}+I_{Q11}) \\ &= g_{m10}dV_{N1}+\beta g_{m10}dV_{N1} \\ &= g_{m10}(1+\beta)dV_{N1}, \end{aligned} \tag{2}$$

where V_{N1} and β represents the node voltage at N1 and the current gain of Q_{11}, respectively. In (2), since the parasitic capacitance at node N2 is much larger than that of node N1, it is assumed that the initial variation rate of node voltage V_{N2} is very small so that the variation rate of I_{M12} and I_{M14} can be neglected. Of course, as the variation rate of V_{N2} increases gradually, the slew current variation rate becomes different from (2)

including the variation effects of I_{M12} and I_{M14}. Eq. (2) shows that large g_{m10} is required for high slew current. In addition, during the transition of full load to no load, the slew current is limited by the bias current flowing through M_{10}. However, large bias current increases the overdrive voltage of M_{10}, which is limited by the minimum drain-source voltages of M_3 and M_7. Thus, the W/L ratio of M_{10} should be increased for high g_{m10} to accommodate high bias current with small overdrive voltage at full load. However, increasing the W/L ratio of M_{10} leads to an increase in the input capacitance of the buffer, which reduces the unity gain bandwidth of the LDO loop as discussed. Therefore, in the LDO with the reported buffer in Fig. 1(c), both the loop bandwidth and the slew current cannot be increased simultaneously. For the LDO with the proposed buffer in Fig. 1(b), the slew current is given by the difference between the currents $I_{m10}+I_{m11}$ and I_2+I_{m12}. Since I_{M10} is fixed by the current source I_9, the slew current flows through M_{11}. Then, the initial variation rate of the slew current in the proposed buffer is given by

$$\begin{aligned} dI_{sl,init} &= d[I_2 + I_{M12} - (I_{M10} + I_{M11})] \\ &= -d(I_{M10} + I_{M11}) \\ &= g_{m10}dV_{N1} + g_{m11}dV_{gs11} \\ &= g_{m10}dV_{N1} + g_{m11}r_{o10}g_{m10}dV_{N1} \\ &= [g_{m10} + (g_{m10}r_{o10})g_{m11}]dV_{N1}. \end{aligned} \quad (3)$$

Eq. (3) shows that, to increase the slew current, g_{m11} should be maximized, which can be achieved by maximizing the drain current and/or the W/L ratio of M_{11}.

Note that, unlike the case of the buffer shown in Fig. 1(c), the W/L ratio of M_{11} can be increased without reducing the pole frequency at the input node of the buffer such that the unity gain bandwidth of the LDO loop is not degraded. Moreover, the W/L ratio of M_{10} can be minimized since the drain current of M_{10} is fixed with a small value of I_9, which reduces the value of C_c such that the unity gain bandwidth can be maximized. Therefore, the unity gain bandwidth and the slew current of the LDO can be increased independently by adopting the buffer shown in Fig. 1(b) since there is no trade-off involved between the two performance parameters. The effect of a pole at the gate of M_{11} on the LDO loop stability is discussed in the following subsection.

2. Stability Analysis

Fig. 2 shows the circuit schematic of the proposed LDO, where M_b and $M_{1\sim8}$ constitute the error amplifier and the buffer consists of $M_{9\sim13}$. When the buffer stage gain from N1 to N2 can be considered as unity for the frequency ranges of interest, the loop gain transfer function of the LDO is given by [1]

$$T(s) = \frac{-Bg_{m1}g_{mp}r_{oe}R_{oeq}}{(1+sR_{oeq}(C_o+g_{mp}r_{oe}C_c))(1+s\frac{C_{ib}C_or_{oe}}{C_o+g_{mp}r_{oe}C_c})}, \quad (4)$$

where R_{oeq} is the output resistance at node V_{out}. Then, by adopting the current buffer compensation technique, the LDO can achieve a single pole feedback loop. However, when the buffer is not designed properly, the LDO loop stability can not be guaranteed. In order to analyze the effect of the buffer loop stability on the LDO loop stability, the small signal model of the proposed buffer is shown in Fig. 3. The open loop gain of the buffer is given by

$$T_B(s) \approx \frac{g_{m10}g_{m11}(r_{o9}//r_{o10})}{(1+sC_{11}(r_{o9}//r_{o10}))\cdot((g_{m10}+g_{m12})+sC_p)}, \quad (5)$$

where C_{11}, and C_p are the input capacitance of M_{11}, and M_p, respectively, and r_{o9}, and r_{o10} the output resistance of M_9, and M_{10}, respectively. The closed loop gain of the buffer from N1 to N2 is given by

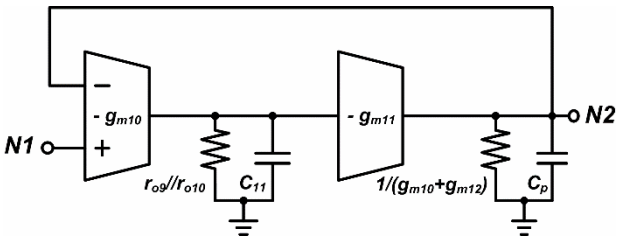

Fig. 3. Small signal model of the proposed buffer.

$$A_B(s) = \frac{N2}{N1} \tag{6}$$

$$\approx \frac{1}{1+s\frac{C_p+(g_{m10}+g_{m12})C_{11}(r_{o9}//r_{o10})}{g_{m10}g_{m11}(r_{o9}//r_{o10})}+s^2\frac{C_{11}C_p}{g_{m10}g_{m11}}} \tag{7}$$

$$= \frac{1}{1+\frac{s}{Q\omega_0}+\frac{s^2}{\omega_0^2}}$$

$$\omega_0 = \sqrt{\frac{(g_{m10}g_{m11})}{(C_{11}C_p)}} \quad and$$

$$Q = \frac{(r_{o9}//r_{o10})\sqrt{(g_{m10}g_{m11}C_{11}C_p)}}{(C_p+C_{11}g_{m12}(r_{o9}//r_{o10}))}. \tag{8}$$

In order for the capacitive loading at N2 to be neglected, design constraints are constructed as

$$Q < \frac{\omega_0}{\omega_{GB}} \quad where \quad \omega_{GB} = \frac{Bg_{m1}g_{mp}r_{oe}}{C_o+g_{mp}r_{oe}C_c} \tag{9}$$

$$PMD_{\omega_0} \approx arctan\left(\frac{\omega_{GB}}{Q\omega_0}\right) \quad where \quad \omega_0^2 \gg \omega_{GB}^2, \tag{10}$$

where PMD_{ω_0} is a phase margin degradation of an LDO loop affected by the natural frequency ω_0. When (9) does not hold, the LDO can oscillate due to a peaking even though enough phase margin is achieved. If a second pole of the LDO loop exists between ω_{GB} and ω_0, the constraint (9) can be relieved. Eq. (8) shows that ω_0 and Q are functions of a load current since g_{m11} and g_{m12} are proportional to g_{mp}. Thus, the design constraints can be approximately categorized into three regions depending on the transconductance g_{mp} of M_p as in Table 1 where $M = (W/L)_p/(W/L)_{12} \approx g_{mp}/g_{m12}$. From Table 1, in order for (9) to hold over the entire load conditions (region I, II, and III), C_{11} should be designed as

$$C_{11} < \frac{C_c}{Bg_{m1}(r_{o9}//r_{o10})}. \tag{11}$$

Table 1. Design constraints under different g_{mp}

Regions	I : $g_{mp} < \frac{C_o}{r_{oe}C_c}$	II : $\frac{C_o}{r_{oe}C_c} < g_{mp} < \frac{C_pM}{C_{11}(r_{o9}//r_{o10}))}$	III : $\frac{C_pM}{C_{11}(r_{o9}//r_{o10}))} < g_{mp}$
ω_{GB}	$\frac{Bg_{m1}g_{mp}r_{oe}}{C_o}$	$\frac{Bg_{m1}}{C_c}$	$\frac{Bg_{m1}}{C_c}$
ω_0	$\sqrt{\frac{g_{m10}g_{m11}}{C_{11}C_p}}$	$\sqrt{\frac{g_{m10}g_{m11}}{C_{11}C_p}}$	$\sqrt{\frac{g_{m10}g_{m11}}{C_{11}C_p}}$
Q	$\frac{(r_{o9}//r_{o10})\sqrt{(g_{m10}g_{m11}C_{11}C_p)}}{C_p}$	$\frac{(r_{o9}//r_{o10})\sqrt{(g_{m10}g_{m11}C_{11}C_p)}}{C_p}$	$\frac{\sqrt{(g_{m10}g_{m11}C_{11}C_p)}}{C_{11}g_{m12}}$
$Q < \frac{\omega_0}{\omega_{GB}}$	$\frac{Bg_{m1}g_{mp}r_{oe}}{C_o} < \frac{1}{(r_{o9}//r_{o10})C_{11}}$	$\frac{Bg_{m1}}{C_c} < \frac{1}{(r_{o9}//r_{o10})C_{11}}$	$\frac{Bg_{m1}}{C_c} < \frac{g_{m12}}{C_p}$
$tan(PMD_{\omega_0})$	$\frac{Bg_{m1}g_{mp}r_{oe}Cp}{g_{m10}g_{m11}(r_{o9}//r_{o10})C_o}$	$\frac{Bg_{m1}C_p}{C_c(r_{o9}//r_{o10})g_{m10}g_{m11}}$	$\frac{Bg_{m1}g_{m12}C_{11}}{C_cg_{m10}g_{m11}}$

Then, the maximum phase margin degradation, which should be as small as possible, can be derived by observing a tendency of $\tan(PMD_{\omega_0})$ under different g_{mp}. For region I, $\tan(PMD_{\omega_0})$ increases as g_{mp} increases since the dominant current, which affects g_{m11}, is provided from not M_{12} but M_{13} at light load conditions. On the other hand, $\tan(PMD_{\omega_0})$ decreases as g_{mp} increases for region II since g_{m11} is much more affected by the current from M_{12}. $\tan(PMD_{\omega_0})$ stays constant with the increase in g_{mp} for region III. Thus, the maximum PMD_{ω_0}, which occurs at $g_{mp} \approx C_o/(r_{oe}C_c)$, is given by

$$PMD_{\omega_0,max} \approx arctan\left(\frac{MNBg_{m1}r_{oe}Cp}{2g_{m10}(r_{o9}//r_{o10})C_o}\right), \tag{12}$$

where $N = \sqrt{(\mu_p(W/L)_{12})/(\mu_n(W/L)_{11})} \approx g_{m12}/(g_{m11|gmp\approx C_o/(r_{oe}C_c)})$. From (12), MN can be designed as

$$MN < tan\left(PMD_{\omega_0,max}\right) \cdot \frac{2g_{m10}(r_{o9}//r_{o10})C_o}{Bg_{m1}r_{oe}Cp}. \tag{13}$$

Considering (11) and (13), the LDO can be designed to be stable.

III. LDO DESIGN AND MEASUREMENT RESULTS

An LDO that adopts the proposed buffer shown in Fig. 1(b) is implemented in a 0.18-μm high voltage CMOS technology. The new LDO is designed for output voltage of 3.3 V, and the maximum load current of 200 mA with 0.2 V dropout voltage where $(W/L)_p = (28000\mu/0.3\mu)$. The value of the output capacitor is $1\ \mu$F. In Fig. 2, the single stage folded cascode error amplifier is designed to have a voltage gain greater than 50 dB over the entire load conditions as in [1]. To maximize the unity gain bandwidth of the LDO loop, the W/L ratio of M_{10} is chosen to be nearly minimum value (0.5 μ /0.3 μ), which reduces the required value of C_c (= 500 fF). Thus, with the chosen value of C_c, the proposed LDO

can maintain a phase margin larger than $70°$ over the entire load conditions shown in Fig. 4. Fig. 5 shows the simulated Bode plot of the loop-gain for the proposed LDO with a $1\,\mu$F output capacitor. The phase margin of the loop gain is about $90°$ under no load and full load conditions. Due to the small compensation capacitance of 500 fF, the maximum unity gain frequency of the proposed LDO is over 1 MHz, whereas it is approximately 40 kHz for the LDO reported in [1] with $C_c = 10$ pF [1]. Even though a peaking occurs near 10 MHz affected by ω_0 of the buffer under full load condition, the peaking does not exceed unity gain because (11) holds. Fig. 6 shows the PMD_{ω_0}, which is always smaller than $1.5°$ for the entire g_{mp}.

In Fig. 2, in order to accommodate high slew current under (11) and (13) hold, the W/L ratio of M_{11} is made large enough ($5\,\mu/0.35\,\mu$), which increases g_{m11} as well. The W/L ratio of M_{12} is made as large as possible ($102\,\mu/0.3\,\mu$) to support the high current of M_{11} with small V_{sg12}. A bias current from M_{13} is designed to be larger than that from M_9 so that current can flow through M_{11} under no load condition. The minimum and maximum quiescent currents under no (0 mA) and full (200 mA) loads are $7.63\,\mu$A and $924\,\mu$A, respectively, whereas the maximum quiescent current of the LDO reported in [1] is $340\,\mu$A under a full load of 200 mA. In the proposed LDO, most of the boosted currents flow through M_{11} increasing g_{m11} such that the system stays stable over the entire load conditions while maintaining high slew current. In other words, the increased quiescent current in the proposed LDO leads to the increase in slew current. Fig. 7 shows the chip microphotograph of the proposed LDO with a size of $211\,\mu$m x $297\,\mu$m. Fig. 8 and 9 show the simulated and measured load transient response of the proposed LDO

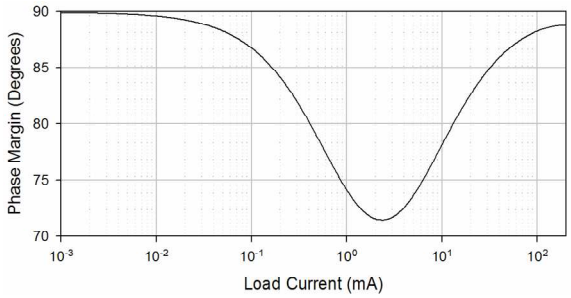

Fig. 4. Simulated phase margin of the LDO loop over the different load conditions with a $1\,\mu$F output capacitance.

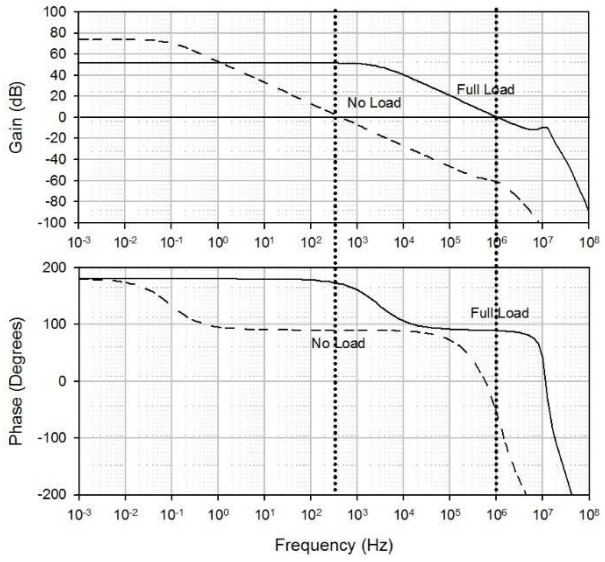

Fig. 5. Simulated Bode plot of the LDO loop-gain with a $1\,\mu$F output capacitance.

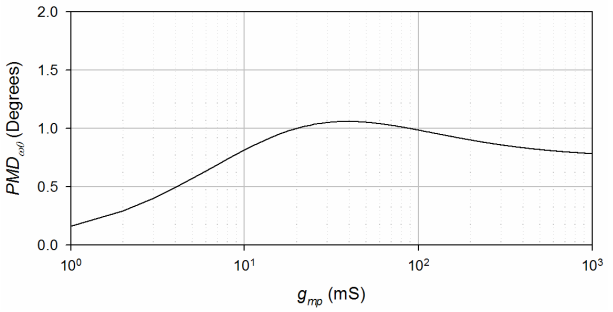

Fig. 6. Phase margin degradation affected by ω_0 under different g_{mp}.

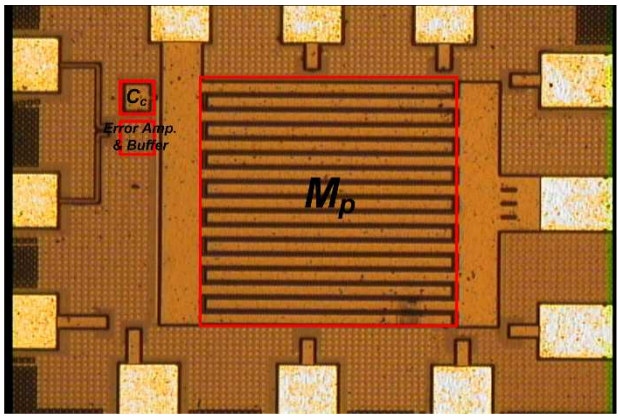

Fig. 7. Microphotograph of the proposed LDO.

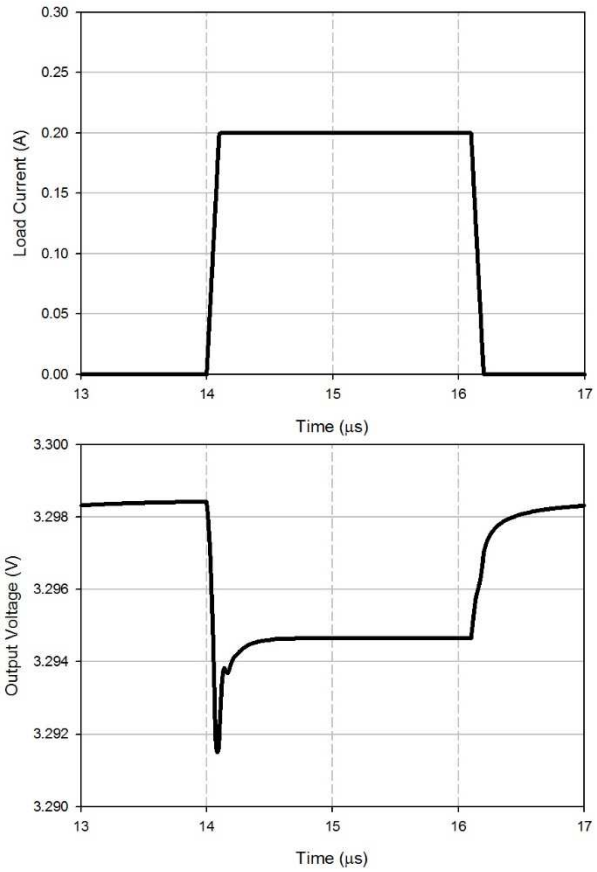

Fig. 8. Simulated load transient response of the proposed LDO for step load current changes of 0 mA to 200 mA with a rise and fall time of 100 ns and V_{OUT} =3.3 V.

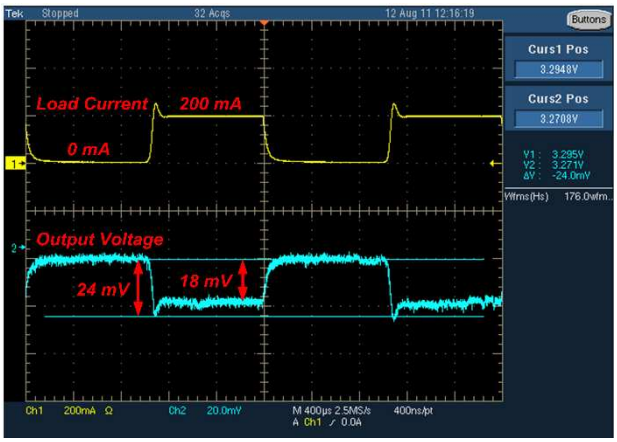

Fig. 9. Measured load transient response of the proposed LDO for step load current changes of 0 mA to 200 mA with a rise and fall time of 100 ns and V_{OUT} =3.3 V.

when the pulse load of 0 mA to 200 mA is applied with a rise and fall time of 100 ns, respectively. Fig. 8 shows the settling time is smaller than 1 μs. As can be seen from Fig. 9, the measured load regulation and the transient output voltage variation are 18 and 24 mV, respectively, which are larger than those of the simulated results due to the voltage drop across the bonding wire between the output pad and the PCB. However, the measured transient output voltage variation is much smaller than those of the LDO in [1] because both the slew current and the unity gain bandwidth of the proposed LDO are much higher than those of the LDO in [1]. The measured line regulation is less than 2 mV at the load current of 2 mA as shown in Fig. 10.

Table 2 summarizes the detailed performance of the proposed LDO, and Table 3 compares the key performance parameters of the proposed LDO with those of other reported LDOs including the figure of merit given by [3]

$$FOM = T_r \frac{I_q}{I_{L,max}} = \frac{C_o \cdot \Delta V_{OUT}}{I_{L,max}} \cdot \frac{I_q}{I_{L,max}} [ns], \quad (14)$$

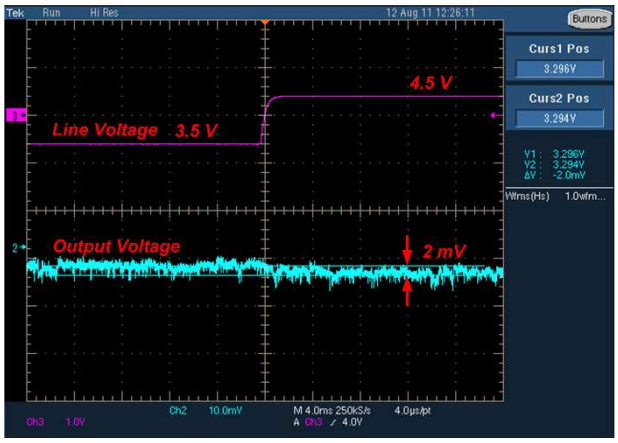

Fig. 10. Measured line transient response of the proposed LDO for step line voltage changes of 3.5 V to 4.5 V with I_L =2 mA.

Table 2. Performance summary of the proposed LDO

Input Voltage	3.5 - 4.5 V
Output Voltage	3.3 V
Dropout Voltage	0.2 V
Maximum Load Current	200 mA
I_q (no load)	7.5 μA
Output Capacitor	1 μF
Load Regulation (0-200 mA)	18 mV @ V_{IN} = 3.5 V
Line Regulation (3.5-4.5 V)	2 mV/V @ I_L = 2 mA
Transient Output Voltage Variation	24 mV
Die Area	0.063 mm^2
Technology	0.18- μm high voltage CMOS

Table 3. Performance comparison with previously reported LDOs

	2007 [1]	2008 [4]	2010 [5]	This Work
Technology (μm)	0.35	0.35	0.09	0.18
C_o (μF)	1	1	1	1
ESR Zero Required	No	No	Yes	No
V_{do} (V)	0.2	0.15	0.1	0.2
$I_{L,\max}$ (mA)	200	50	50	200
I_q (μA)	20	4	9.3	7.5
Current Efficiency (%) (@ Full Load)	99.8	99.67	N.A.	99.5
ΔV_{OUT} (mV)	54	6.6	10	24
T_r (μs)	0.27	0.132	0.2	0.12
Load Regulation (μV /mA)	170	61	82	90
Line Regulation (mV/V)	2	1	14	2
Die Area (mm^2)	0.264	0.053	0.00274	0.063
FOM (ns)	0.027	0.0106	0.0372	0.0045

where T_r is the response time of the LDO loop, I_q the quiescent current at no load condition, $I_{L,\max}$ the maximum load current, C_o the output capacitance, and ΔV_{OUT} the transient output voltage variation. As can be seen in Table 3, the proposed LDO achieves the best performance among the reported LDOs with the lowest value of FOM. Since the maximum quiescent current of the proposed LDO under full load is higher than that of the LDO in [1], the current efficiency at full load is degraded slightly. However, the current efficiency is still higher than 99 % and the proposed LDO is suitable for battery powered portable devices.

IV. CONCLUSIONS

In this paper, a low dropout regulator (LDO) based on a modified buffer impedance attenuation (BIA) technique to achieve fast transient response is proposed and implemented. By changing the path of the slew current, the proposed LDO overcomes the trade-off relation between the slew rate and the unity gain bandwidth of the reported LDO and achieves a high slew rate and large unity gain bandwidth simultaneously. Implemented in a 0.18-μm high voltage CMOS technology, the measurement results of the proposed LDO show an output voltage variation of just 24 mV for 200 mA load variation with a 1 μF output capacitance.

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