LETTER

Measured Results on Symmetric Dual-Level Spiral Inductors for RF ICs

Sang-Gug LEE[†a)], **So-Bong SHIN**[†], *and* **Gook-Ju IHM**[†], ***Nonmembers***

SUMMARY A completely symmetric dual-level spiral inductor structure is proposed. The symmetry, area efficiency, the size dependence of the coupling factor, and the quality factors of the dual-level inductors are evaluated and compared with that of the single-level. This work demonstrates that, with most RF applications, the dual-level inductors are the better choice than the single-level.

key words: *spiral inductors, symmetric, RF ICs, quality factor*

1. Introduction

The rising demand for the high quality monolithic inductors led to a significant progress in the silicon-based monolithic spiral inductor design techniques. Much of the effort has been given to the enhancement of the quality factors [1]–[4]. In spite of all the progresses that have been made, designers are reluctant to use the monolithic spiral inductors in the commercial RF ICs because of the large area needed.

At RF frequencies (0.3–3 GHz), the quality factors of the ordinary silicon based monolithic inductors are typically below 10, and often below 5. For many RF applications, such as the inter-stage or the output matching networks, inductive loads, etc., these inductors are acceptable. Yet for the applications such as the input side of the low noise amplifiers or the output stage of the power amplifiers, there is little hope that the conventional monolithic inductors would meet the level of the quality factors required. Therefore, in order to take advantage of the practical monolithic inductors, improving the area efficiency is important, and sometimes even more important than the quality factor.

2. Inductor Design

The concept of multi-level inductors has been originally introduced by Merrill [5], and Burghartz [6] reported more detailed characteristics of multi-level inductors and compared with the conventional single-level inductors. The idea of multi-level inductor is that while the single-level inductors use the lateral coupling of the adjacent metal lines to increase the inductance, the multi-level inductors use the vertical coupling as well by stacking inductors vertically. As reported in [5] and [6], if the coupling coefficient of the inter-level inductor is 1, the n-level inductors can provide n^2 times higher inductance than the conventional single-level inductors. The problem with dual-level inductors is that they tend to have high parasitic capacitances by the placement of the upper level metal on top of the lower level. This high parasitic capacitances lead to low resonance frequencies. Without a careful consideration for the parasitic capacitances, the advantages of the dual-level inductors can be seriously degraded by the low resonance frequency.

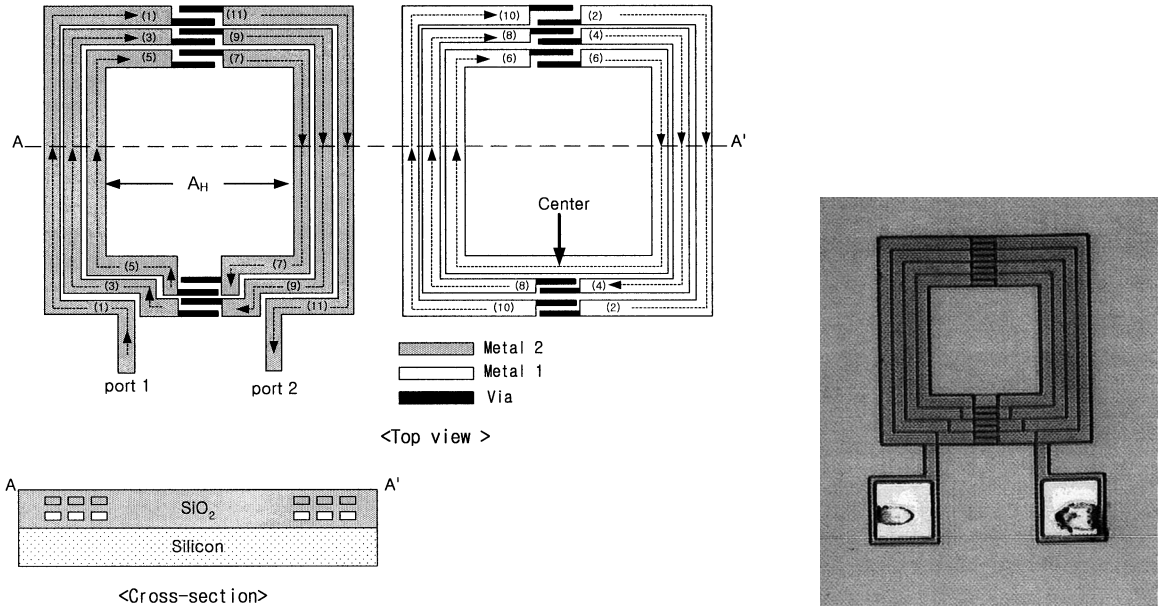
Figure 1 shows the layout of a 3-turn symmetric dual-level square spiral inductor proposed by this work. In Fig. 1(a), placing the upper-metal layer (shown on the left side) on top of the lower-metal layer (shown on the right side) completes the final inductor structure and the metal layers are connected through via. Figure 1(b) shows the microphotograph of the fabricated dual-level inductor. In Fig. 1, the dashed line indicates the signal flow. The alternation of the layers between the upper- and lower-metal leads to a perfectly symmetric inductor structure. The proposed symmetric inductor layout is simple and requires only double metal process. The multi-level inductors proposed by Merill [5] and Burghartz [6] are not symmetric. Generally, passive elements are expected to be symmetric and some RF designs require symmetric inductors [7].

The proposed symmetric inductor structure can be extended to higher (even) number of metal layers, e.g., 4-, 6-, 8-metal processes. For example, with 4-metal process, the layout of the upper two-layers (4th- and the 3rd-metal) would be the same as that of Fig. 1. Then, the layout of the bottom two-layers can be started at the "center" position (shown in Fig. 1) and be extended applying the same concept. The layout of the bottom two-layers will be going from the inner-side to the outer-side of the spiral.

Inductors are fabricated on a 4-metal 0.35-μm CMOS process. Figure 2 shows the cross-section of the metal layers and the oxides. In Fig. 2, the sheet resistance of the 4th-metal is 40 m$\Omega/\square$, and the rest are 80 m$\Omega/\square$, respectively. The dual-level inductors are fabricated for two different hollow areas (A_H), $50\times50\,\mu$m^2 and $100\times100\,\mu$m^2, and the number of turns cover 2 to 6. The metal line width of 10 μm and the

Manuscript received November 21, 2000.
Manuscript revised January 22, 2001.

[†]The authors are with Information and Communications University, P.O. Box 77, Yusong, Taejon 305-600, R.O. Korea.
a) E-mail: sglee@icu.ac.kr



(a) (b)

Fig. 1 A 3-turn symmetric dual-level inductor structure, (a) drawing, the dotted arrow represents the signal flow, (b) the microphotograph.

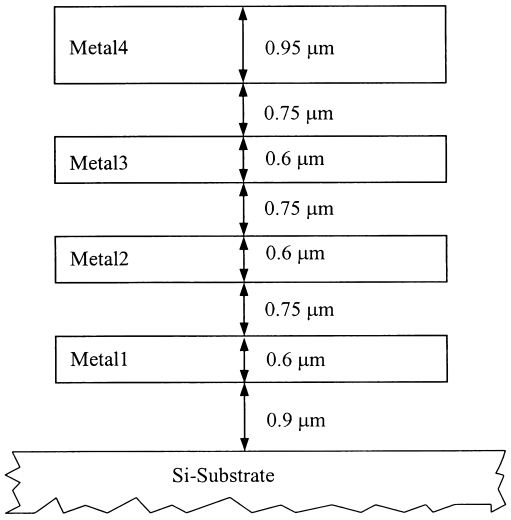


Fig. 2 The cross-section of the CMOS process showing the metal and oxide thickness.

spacing of 1 μm are used. Similarly, the corresponding single-level inductors are also fabricated for comparison. The single-level inductors used the 4th-metal, and with the dual-level, the 4th-metal is used for the upper-level and the 2nd- and 3rd-metal-in-parallel are used as the lower-level spiral. The 2nd- and 3rd-metal are connected through multiple via. Parallel combination of 2nd- and 3rd-metal makes the upper- and lower-level spirals of the dual-level inductors to have approximately same resistivity.

3. Measurement Results and Discussions

Inductors are laid out for two-port measurement. From Fig. 1(b), a rectangular ground metal-plate is placed 150 μm away from the inductor pad, horizontally. The two-port S-parameters are measured on-wafer using the microwave probes (GS and SG type) and the network analyzer.

Table 1 summarizes the inductor size, the inductance, and the resonant frequencies of the fabricated inductors. In Table 1, the inductance of the dual-level are 3–4 times higher than that of the single-level structures of the same size. This is not in agreement with the expectations that the dual-level will provide 4 times higher inductances. Figure 3 shows the normalized multiplication factors (multiplication factor/4) as a function of the number of turns. As can be seen from Fig. 3, it appears that the inter-level mutual-coupling coefficients of the dual-level inductors are less than 1 for small number of turns, and linearly increase with increase in number of turns. If we assume the upper- and lower-level inductors generate the same amount of inductance as the corresponding single-level inductors, the mutual coupling coefficient between the upper- and lower-level inductor of the 2-turn inductor, shown in Fig. 3, is about 0.6. The coupling coefficients approach the expected value of 1 for higher than 5 turn inductors. Note that the coupling coefficients show only the dependence on the number of turns but not on the inner-diameter (A_H).

Figure 4 shows the quality (Q) factors of the fab-

Table 1 List of inductances and the resonant frequencies of the single- and dual-level inductors fabricated.

Levels	A_H(μm)	# of turns	Inductance (nH)	Resonance Freq (GHz)
single	50	2	0.56	
		3	1.11	
		4	1.9	
		5	3.1	14
		6	4.7	10
	100	2	1.07	
		3	2.1	18
		4	3.65	12
		5	5.63	8.5
		6	8.55	6
dual	50	2	1.7	12
		3	3.7	6
		4	7.16	3.5
		5	12.26	2.3
		6	18.4	1.5
	100	2	3.6	
		3	7.2	3
		4	13.56	1.95
		5	22.04	1.4
		6	34.22	0.9

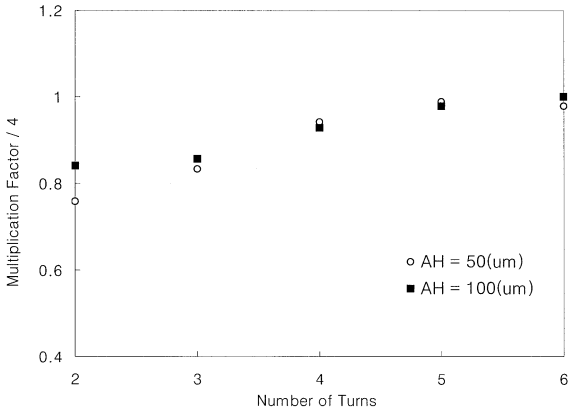


Fig. 3 The normalized multiplication factors of the dual-level inductors as a function of the number of turns. The multiplication factors are calculated by taking the ratio of the inductances of the same number of turn inductors (L_{dual}/L_{single}).

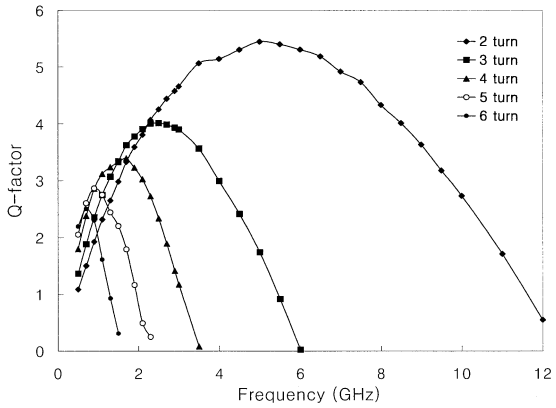


Fig. 4 The quality factor of the dual-level inductors as a function of frequency for various numbers of turns. $A_H = 50\,\mu$m.

ricated dual-level inductors for $A_H = 50\,\mu$m. The Q-factors are obtained with the commonly used method [3]–[5] based on $[-\mathrm{Im}(y_{11})/\mathrm{Re}(y_{11})]$ of the measured data. As can be seen in Fig. 4, the increase in the number of turns lead to a fast reduction in resonance frequency and, consequently, the quality factor. Therefore, one might be tempted with a hasty conclusion that the high parasitic capacitances make the dual-level inductors useless. However, note the inductor sizes of the dual-level inductors (see Table 1). With most RF ICs operating 1 to 3 GHz ranges, the inductor values needed are typically below 10 nH [8]. In fact, the majority of the inductors used in RF IC designs are below 5 nH, especially near or above 2 GHz. The data shown in Table 1, tells us that the dual-level inductors of up to 10 nH can be obtained with resonance frequencies higher that 3 GHz. Also, note that the inductors fabricated in this work used the upper three metal layers (2nd through 4th-metals). Had the 4th-metal combined with 2nd- or 1st-metal as the lower-level inductor, the resonance frequency could have been extended to higher frequencies.

Considering the sizes of the inductors listed in Table 1, one can assess that, for most RF applications, the on-chip inductors could be incorporated with the size comparable to bond-pad (typically $100 \times 100\,\mu\mathrm{m}^2$). Based on [9] and assuming the inter-level coupling coefficient of 1, it can be shown that the dual-level inductor that uses 5 μm width and 1 μm spacing can provide inductance greater than 11 nH within the size of $100 \times 100\,\mu\mathrm{m}^2$. RF IC designers are usually not afraid of utilizing capacitors extensively, often greater than the bond-pad size.

The Q-factors of the single- and dual-level inductors are compared. Though the specific data are not provided, overall, measurements show that the Q-

factors of the dual-level are approximately the same or slightly better than that of the single-level inductors over the RF frequencies, for the similar values of inductances.

The symmetry of the dual-level inductors are also evaluated. The dual-level showed nearly perfect symmetry over the frequency. The dual-level showed high impedance at resonance (600–900 Ω). The low resonance frequency and high peak impedance of the dual-level inductors suggest other possible application, the RF choke. RF choke is one of the frequently requested components in RF IC design.

4. Conclusion

A novel symmetric dual-level spiral inductor structure is proposed and the RF characteristics of the dual-level inductors are compared to that of the single-level inductors. This work demonstrates that the inter-level coupling coefficient of the dual-level inductors are less than 1 at low number of turns, and approaches to 1 at higher than 5-turn inductors. The quality factors of the dual- and single-level are compared through the measurements. This work shows that, with typical RF ICs of 1 to 3 GHz applications, where the required inductances are typically below 10 nH, the dual-level structures have advantages in area efficiency and quality factor. The dual-layer structure is also proposed as a candidate for the high impedance choke at radio frequencies.

Acknowledgements

This work is supported by the Ministry of Information and Communications, Korea, Grant #99-S-016.

References

[1] M. Danesh, J.R. Long, R. A, Hadaway, and D.L. Harame, "A Q-factor enhancement technique for MMIC inductors," IEEE RFIC Symp., pp.217–220, 1998.
[2] J.R. Long and M.A. Copeland, "The modeling, characterization, and design of monolithic inductors for silicon RF IC's," IEEE J. Solid-State Circuits, vol.32, no.3, pp.357–369, March 1997.
[3] J.N. Burghartz, M. Soyuer, and K.A. Jenkins, "Integrated RF and microwave components in BiCMOS technology," IEEE Trans. Electron Devices, vol.43, no.9, pp.1559–1570, Sept. 1996.
[4] K.B. Ashby, I.A. Koullias, W.C. Finley, J.J. Bastek, and S. Moinian, "High Q inductors for wireless applications in a complementary silicon bipolar process," IEEE J. Solid-State Circuits, vol.31, no.1, pp.4–9, Jan. 1996.
[5] R.B. Merrill, T.W. Lee, H. You, R. Rasmussen, and L.A. Moberly, "Optimization of high-Q integrated inductors for multilevel metal CMOS," IEDM Tech Dig., pp.983–986, 1995.
[6] J.N. Burghartz, K.A. Jenkins, and M. Soyuer, "Multilevel-spiral inductor using VLSI interconnect technology," IEEE Electron Device Lett., vol.17, no.9, pp.428–430, Sept. 1996.
[7] J. Craninckx, M. Steyaert, and H. Miyakawa, "A fully integrated spiral-LC CMOS VCO set with prescaler for GSM and DCS-1800 systems," IEEE CICC, pp.403–406, 1997.
[8] T.H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge, United Kingdom, 1998.
[9] S.S. Mohan, M. Hershenson, S.P. Boyd, and T.H. Lee, "Simple accurate expressions for planar spiral inductances," IEEE J. Solid-State Circuits, vol.34, no.10, Oct. 1999.