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LETTER

Low Voltage Current-Reused Pseudo-Differential Programmable Gain Amplifier

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SUMMARY This paper reports a current-reused pseudo-differential (CRPD) programmable gain amplifier (PGA) that demonstrates small size, low power, wide band, low noise, and high linearity operation with 4 control bits. Implemented in 0.18um CMOS technology, the PGA shows the gain range from −9.9 to 8.3 dB with gain error of less than ±0.38 dB. The IIP3, P1 dB, and smallest 3-dB bandwidth are 10.5 to 27 dBm, −9 to 9.5 dBm, and 250 MHz, respectively. The PGA occupies the chip area of 0.04 mm^2 and consumes only 460 μA from a 1.2 V supply.

key words: *variable gain amplifier (VGA), programmable gain amplifier (PGA), low power amplifier, analog circuit*

1. Introduction

Lately, the growing demands of portable electronic equipments and system-on-chip have been pushing circuit designs to low voltage and low power consumption [1], [2]. The programmable gain amplifier (PGA) is an important building block in many applications to accommodate the large dynamic range of signals, for example in wireless communication systems. Realizing a wideband PGA with low power consumption while maintaining high linearity and low noise is a challenge, especially in modern deep submicron CMOS technology where the supply voltage can be as low as 1.2 V. In this letter, a new low voltage, low power, and high performance PGA that adopts a current-reused pseudo-differential pair is presented. The reconfiguration technique is also introduced to realize a 50% saving in chip area.

2. Proposed Idea

Nguyen et al. [3] reported a PGA cell following the pseudo-exponential approximation function $e^{2t} \approx (1+t)/(1-t)$ by simultaneously changing the transistor size and bias currents of the input and diode-connected load transistors of the differential amplifier. Thus the PGA cell in [3] can provide a dB-linear gain range of 20 dB with less than ±0.25 dB gain error. However, for the low voltage and large signal swing requirements, pseudo-differential amplifiers are more attractive since the voltage drop across the tail current source can be eliminated [1].

Applying the same gain control scheme of the PGA cell introduced in [3] but removing the current tail and adopting current-reused architecture, the newly proposed PGA is shown in Fig. 1. As can be seen in Fig. 1, the input-G_m stage and diode-connected load consist of the same size transistors so that the two circuits can be directly coupled. The input and output voltage levels depend on the size ratio of the PMOS and NMOS transistor pairs. The feedback resistor R_f in the input-G_m stage is large enough to minimize the loading effect at the output nodes.

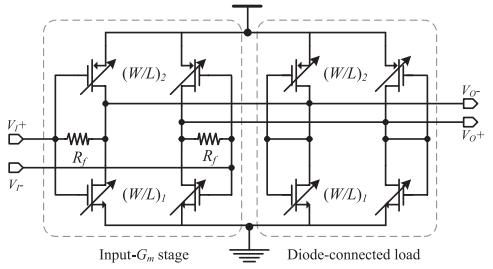

Fig. 1 The current-reused-pseudo differential-pair based PGA architecture.

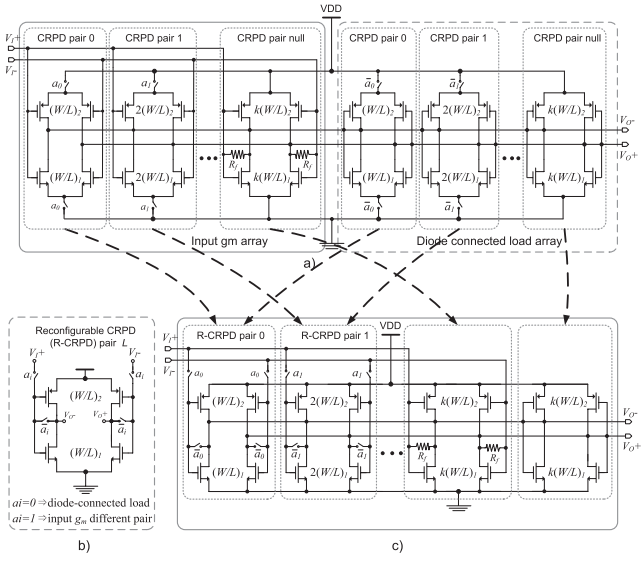

Fig. 2 a) The proposed PGA with separated input-G_m and load CRPD pairs. b) Schematic of configurable-CRPD pair. c) The proposed PGA schematic based on reconfigurable-CRPD pair.

Figure 2(a) shows the full circuit of the PGA where the input-G_m and diode-connected load array contains CRPD pairs with the size factors in the form of a geometric sequence. Similar to the gain control scheme introduced in [3], the transconductance of the input-G_m and diode-connected

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load array can be varied by switching ON or OFF the CRPD pairs. For example, when the control word $a_3a_2a_1a_0$ is set to 0000, all CRPD pairs in the input-G_m array turn OFF except the null pair, while all CRPD pairs in diode-connected load array turn ON, including the null pair, leading to the smallest value of input transconductance and load resistance. Thus the lowest level of voltage gain is achieved. When the control word $a_3a_2a_1a_0$ is changed to 0001, in the input-G_m array, the CRPD pair 0 and CRPD pair null turn ON, while in the diode-connected load array, the CRPD pair 0 turns OFF. Thus the input transconductance and load resistance increases slightly, leading to one step increasing of the voltage gain, and so on ... Note that, in Fig. 2(a), neither of the two i-th CRPD pairs in the input-G_m and diode-connected load array turns ON or OFF at the same time, while the two null pairs are always ON. Therefore, each i-th input-G_m and load CRPD pairs can be combined into one reconfigurable-CRPD pair as shown in Fig. 2(b) to save the chip area nearly 50%. In Fig. 2(b), the reconfigurable-CRPD pair i can be used as an input-G_m stage ($a_i = 1$) or diode-connected load ($a_i = 0$) depending on the states of switches a_i. Figure 2(c) shows the final circuit schematic of the proposed 4-bit PGA based on the reconfigurable-CRPD pairs, which occupies approximately half the amount of chip area compared to that of the original PGA shown in Fig. 2(a).

The CRPD pairs in Fig. 2(c) are designed so that the transconductance of the PMOS transistor pair would be equal to that of the NMOS transistor pair. Therefore, the transconductance of CRPD pairs are two times that of the NMOS transistor pairs. The bias current of each CRPD pair is directly proportional to the size factor. The total sizes, and therefore the bias currents, of the NMOS transistors in the input-G_m and diode-connected CRPD stages as a function of control bits can be given by

$$(W/L)_{Ninput} = (W/L)_1(2^0a_0 + 2^1a_1 + 2^2a_2 + \ldots + 2^{n-1}a_{n-1} + k) \quad (1)$$

$$(W/L)_{Nload} = (W/L)_1(2^0\overline{a_0} + 2^1\overline{a_1} + 2^2\overline{a_2} + \ldots + 2^{n-1}\overline{a_{n-1}} + k) \quad (2)$$

$$I_{input} = I_0(2^0a_0 + 2^1a_1 + 2^2a_2 + \ldots + 2^{n-1}a_{n-1} + k) \quad (3)$$

$$I_{load} = I_0(2^0\overline{a_0} + 2^1\overline{a_1} + 2^2\overline{a_2} + \ldots + 2^{n-1}\overline{a_{n-1}} + k) \quad (4)$$

where $(W/L)_1$ and I_0 are the size and bias current of the smallest NMOS pair, respectively, a_i the digital control bit, n the number of control bit, and k the constant for adjusting the gain range of the PGA. From (1) to (4), the differential voltage gain of the proposed PGA cell can be given by

$$A_V = \frac{g_{m-input}}{g_{m-load}} = \frac{2\sqrt{(W/L)_{Ninput}I_{input}}}{2\sqrt{(W/L)_{Nload}I_{load}}} = \frac{(k+x)}{(k+2^n-1-x)} \quad (5)$$

where $x = 2^0a_0 + 2^1a_1 + 2^2a_2 + \ldots + 2^{n-1}a_{n-1}$. From (5), by defining $t = [x-2^{n-1}-1/2]/[k+2^{n-1}-1/2]$, the voltage gain follows the pseudo-exponential function $e^{2t} \approx (1+t)/(1-t)$. Therefore, the PGA cell can cover the dB-linear gain range of 20 dB with a gain error of less than ±0.25 dB [3].

As mentioned before, one of the key advantages of the proposed PGA cell by adopting the pseudo-differential pair is low voltage operation. The theoretical minimum supply voltage is $VDD_{min} = V_{THn} + V_{THp}$ where $V_{THn,p}$ are the threshold voltage of NMOS/PMOS transistors. For example, with $V_{THn} = V_{THp} = 0.5$ V, the minimum supply voltage can be 1 V. The output signal swing of the PGA is limited by the saturation mode requirement of the input-G_m stage transistors since one transistor (NMOS or PMOS) in each branch of the diode-connected load is always in saturation mode regardless of the instant output node voltage. Another advantage of the proposed complimentary pseudo-differential pair based PGA is simplicity. By avoiding the need of extra circuitry for common mode feedback and bias, noise and parasitic capacitance at the output node can be reduced. Moreover, due to the current-reused complimentary architecture, the transconductance of the input transistor and diode-connected load are doubled; the output impedance is reduced by half, leading to the same gain but better linearity and wider bandwidth compared to the non-complimentary pseudo-differential architecture.

Main disadvantages of pseudo-differential architecture are common mode signal behavior and supply noises that degrade performance of the amplifiers. Common mode feedforward [4] and low drop out dc-dc converter circuits are normally used to suppress common mode signals and to reduce supply noises, respectively. However, the circuits are not covered in this design.

3. Measurement Results

The proposed PGA is fabricated in 0.18-μm CMOS technology. The micro-photograph of the proposed PGA is shown in Fig. 3. The PGA chip occupies 0.04-mm^2 excluding bonding pads and dissipates current of 460uA from 1.2 V supply. Figure 4 shows the measured gain and gain

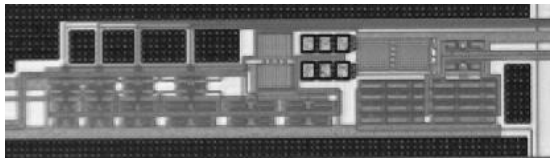

Fig. 3 Microphotograph of the proposed PGA chip.

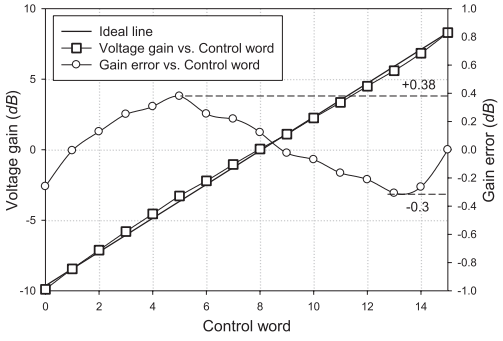

Fig. 4 Measured gain and gain-error versus control word.

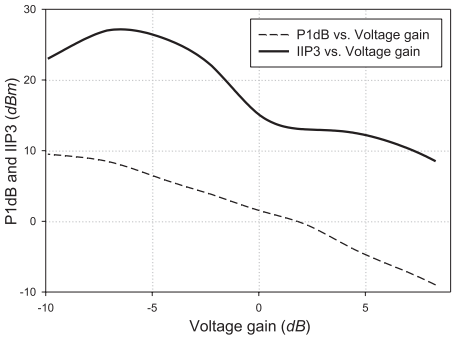

Fig. 5 Measured input P1 dB and IIP3 of the proposed PGA.

Table 1 Performance summary and comparison.

Parameter	Proposed PGA	[1]	[2]	Units
Technology	***0.18-μm CMOS***	0.18-μm CMOS	0.13-μm CMOS	
Power/supply voltage	***0.55/1.2***	16.6/1.8	0.05/1	mW/ V
Gain range	***-9.9 ÷ 8.3***	0 ÷ 12	-10 ÷ 30	dB
Gain step	***1.21***	6	2	dB
Gain error	***<±0.38***	-	-	dB
-3dB bandwidth	***250***	1400	130	MHz
P1dB	***-9 ÷ 9.5***	-	-	dBm
IIP3	***8.5 ÷ 27***	-	-20.5 ÷ 4.9	dBm
Noise Figure	***10***	12.4	-	dB
Die area	***0.1x0.4***	-	-	mm^2

error versus digital control word at 100 MHz. As can be seen in Fig. 4, the proposed PGA shows the dB-linear gain range of 18.2 dB from −9.9 to 8.3 dB with gain error less than ±0.38 dB. The measured IIP3 and P1 dB are 10.5 to 27 dBm and −9 to 9.5 dBm, respectively, as shown in Fig. 5. The measured 3-dB bandwidth at the voltage gain of 8.3 dB is 250 MHz. The 3-dB bandwidth of the PGA depends on parasitic capacitance at the output node and load resistance. At lower gain levels, the parasitic capacitance at the output nodes is kept the same, while load resistance is reduced, leading to larger 3-dB bandwidths. The PGA shows the noise figure (NF) of less than 10 dB at the maximum gain of 8.3 dB. The performance of the proposed PGA is compared with [1] and [2], which is shown in Table 1.

4. Conclusions

This letter reported a compact 4-bit programmable gain amplifier based on current-reused pseudo-differential pair to satisfy the presently increasing demand for small size, low power, and low voltage requirements. By switching the size of the pseudo differential transistor pair, the pseudo-exponential function $e^{2x} \approx (1 + x)/(1 - x)$ is implemented to achieve a wide dB-linear range while maintaining good linearity; and by adopting the reconfiguration of the current reused pseudo differential pair, the proposed PGA save 50% in the chip area.

Acknowledgments

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