LETTER

Yield-Ensuring DAC-Embedded Opamp Design Based on Accurate Behavioral Model Development

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SUMMARY An accurate behavioral model of a DAC-embedded opamp (DAC-opamp) is developed for a yield-ensuring LCD column driver design. A lookup table for the *V-I* curve of the unit differential pair in the DAC-opamp is extracted from a circuit simulation and is later manipulated through a random error insertion. Virtual ground assumption simplifies the output voltage estimation algorithm. The developed behavioral model of a 5-bit DAC-opamp shows good agreement with the circuit level simulation with less than 5% INL difference.

key words: *DAC, DAC-embedded, behavioral model, yield*

1. Introduction

Among the many digital-to-analog converter (DAC) architectures, one with a DAC-embedded opamp (DAC-opamp) has been a good choice for a size-efficient LCD column driver [1], [2]. Figure 1 shows a DAC architecture employing an L-bit DAC-opamp along with an M-bit R-string DAC (RDAC). The input differential pair (DP) of the DAC-opamp is composed of identical 2^L ($=n$) unit DPs. The DAC-opamp linearly interpolates V_H and V_L, which are the outputs of the coarse DAC, according to its input code. In a real circuit, however, the resolution of the DAC-opamp is limited by the interpolation nonlinearity caused by the transconductance (g_m) nonlinearity of the differential pair and the random mismatches between unit DPs, such as offset and tail current mismatch. As a result, the performance of the DAC-opamp reduces as the resolution increases. Because of random errors combined with circuit nonlinearity, it is difficult to estimate the statistical performance, i.e., the yield, with a simple mathematical model. Monte-Carlo circuit simulation might be considerable, but it usually takes too much time to be used in every design step. With this in mind, a yield-assuring design methodology for a DAC-opamp based on behavioral model development is proposed in this letter.

2. Behavioral Model Development

In this letter, we present several ideas to develop a simple, circuit-simulator-level accurate DAC-opamp model.

A) Output voltage calculation: Output voltage of the DAC-opamp can be calculated simply if the loop gain is high enough, which is true especially when the current consumption is very small, as in LCD column drivers. Since the DAC-opamp is in a negative feedback loop, its two drain currents of the first stage become almost the same ($\Sigma I_O^+ = \Sigma I_O^-$ in Fig. 1) owing to the virtual ground. This is depicted in Eq. (1).

$$\sum I_O^+ - \sum I_O^- = \sum_{k=1}^{n} \Delta I_{O,k}(V_{id,k}) \approx 0 \tag{1}$$

where $\Delta I_{O,k}(V_{id,k}) = I_{O,k}^+(V_{id,k}) - I_{O,k}^-(V_{id,k})$, $I_{O,k}^+$ and $I_{O,k}^-$ are output currents, and $V_{id,k} = (V_{in,k} - V_O)$ of the k-th unit differential pair (DP_k) shown in Fig. 1. Thus, the best estimation of V_O can be found by using only the first stage of the DAC-opamp (2^L unit DPs). By sweeping one input terminal, which is supposed to be connected to V_O from V_L to V_H with a finite step while the other inputs are connected to V_L or V_H according to the input code, we can choose the input value that gives the closest result to (1) as a best estimation of V_O.

B) V-I curve description: The accuracy of the estimated V_O from the above algorithm strongly depends on how accurately the *V-I* curve of DP, $\Delta I_O(V_{id})$, is described. The MOS square law could be the simplest choice, but it is not enough to achieve circuit simulator level accuracy. In this work, $\Delta I_O(V_{id})$ of a random-error-free unit DP is obtained from a real circuit simulation in the form of a lookup table (LUT). Note that this completely reflects the real circuit behavior including its nonlinearity. For this, the candidate unit DP should first be created in the circuit level. Then, the LUT of the unit DP's *V-I* curve is extracted using circuit simulation by sweeping one input from V_L to V_H while the other one is fixed to V_L.

C) Random error insertion: The last concern in this model generation is how to implement the random error effects in a random-error-free LUT. Figure 2(a) shows the DP's *V-I* curve change by the input pair offset and the tail current error. When offset (V_{OS}) exists, the *V-I* curve shifts by that amount on the V_{id} axis. The LUT can reflect it by shifting the output current data by $-V_{OS}$ in the V_{id} column as shown in Fig. 2(b). In contrast, the tail current error scales the maximum output current from I_{ss} to $(1 + \alpha)I_{ss}$, where α is the fractional error amount of the tail current. This is also depicted in Fig. 2(b). Even if the real current scaling does not occur linearly along the V_{id} axis, it is a reasonable approximation, as will be proved later, because current sources in strong inversion can easily be designed accurately.

It is well known that the differential pair offset voltage and current source mismatch are estimated by Eqs. (2) and

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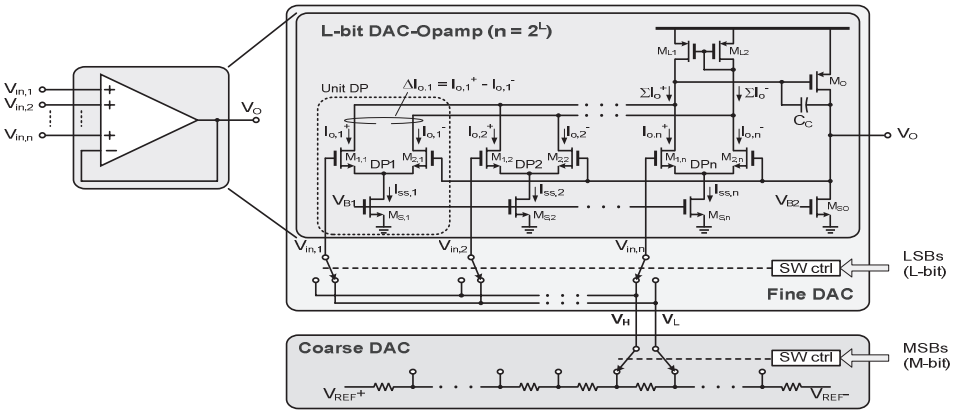
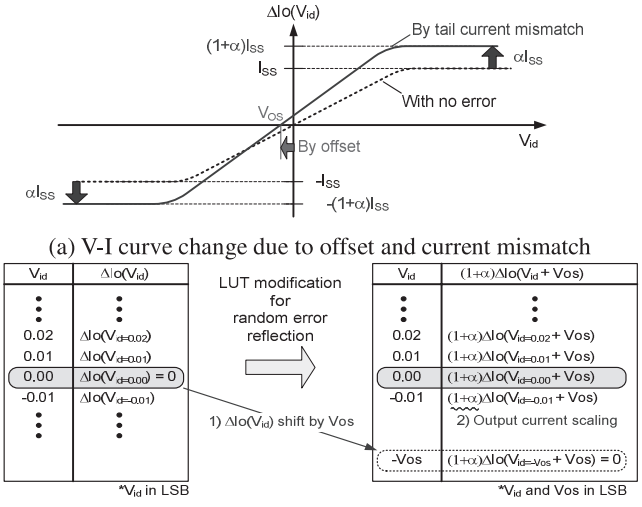


Fig. 1 Schematic of a DAC with a DAC-opamp and RDAC.



(a) V-I curve change due to offset and current mismatch

(b) LUT modification to reflect (a)

Fig. 2 LUT generation and its modification for random error reflection.

(3) based on A_{VT}, A_β, transistor size (WL), and overdrive voltage ($V_{GS} - V_T$) [3].

$$\sigma^2(V_{OS}) = \frac{1}{WL}\left(A_{VT}^2 + \frac{A_\beta^2(V_{GS}-V_T)^2}{4}\right) \quad (2)$$

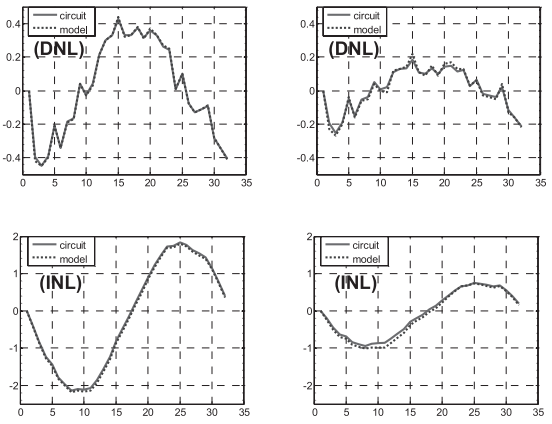
$$\sigma^2\left(\frac{\Delta I}{I}\right) = \frac{1}{WL}\left(A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS}-V_T)^2}\right) \quad (3)$$

Thus, random error generation for yield estimation is easy and reliable. Note that the non-idealities from the second stage of the opamp are ignorable owing to the large DC gain of the first stage. Also, the mismatch of the active load (M_{L1} and M_{L2} in Fig. 1) does not degrade the linearity of the DAC-opamp even though it is desirable to design it with a low transconductance in order to reduce the column-to-column mismatch of LCD panels.

3. Model Verification and Conclusions

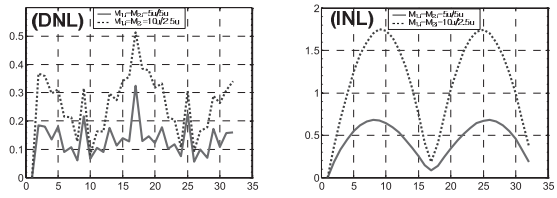
To verify the accuracy of the proposed modeling method, a behavioral model of 5-bit DAC-opamp has been developed for an 18 V 0.35 μm CMOS process. It is based on the LUTs of 32 unit DPs with a 5-bit coarse RDAC for 10-bit resolution. By applying 17 V for V_{REF}+ and 9 V for V_{REF}- for the upper side driver, full scale input of the DAC-opamp ($V_H - V_L$) is decided as 256 mV and, thus, the 1 LSB level of the DAC-opamp is 8 mV. In this work, the input step size of 80 μV has been used for sufficient accuracy. For the model generation, a case with V_L = 9 V and V_H = 9.256 V were used since this gives the worst DAC linearity due to the highest g_m condition. As V_L increases as the MSBs in RDAC do, the linearity of the DP enhances owing to the reduced g_m by the increased body effect. Note that the offset variation according to the input common level (or V_L) change should be negligible. Such behavior can be understood by the offset estimating Eq. (2). As long as the tail current does not change, V_{GS}-V_T is constant no matter how V_T changes, and thus the offset does not change. Our Monte-Carlo simulation also proved that by showing only 4% change of the standard deviation of the offset while V_L is swept from $0.5V_{DD}$ to $0.9V_{DD}$, where V_{DD} is the supply voltage. If the DAC-opamp is linear enough, the total transfer curve of the 10b DAC will follow that of RDAC. Since the linearity of RDAC is not a concern here, we focus only on the linearity of the DAC-opamp in a segment of RDAC. With these backgrounds discussed thus far, we have concluded that the first interpolating point (V_L = 9 V and V_H = 9.256 V) is the worst case in the point of linearity. A V_{DS} change of the tail current source ($M_{S,k}$) by the changed V_L is not a problem either for the same reason. It is assumed that the input voltage change from V_L to V_H makes an ignorable change in the tail current.

A circuit level DAC-opamp has been designed for accuracy comparison. 32 unit DPs draw a 4 μA ($I_{ss,k}$ = 125 nA) total current, and the 2nd stage draws a 5 μA current. The first DP candidate has 10 μ/2.5 μ input transistors ($M_{1,i}$, $M_{2,i}$). The sizes of the other transistors in Fig. 1 are as follows: M_L = 40 μ/4 μ, C_C = 400 fF, Mo = 20 μ/1.8 μ, Mso = 15 μ/4 μ, and Ms = 1 μ/10 μ. The open-loop DC gain of the designed DAC-opamp is 90 dB and the loop bandwidth is 1 MHz. A clock period of 16 μs has been used for the SPEC-



(a) Input transistor = 10μ/2.5μ b) Input transistor = 5μ/5μ

Fig. 3 DNL and INL comparison: circuit vs. model.



(a) RMS DNL (b) RMS INL

Fig. 4 Expected RMS values of DNL and INL from 1000 samples.

TRE transient simulation. From the process information, the standard deviation of the differential pair offset and the tail current mismatch were estimated as 20 mV and 5%, respectively. Note that random offsets and current mismatches for 32 unit DPs have been generated based on those values and are used for the yield test with the developed model. The offset voltage in each DP, $V_{os,i}$, was truncated with $80\,\mu$V steps.

Simulation has been done using the candidate circuit and model of the DAC-opamp. Figure 3(a) shows the DNL and INL from both the circuit level transient simulation and proposed MATLAB model simulation with the same errors. Note that the behavioral model gives almost the same results as the circuit simulation with less than a 5% difference. Since the INL is not enough, in order to increase the linearity, and also to further verify the model accuracy, the design has been modified with $M_{1,i} = M_{2,i} = 5\,\mu/5\,\mu$. Figure 3(b) shows the results. Again, they are almost the same, proving further that a smaller g_m of the input transistor provides better linearity as expected. Since the accuracy of the developed model has been proven, it can now be used for yield estimation. Figure 4 shows the RMS value of the DNL and INL of the two designs discussed above after 1000-time simulations. From the result, it is expected that the designed 5-bit DAC-opamp satisfies ±1.8 LSB and ±0.7 LSB INL with a yield of 68% for input transistor sizes of $10\,\mu/2.5\,\mu$ and $5\,\mu/5\,\mu$, respectively.

In this letter, a simple and accurate behavioral model of a DAC-opamp has been presented. Based on the proven accuracy, it can be used as an efficient tool for a yield-guaranteed DAC-opamp design.

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