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BRIEF PAPER

A Low Power Driver Amplifier for Unlicensed 2.4 GHz Band

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SUMMARY This paper presents the design of a driver amplifier (DA) for a cordless mouse application, operating at the 2.4 GHz ISM unlicensed band. The DA is a single-ended topology, and is composed of two stages: the first stage is a cascode amplifier to provide high gain and good input-output isolation, while the output stage is a simple common source amplifier that adopts a novel current reuse scheme to reduce the DC bias current by half. The DA implemented in a 0.18 μm CMOS process has a 16 dB gain at 2.4 GHz, and it can drive a 3 dBm to the antenna with an output stage drain efficiency of 31% and a power-added efficiency (PAE) of 20% while drawing 4.5 mA from a 1.8 V supply.

key words: *current reuse, driver amplifier, high drain efficiency, high PAE, low power transmitter*

1. Introduction

Recently, low speed, low power, low cost and low complexity wireless transceivers have drawn much attention as future transceiver technology trends. IEEE specifies several low power standards such as Bluetooth 802.15.1 and ZigBee 802.15.4, which operate at the unlicensed ISM band of 2.4 GHz with output power of 0 dBm [1]. The transceivers for these standards require very small current dissipation. In the transmitter chain, the driver amplifier (DA) is the last and the highest power consuming block, since it has to drive sufficient RF signal to the antenna [2]. Another critical factor of the DA is linearity. In general the linearity requirements for amplifiers can be satisfied by either employing a linearly operating output stage or by applying linearization techniques to nonlinear-high efficiency amplifiers. Linearization techniques are usually adopted in high output power, complex, and expensive RF systems, which are not suitable for low power, low cost, and low complexity transmitters. Linearization technique based systems require various adjustments and become less effective as device characteristics change with temperature and output power [2], and the additional power dissipated by the linearization circuit becomes an issue. Hence, for low power, low cost and inexpensive transceiver applications, employing a linearly operating class A amplifier is an appropriate choice. However, class A amplifiers typically have poor efficiency [3]. Several studies [4]–[7] have documented attempts to reduce the DC power of the DA; nevertheless, the efficiency is still poor. A CMOS amplifier with harmonic tuned class of operation is one of the most effective ways to realize high efficiency for low power linear modulation systems [8]. There are few reports on CMOS low-power, high efficiency amplifiers which are based on a different class of operation from the tuned topologies. This work presents a linearly operating class A amplifier with reduced DC bias current while providing high output RF power, which equates with high drain efficiency and PAE.

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2. Circuit Design

For low power applications, power consumption, integration and complexity are the main considerations for choosing the circuit schematic of the constituent blocks for the transmitter. Therefore, a single-ended DA is preferred to decrease power consumption [9]. And, due to their simple configuration and absence of DC current, passive mixers are widely adopted [9], [10]. However, because of the power conversion loss of the passive mixer, to obtain sufficient gain, linearity, and RF power at the antenna, the DA should cover the mixer gain loss as well as the remaining power gap to the antenna. Therefore, DAs are typically designed with two stages. A simplified schematic of a conventional DA is shown in Fig. 1, where the DA consists of two stages: gain and output stages. In Fig. 1, the gain stage uses a conventional cascode topology to achieve high gain, good reserve, and small Miller capacitance, and to retain stability [2]. Also, the inductive-load is used to decrease the amount of current needed to drive large capacitances at the input of the output stage [2]. The output stage adopts a common source topology for higher voltage headroom at the output signal, providing high linearity.

The efficiency and output power for an amplifier oper-

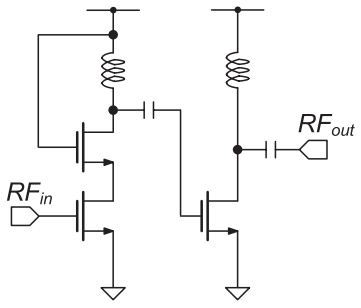

Fig. 1 Conventional two stage DA.

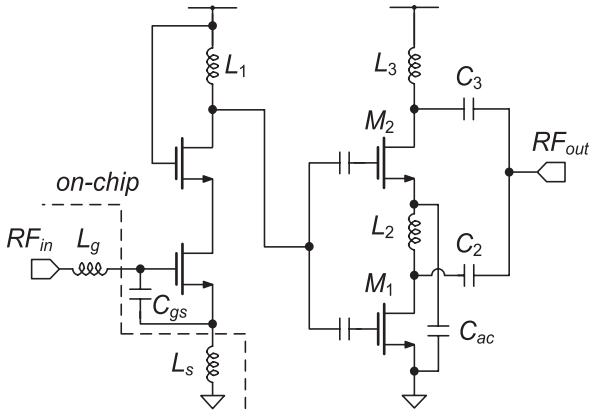

Fig. 2 Proposed current reuse DA.

ating in class A, AB, B, or C, are given by [2]

$$\eta = \frac{V_{DD} - V_{Dsat}}{V_{DD}} \frac{\theta - \sin\theta}{4\left(\sin\frac{\theta}{2} - \frac{\theta}{2}\cos\frac{\theta}{2}\right)} \tag{1}$$

$$P_{out} = \frac{1}{2}(V_{DD} - V_{Dsat})\frac{I_M}{2\pi}(\theta - \sin\theta) \tag{2}$$

where V_{DD} is the supply voltage, θ the conduction angle of the drain current (class A: θ is 2π), V_{Dsat} the pinch-off voltage (knee voltage), and I_M the maximum drain current of the input transistor.

In (1), while V_{DD} and V_{Dsat} are technology dependant, reducing the conduction angle θ increases efficiency, at the expense of reduced output power as described in (2).

However, reducing the conduction angle leads to more serious drawbacks, because it not only reduces the output power but also the linearity and gain of the amplifier [2]. Before addressing this issue, the required DC current to provide specific output RF power is studied. For example, with the output RF signal delivered into a 50 Ohm antenna, the output RF power can be expressed as [11]:

$$P_o = \left(\frac{I_{pp}}{2\sqrt{2}}\right)^2 R_{load} \tag{3}$$

where I_{pp} is the peak to peak RF current and R_{load} is the antenna impedance (50 Ohm).

If the required output power into the 50 Ohm antenna is 0 dBm, the RF peak to peak current is:

$$I_{pp} = 2\sqrt{2}\sqrt{\frac{P_o}{R_{load}}} \approx 12.6\,[\text{mA}] \tag{4}$$

To provide such output RF current, the required DC bias current for a class A amplifier should be at least half of I_{pp}. Hence, the DC bias current should be $I_{pp}/2$=6.3 mA.

Figure 2 shows a simplified schematic of the DA proposed in this work, where a current reuse output stage is proposed in order to reduce the DC current without sacrificing other performances such as gain and linearity. As can be seen in Fig. 2, the output amplifier consists of two common source amplifiers configured in parallel, and each amplifier

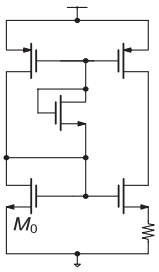

Fig. 3 Bias circuit for the output stage of DA.

can provide half of the required output current. Therefore, the DC bias for each amplifier is $I_{pp}/4$, and as a result, the DC bias can be reduced by half in comparison to that of the conventional topology.

In Fig. 2, the two transistors M_1 and M_2 utilize the same DC current from a 1.8 V supply but are AC separated by capacitor C_{ac}. The two transistors work as two separated common source amplifiers, which will provide twice as much current into the load but will dissipate the current of only one amplifier. Figure 3 shows the bias circuit for the output amplifier. Transistor M_1 in Fig. 2 is current-mirrored by the current source M_0 in the bias circuit shown in Fig. 3. The gate of M_1 is about 0.68 V. The gate of M_2 is biased at 1.8 V. In Fig. 2, the first stage of the DA is biased at 1.5 mA while the second stage is biased at 3 mA. The gate widths of the output stage's transistors were determined to be 80 μm. The values of inductors L_1, L_2, and L_3 are 3.7, 2.8 and 2.8 nH, respectively, whereas L_g and L_s are, respectively, off-chip and bonding wire inductors. As can be seen in Fig. 2, the tradeoff of the proposed DA is an additional inductor, which will increase the chip size. The fabricated chip shows an approximately 30% size increase. However, the efficiency improvement makes the additional expense acceptable. The DA uses three on-chip inductors.

3. Measurements

The DA is fabricated in a 0.18 μm CMOS process. As can be seen in Fig. 2, the input of the DA is matched to 50 Ohm using the off-chip inductor L_g, and the output is directly connected to 50 Ohm by AC coupling capacitors C_2 and C_3. The measured S-parameters of the DA are shown in Fig. 4. The gain (S21) is 16 dB and the input-output isolation is more than 35 dB at the operating band. As shown in Fig. 4, S21 experiences an additional peaking at around 2.8 GHz which can be explained by additional resonance at the output caused by several inductors and capacitors on-chip and off-chip including the bonding wire. However, this additional peaking gain is sufficiently far from the band of interest, and thus does not affect the DA's performance. Figure 5 shows the measured gain versus input power where the measured gain is 16 dB and drops 1 dB when the input power is −11 dBm. The IIP3 measurement results are presented in Fig. 6. In Fig. 6, the two fundamental tones of 2.405 and 2.4055 GHz are applied, and the IMD3 is captured

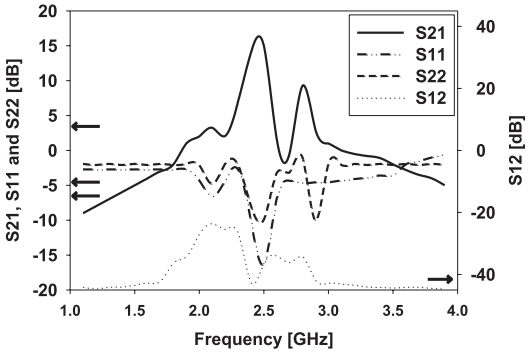

Fig. 4 S-parameters.

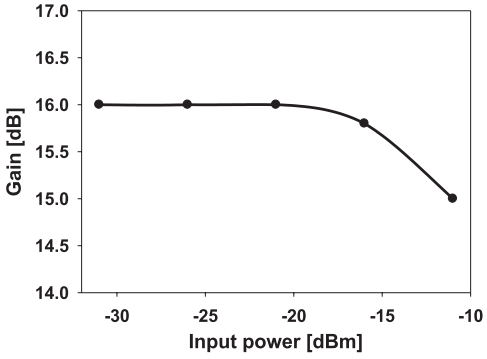

Fig. 5 Gain vs. Pin.

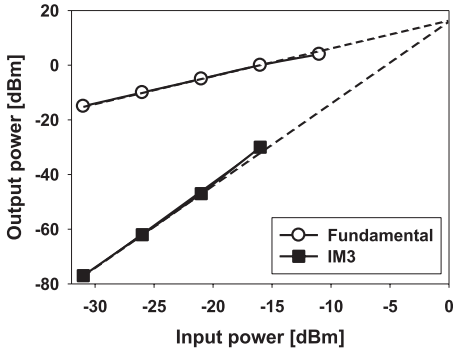

Fig. 6 OP1 dB and OIP3.

at 2.406 GHz. The OP1 dB and OIP3 are 4 and 15 dBm, respectively and the IMD3 level at OP1 dB is −18 dBm. The IEEE 802.15.1 standard's spectrum mask specifies unwanted signal suppression of −20 dBc at ±500 kHz offset from the center frequency. Therefore, the proposed amplifier should operate at the back-off state, where the output power is 2–3 dB lower than the OP1 dB. With 2 dBm output power, the IMD3 levels are under −24 dBm which satisfies the IEEE 802.15.1 standard. The output stage drain efficiency and PAE of the DA are shown in Fig. 7. At 3 dBm output power the output stage drain efficiency and PAE are 31 and 20%, respectively. Figure 8 shows the fabricated DA's chip microphotograph with chip size of 0.8 mm^2. Table 1 summarizes the measured performance of the proposed

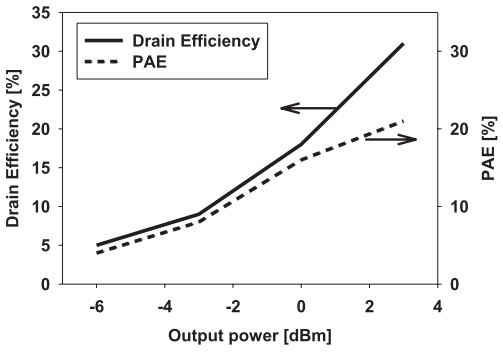

Fig. 7 Output stage drain efficiency and PAE of the DA.

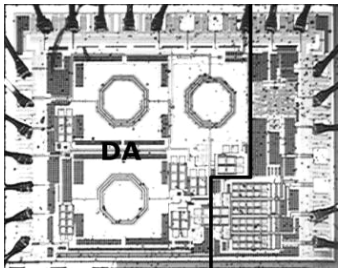

Fig. 8 Chip microphotograph.

Table 1 Summarization of DA's performances.

	This work	[4]	[5]	[11]
Gain [dB]	**16**	6	12	*
P1dB [dBm]	**3**	-3.5	3.5	0
Drain efficiency [%]	**31**	22	*	13
PAE [%]	**20**	18	12	*
Technology [μm]	**0.18**	0.13	0.18	0.25

*: not available

DA together with previously published results. In comparison with other designs, the proposed DA shows higher gain and output power with higher drain efficiency and PAE.

4. Conclusion

A low power consumption DA is presented. The output power, gain, and efficiency trade-off of the linear amplifier are reviewed as background for the proposed solution. A novel current reuse DA structure is proposed. This structure helps to reduce the DC bias current and thereby improves the efficiency and PAE. In comparison with the state of the art amplifiers, the proposed DA shows superior performances with a minor trade-off of chip size increase. The DA implemented in 0.18 μm CMOS shows 16 dB gain at 2.4 GHz and is able to drive 3 dBm to the antenna with an output stage drain efficiency of 31% and a PAE of 20%. Dissipating 4.5 mA from a 1.8 V supply, the DA's performance is quite good and it can be applied for low power wireless transmitters operating in the ISM band.

Acknowledgments

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