

Fig. 2 The half of the proposed LNA for noise analysis.

is amplified by M_4 , M_6 , and M_2 , creating output noise current ($I_{n2,M1}^2$). And the noise current ($I_{n2,M1}^2$) is now in phase with noise current at the drain of M_1 . Since the output current is differential, the noise current is partially cancelled.

Furthermore, in the proposed LNA, as can be seen in Fig. 1, the input common gate transistors (M_1 , M_2) are capacitively cross coupled to achieve input impedance matching with lower transconductance [8]. The input impedance R_{in} is given as [8]:

$$R_{in} = 1 / (2g_{mCG}) \quad (1)$$

where g_{mCG} is the transconductance of the common gate amplifier. Firstly, as can be seen in (1), due to the capacitive cross coupling configuration, the dissipating current needed to achieve specific $R_{in} = R_s$ is reduced by half. Consequently, the noise current is reduced by half, since $I_n^2 = 4kTg_{mCG}$ [3]. Secondly, as can be seen in Fig. 2, due to capacitive cross coupling configuration, transistor M_2 works as common source amplifier like M_4 and M_6 . So the required g_{mM4} and g_{mM6} to realize noise cancellation is lower. Therefore, noise currents produced by M_4 and M_6 are reduced. As a result of capacitive cross coupling configuration, the NF of the proposed LNA is reduced further in comparison with the NFs of the noise cancellation LNAs presented in [7] and [9]. The improvement in NF is shown in Fig. 3. This improvement is a result of a more quantitative understanding of the noise behavior of the proposed LNA, provided in the following. The noise analysis can be carried out for each half of the LNA, one of which consists of the common gate transistor M_1 and three common source transistors, M_2 , M_4 , and M_6 , sharing the same positive input $IN+$, shown in Fig. 2. In Fig. 2, the total input parasitic capacitance is simply presented as C_{IN} . The output noise current created by R_s is given as [3]:

$$I_{nout,R_s}^2 = 4kTR_s \left| \frac{Z_{IN}}{R_s + Z_{IN}} g_{mtotal}(f) \right|^2 = 4kTR_s \left| \frac{Z_{IN}}{R_s + Z_{IN}} \left(g_{mM4} + g_{mM6} + g_{mCGeff} + \frac{g_{mM2}}{1 + Z_s g_{mM2}} \right) \right|^2 \quad (2)$$

where g_{mM4} , g_{mM6} , is the transconductance of the common source M_4 , M_6 , respectively, g_{mCGeff} is the effective transconductance of common gate M_1 , R_{in} the input

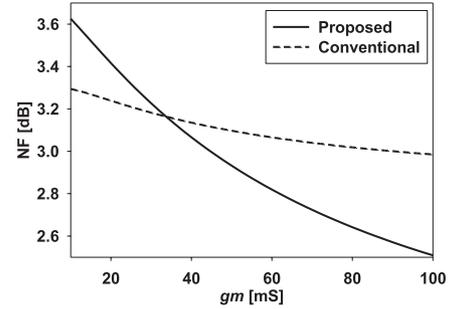


Fig. 3 Calculated NF as a function of transconductance of the common source amplifiers.

impedance of M_1 , Z_{IN} the impedance of the parallel network $R_{in} // L_{IN} // C_{IN}$, Z_s the impedance of the parallel network $R_s // L_{IN} // C_{IN}$, and $g_{mM2} / (1 + Z_s g_{mM2})$ the transconductance of the source degeneration M_2 , respectively.

The output noise current caused by the common gate amplifier M_1 is given as [3], [7]:

$$I_{nout,M1}^2 = |I_{n1,M1} - I_{n2,M1}|^2 = 4kT\gamma g_{mM1} \left| \frac{1}{1 + g_{M1} Z_s} \left(1 - Z_s \left(g_{mM4} + g_{mM6} + \frac{g_{mM2}}{1 + Z_s g_{mM2}} \right) \right) \right|^2 \quad (3)$$

where γ is the noise access factor and g_{mM1} the transconductance of transistor M_1 ($=g_{mCGeff}/2$).

The output noise current created by M_2 , M_4 , and M_6 is given as [3]:

$$I_{nout,M1}^2 = 4kT\gamma (g_{mM2} + g_{mM4} + g_{mM6})^2 \quad (4)$$

where g_{mM2} is the transconductance of amplifier M_2 ($=g_{mCGeff}/2$). The noise factor of the proposed LNA can be given as:

$$F = 1 + \frac{\gamma g_{m,M1} \left| \frac{1}{1 + g_{M1} Z_s} \left(1 - Z_s \left(g_{mM4} + g_{mM6} + \frac{g_{mM2}}{1 + Z_s g_{mM2}} \right) \right) \right|^2}{R_s \left| \frac{Z_{IN}}{R_s + Z_{IN}} g_{mtotal}(f) \right|^2} + \frac{\gamma (g_{mM2} + g_{mM4} + g_{mM6})}{R_s \left| \frac{Z_{IN}}{R_s + Z_{IN}} g_{mtotal}(f) \right|^2} \quad (5)$$

As can be seen in (5), the second term of the noise factor expression can be partially cancelled.

At the frequency of interest, L_{IN} tunes out the input parasitic capacitance C_{IN} , and $R_{in} = R_s$, therefore (5) can be rewritten as:

$$F = 1 + \frac{\gamma g_{m,M1} \left[1 - R_s \left(g_{mM4} + g_{mM6} + \frac{g_{mM2}}{1 + R_s g_{mM2}} \right) \right]^2}{R_s g_{mtotal}^2} + \frac{4\gamma (g_{mM2} + g_{mM4} + g_{mM6})}{R_s g_{mtotal}^2} \quad (6)$$

In order to match the input impedance (R_{in}) of the LNA to $R_s = 50 \Omega$, M_1 , M_2 are sized to have transconductance $g_{mM1} = g_{mM2} = 10 \text{ mS}$ (effective transconductance

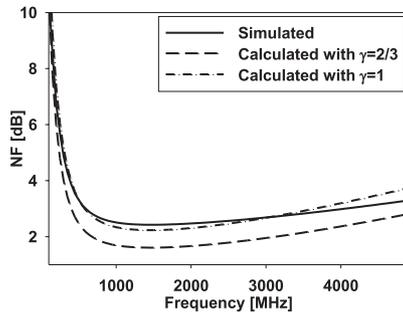


Fig. 4 Simulated and calculated NF of the proposed LNA.

$g_{mC_{eff}}$ will be 20 mS). For comparison, Fig. 3 shows the calculated NF, expressed in (6), of the proposed LNA and the NF of the noise cancellation LNA reported in [7] and [9]. The NFs are functions of the total transconductance ($g_{mCS} = g_{mM4} + g_{mM6}$) of the common source amplifier (M_4, M_6). As can be seen in Fig. 3, while the NF of the LNA reported in [7] and [9] slightly decreases, the NF of the proposed LNA significantly reduces as g_{mCS} increases. If a g_{mCS} of 100 mS is chosen, the improvement in NF is almost 0.5 dB.

In order to assess noise behavior of the proposed LNA in the entire operating frequency, the NF is calculated and studied using (5). In this design L_{IN} is chosen as 8 nH to completely tune out the input parasitic capacitance C_{IN} at the center of frequency band of interest (0.7~2.7 GHz), which is around 1.5 GHz. Thus C_{IN} is approximately 1.5 pF. g_{mM4}, g_{mM6} are chosen as 45 and 60 mS, respectively. The NF as a function of frequency, expressed in (5), is calculated and plotted in Fig. 4. The simulated NF of the proposed LNA is also shown in Fig. 4. As can be seen in this figure, the minimum NF is achieved at the resonating frequency of the LC network and increases slightly with frequency. In the operating band, the simulated minimum NF is 2.4 dB. The maximum NF is 2.6 dB at the maximum operating frequency (2.7 GHz).

To satisfy the system linearity, the LTE receiver should work in the current mode adopting the architecture as presented in [9]. Thus, the proposed LNA is designed as a transconductance stage, thereby remaining highly linear [9]. Moreover the mechanism leading to cancellation of the output noise can also lead to the cancellation of the nonlinearities of the devices [6]. Consequently, the proposed LNA shows very good linearity performance as well.

3. Simulation Results

The proposed LNA is implemented in a 0.18 μm CMOS process. The proposed LNA dissipates 9 mA from a 1.8 V supply.

Figure 5 shows the simulated input matching of the proposed LNA. As can be seen in this figure, the input return loss (S11) is lower than -10 dB in the operating band. Figure 6 shows the simulated Gm of the proposed LNA. Table 1 summarizes the simulation results of the proposed LNA in

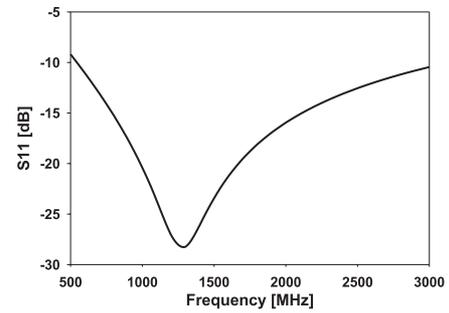


Fig. 5 Simulated input return loss of the proposed LNA.

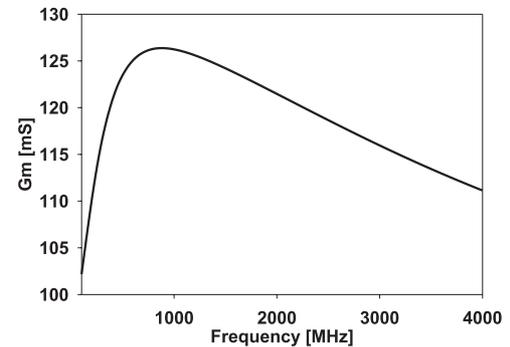


Fig. 6 Simulated Gm of the proposed LNA.

Table 1 Summary performances of the LNA.

	This work	[5]	[7]	[8]
Frequency [GHz]	0.7~2.7	3.1~10.6	1.2~11.9	0.02~1.6
S11 [dB]	<-10	-13.5	-11	-8
S21 [dB]/Gm [mS]	125mS	7~12 dB	9.7 dB	13.7 dB
NF [dB]	2.4~2.6	5.27~7	4.5~5.1	2.55~2.85
DC power [mW]	16.2	4.5	20	1.9
Technology [μm]	CMOS 0.18	CMOS 0.18	CMOS 0.13	CMOS 0.13

comparison with other published works. As can be seen here, the LNAs in [5] and [7] show ultra wideband but high NF. The LNA in [8] shows low NF and low power but poor linearity, and thus it cannot satisfy the LTE system requirement. The proposed LNA shows low NF and high linearity with moderate power consumption, and is thus suitable for adoption in the LTE receiver.

4. Conclusion

A low noise wideband amplifier design is presented. The circuit operates over a wide range of frequencies, 0.7–2.5 GHz. By adopting noise cancellation and a capacitive cross coupling technique, the NF of the LNA is significantly reduced. The frequency dependence of the noise behaviour of the proposed LNA is investigated. It has been shown that the NF of the proposed LNA slightly increases as the operating frequency increases. Simulated in 0.18 CMOS μm technology, the proposed LNA shows less than 2.6 dB NF while drawing 9 mA from a 1.8 V supply. The LNA shows good performance making it suitable for adoption in the LTE receiver.

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References

- [1] The 3GPP website. [Online]. Available: <http://www.3gpp.org>
 - [2] T.K. Nguyen, N.J. Oh, V.H. Le, and S.G. Lee, "A low-power CMOS direct conversion receiver with 3-dB NF and 30-kHz flicker-noise corner for 915-MHz band IEEE 802.15.4 ZigBee standard," *IEEE Trans. Microw. Theory Tech.*, vol.54, no.2, pp.735–741, Feb. 2006.
 - [3] B. Razavi, *Design of Analog CMOS Integrated Circuits*, Int. ed., MacGraw-Hill, 2001.
 - [4] C.W. Kim, M.S. Kang, T.A. Phan, H.T. Kim, and S.G. Lee, "An ultra-wideband CMOS low noise amplifier for 3–5 GHz UWB system," *IEEE J. Solid-State Circuits*, vol.40, no.2, pp.544–547, Feb. 2005.
 - [5] R.M. Weng, C.Y. Liu, and P.C. Lin, "A low-power full-band low-noise amplifier for ultra-wideband receivers," *IEEE Trans. Microw. Theory Tech.*, vol.58, no.8, pp.2077–2083, Aug. 2010.
 - [6] F. Bruccoleri, E.A.M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise cancelling," *IEEE J. Solid-State Circuits*, vol.39, pp.275–282, Feb. 2004.
 - [7] C.F. Liao and S.I. Liu, "A broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receivers," *IEEE J. Solid-State Circuits*, vol.42, no.2, pp.329–339, Feb. 2007.
 - [8] A. Amer, E. Hegazi, and H. Ragai, "A low-power wideband CMOS LNA for WiMAX," *IEEE Trans. Circuit Syst. II, Analog Digit. Signal Process.*, vol.54, no.1, pp.4–8, Jan. 2007.
 - [9] Z. Ru, N.A. Moseley, E. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE J. Solid-State Circuits*, vol.44, no.12, pp.3359–3375, Dec. 2009.
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