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LETTER

An Analog Controlled Variable Gain LNA with Tunable Frequency Bands

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SUMMARY An analog controlled Variable Gain LNA (VGLNA) with tunable operating frequency bands is reported. The analog control circuit for the continuous gain variation is proposed as a low voltage version. The fabricated LNA based on 0.18 μm CMOS shows a gain range of 15 ~ −12 dB (27 dB gain control), a noise figure (NF) of 2 dB, and an IIP3 of −10 dBm while 5 mA is drawn from a 1.2 V supply over the frequency range of 470~880 MHz.

key words: *analog control, LNA, low supply voltage, wideband*

1. Introduction

Designing wideband LNA involves many challenges. One of the key technical issues is recovering a weak signal under co-existing strong interferers. To make the system operate properly under the above condition, a system needs to satisfy two important parameters, noise figure (NF) and linearity. In general, for a receiver system, the system NF and cascaded IIP3 are strongly related to the gain of the first block [1]. Thus, a Variable Gain LNA (VGLNA) can offer a good overall receiver's performance (NF and IIP3) over the input signal level variations. This paper presents an LNA in combination with an analog controlled attenuator, VGLNA. In the VGLNA design, the attenuator can be placed in front [2], [3] or at the back of the LNA. The former approach can provide good LNA linearity at a low gain, but signal attenuation before the LNA can degrade the receiver NF. For the latter case, the LNA linearity stays nearly constant over the gain variation, while the system linearity and NF is improved. This work is about a VGLNA as a combination of an LNA and an attenuator whose configuration is that the attenuator is placed at the back of the amplifier for better NF. In addition, for the best NF over wide bandwidth, narrow band approach [4] with tunable function is adopted instead of wide band approaches such as feedback and common-gate which show poor NF. The Analog Control Circuit (ACC) is an important part of the attenuator adopted in this work. The previously reported ACC requires a high supply voltage and a large amount of control voltage offset, which can lead to a large control voltage [3].

The proposed tunable VGLNA has adopted an analog control circuit that can work under a lower supply voltage with no control voltage offset.

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2. Circuit Design

Figure 1 shows the frequency tunable VGLNA which consists of an LNA and an attenuator. As Fig. 1 shows, the LNA adopted the inverter type current reused topology (M_{L1}, M_{L2}) with an array capacitor (C_n) at the input and an off-chip gate inductor ($L_{g,off}$) for the wideband matching. The input impedance of the LNA shown in Fig. 1 is given by

$$Z_{in} = \frac{1 - j\omega C_{gd} R_{in,buf}}{\omega^2 (C_{gs} + C_n) C_{gd} R_{in,buf} + j\omega \left[(C_{gs} + C_n) - C_{gd}(1 + g_m R_{in,buf}) \right]} \quad (1)$$

where $R_{in,buf}$ represents the input impedance of the buffers. In (1), the value of C_n can be varied by the switches shown in Fig. 1. Suppose the $R_{in,buf}$ is infinite, the Z_{in} can be simplified to

$$Z_{in} \approx -\frac{1}{j\omega(C_{gs} + C_n) + g_m} = \frac{g_m}{g_m^2 + \omega^2 (C_{gs} + C_n)^2} - j\frac{\omega(C_{gs} + C_n)}{g_m^2 + \omega^2 (C_{gs} + C_n)^2} \quad (2)$$

From (2), the real part of Z_{in} ($\mathrm{Re}[Z_{in}]$) varied more strongly than the imaginary part ($\mathrm{Im}[Z_{in}]$) as a function of frequency. For the wideband matching, the variation of $\mathrm{Re}[Z_{in}]$ is compensated by the variation of C_n. The slower variation of $\mathrm{Im}[Z_{in}]$ with frequency is also compensated by the variation of C_n due to the slower dependence on C_n. Then, $\mathrm{Re}[Z_{in}]$ becomes optimized to stay close to 50 Ω while the $\mathrm{Im}[Z_{in}]$ is canceled by the external inductor, $L_{g,off}$. Figure 1(b) shows

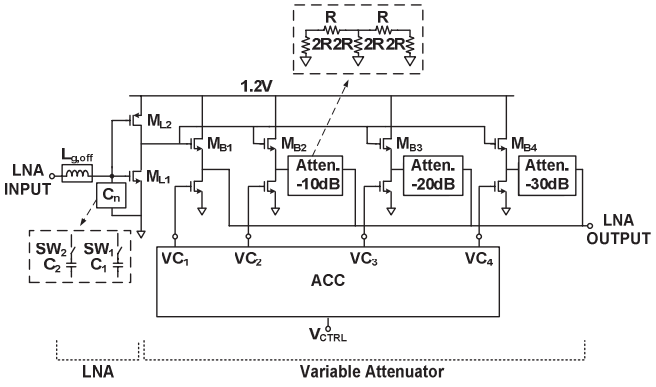


Fig. 1 Proposed frequency tunable VGLNA (bias is not shown).

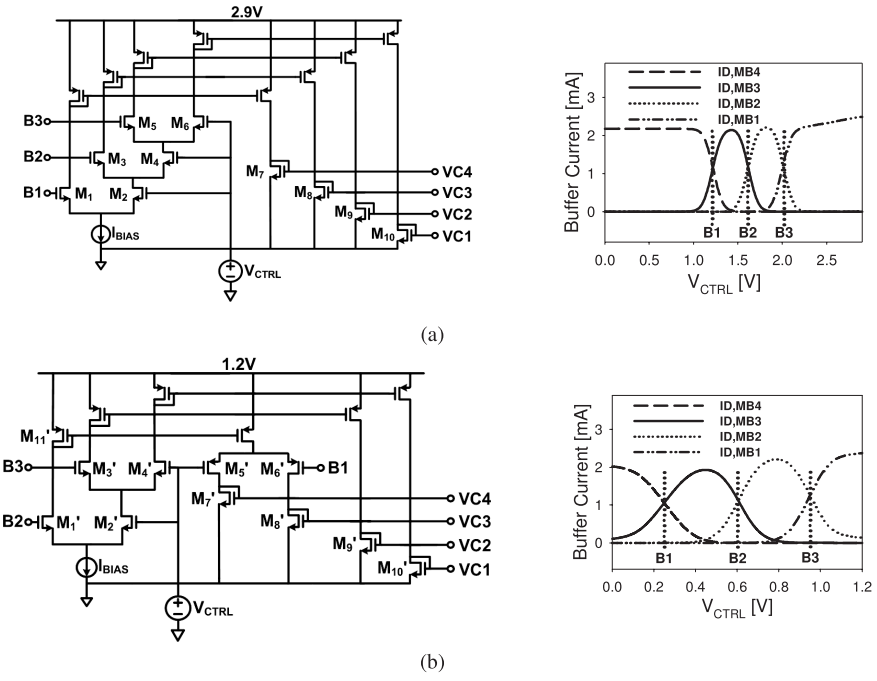


Fig. 2 ACC schematic and $I_{D,MB1-4}$ vs. V_{CTRL} (a) reported [3], (b) proposed.

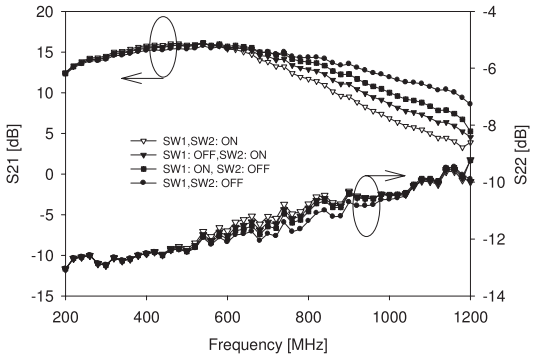
the variable attenuator in detail, which consists of buffers, attenuators, and an Analog Control Circuit (ACC). The four buffers in combination with the three attenuators are designed to provide 0, −10, −20, and −30 dB of attenuation, respectively. As can be seen in Fig. 1, the −10 dB attenuator is implemented by the cascade of two *R*-2*R* ladders. Likewise, the −20 and −30 dB attenuators are the cascade of four and six *R*-2*R* ladders, respectively. For the continuous variation of V_{CTRL}, the analog control circuit generates four consecutively continuous voltage signals, which are used to turn on the four buffers, consecutively and continuously, such that the attenuator can provide continuously varying attenuation from 0 to −30 dB. Figure 2 shows the ACC schematic and the resulting variation in the bias currents of the buffer transistors (M_{B1}, M_{B2}, M_{B3}, and M_{B4} shown in Fig. 1) by the ACC output voltage (VC_{1-4}) variations. Figure 2(a) shows the previously reported ACC schematic and the variation of buffer bias currents ($I_{D,MB1-4}$) as a function of V_{CTRL}. The problem with the ACC shown in Fig. 2(a) is the high supply voltage (2.9 V) and the large value of offset in V_{CTRL} (∼1 V) before the start of $I_{D,MB1-4}$ variations. In Fig. 2(a), the consecutive and continuous variation in $I_{D,MB1-4}$ occurs as V_{CTRL} turns on M_2, M_4, and M_6, consecutively. TheV_{CTRL} offset is caused by the minimum voltage required to turn on I_{BIAS} and M_2 as shown in Fig. 2(a), which is the point where $I_{D,MB1-4}$ variation starts. Figure 2(b) shows the proposed ACC and the corresponding $I_{D,MB1-4}$ versus V_{CTRL}. The proposed ACC can operate with a smaller supply voltage (1.2 V) due to a smaller number of transistor stacks from adopting PMOSFETs. Figure 2(b) shows the $I_{D,MB1-4}$ variations occurring from turning on M_5', M_2', and M_4', consecutively. The proposed ACC requires no offset in V_{CTRL} since M_5' is already on for $V_{CTRL} = 0$ V as M_{12}' is turned on by the combination of I_{BIAS}, V_{B2}, M_{11}', M_{12}', and V_{CTRL}. As Fig. 1 shows, when M_{B1} is off, the output impedance of the LNA stays nearly 50 Ω by choosing R=150 Ω, regardless of the bias current flowing through M_{B2}, M_{B3}, and M_{B4}. Therefore, by choosing $1/g_{m,MB1}|_{VCTRL=1.2\,V} \approx 50\,\Omega$, the LNA output matching (∼50 Ω) can be satisfied at all of the attenuation levels.

3. Measurement Results

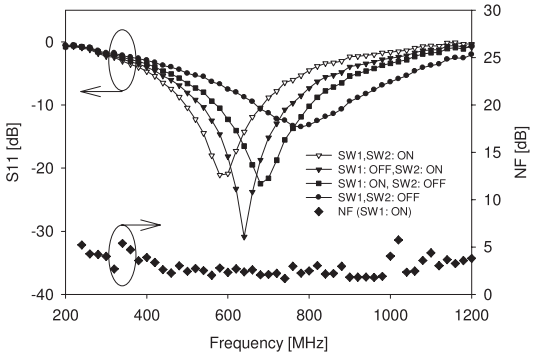
The proposed VGLNA, shown in Fig. 1 with the ACC of Fig. 2(b), is fabricated in 0.18 μm CMOS process. Fig. 3 shows the measurement results. Figure 3(a) shows the S21, S22 and Fig. 3(b) presents S11, NF versus frequency for three different settings of input matching by varying the value of C_n in Fig. 1. Two switches (SW1, SW2) make the value of C_n different for multi-band operations. For instance, the VGLNA works for lowest frequency (470∼630 MHz) when both switches are turned on. Also, the reason why the S22 shows the same results with variation of the value of C_n is good isolation between input and output.

As can be seen in Fig. 3(b), S11 is better than −10 dB in satisfying the frequency range of 470∼880 MHz. The measured peak gain and NF at 500 MHz are 15 and 2 dB, respectively. Figure 3(c) shows the gain, NF, and IIP3 at 500 MHz as a function of V_{CTRL}. From Fig. 3(c), the VGLNA shows a gain range of 27 dB (−12 to 15 dB), a NF variation of 11 dB (2 to 13.3 dB), and an IIP3 variation of 2.5 dB (−11 to −8.5 dBm) with an average value of −10 dBm.

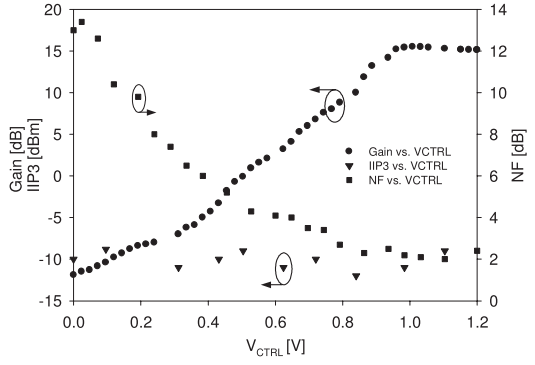
Nonlinearity always occurs from active components,



(a)



(b)



(c)

Fig. 3 Measurement results (a) S21 and S22, (b) S11 and NF vs. frequency, (c) Gain and NF vs. V_{CTRL} at 500 MHz, and IIP3 measured with 500, 510 MHz two tones.

not the passive attenuator part, so the measured IIP3 is almost constant when the gain is varied. Note that as the attenuator is being placed after the LNA, the NF at a medium gain is still low at 5.2 dB at −2 dB gain. Figure 4 is the die photograph of the proposed VGLNA. The fabricated VGLNA dissipates 5 mA from 1.2 V supply and the chip size is $700 \times 550\,\mu m^2$.

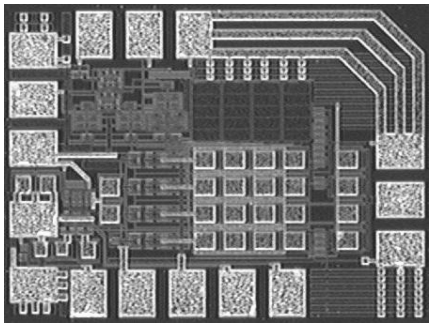


Fig. 4 The die photograph of the proposed VGLNA for DVB-H.

4. Conclusion

A variable gain LNA with tunable frequency bands is reported. The analog control circuit for the continuous gain variation is proposed as a low voltage version. The fabricated LNA based on 0.18 μm CMOS shows gain range of $15 \sim -12$ dB (a gain control range of 27 dB), a NF of 2 dB, and an IIP3 of −10 dBm while drawing 5 mA from a supply of 1.2 V over the frequency range of 470∼880 MHz.

Acknowledgments

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