A Fast and Precise Blind I/Q Mismatch Compensation for Image Rejection in Direct-Conversion Receiver

Suna Kim, Dae-Young Yoon, Hyung Chul Park, Giwan Yoon, and Sang-Gug Lee

In this paper, we propose a new digital blind in-phase/quadrature-phase (I/Q) mismatch compensation technique for image rejection in a direct-conversion receiver (DCR). The proposed image-rejection circuit adopts DC offset cancellation and a sign-sign least mean squares (LMS) algorithm with a unique step size adaptation both for a fast and precise I/Q mismatch estimation. In addition, several performance-optimizing design considerations related to accuracy, speed, and hardware simplicity are discussed. The implementation of the proposed circuit in an FPGA results in an image-rejection ratio (IRR) of 65 dB, which is the best performance with modulated signals, along with an adaptation time of 0.9 seconds, which is a tenfold increase in the compensation speed as compared to previously reported circuits. The proposed technique will be a promising solution in the area of image rejection to increase both the speed and accuracy of future DCRs.

Keywords: Image rejection, I/Q gain mismatch, I/Q phase mismatch, DC offset, direct-conversion receiver, DCR, low-IF, zero-IF, LMS algorithm, adaptive step size.

Manuscript received Apr. 05, 2013; revised Oct. 14, 2013; accepted Oct. 21, 2013.

This work was supported by the Center for Integrated Smart Sensors funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012M3A6A6054195).

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I. Introduction

The direct-conversion receiver (DCR), referred to as a low intermediate frequency (low-IF) or zero intermediate frequency (zero-IF) receiver, has been a preferred choice for many wireless communication systems of today due to its simple architecture and low power consumption. However, the in-phase/quadrature-phase (I/Q) mismatch, which degrades image signal rejection performance, has been a chronic problem in DCRs, particularly those with a low-IF receiver [1]. Some image-rejection techniques based on analog circuits have been considered as less competitive due to I/Q mismatches, which stem from an imperfectly balanced layout and process and voltage and temperature variations [2]. Currently, wireless communication systems typically require multi-mode multi-band (MMMB) single chip solutions. Unfortunately, analog calibration circuits for an MMMB single chip result in relatively high power consumption and a large chip size, thus increasing the cost to the difficulty in sharing multiple standards. For this reason, some I/Q mismatch compensation techniques have been investigated. These adopt digital or hybrid (analog/digital) solutions [3]-[12]. They overcome the limitations of analog-only solutions, and digital solutions in particular provide a programmable single calibration circuit that is likely to enable a software-defined radio receiver for the implementation of an MMMB single chip.

More specifically, digital I/Q mismatch compensation techniques have been developed not only by data-aided (DA) estimation using on-line pilot signals or off-line test tones [3]-[5] but also by non-data-aided (NDA) (blind) estimation using

statistical attributes [6]-[11]. Although DA estimation methods are usually fast and show desirable performance, blind estimation methods are preferred due to their lower levels of application dependency and complexity. Among the studies of a blind image-rejection technique, Lerstaveesin and Song [10] reported the best image-rejection ratio (IRR) of 65 dB along with simply implemented hardware enabled by a sign detection-only method. The drawbacks of their technique are its relatively long adaptation time of 6.7 seconds as well as the significant degradation of the level of accuracy that occurs under a condition of DC offset. To overcome the DC offset issue, other digital I/Q mismatch compensation techniques, including DC offset cancellation, have been investigated, but they have resulted in increased hardware complexity [4].

This paper reports a new digital image-rejection circuit using a blind I/Q mismatch compensation technique along with a DC offset cancellation scheme. The proposed image-rejection technique shows very precise accuracy, a significantly shorter adaptation time, and relatively simple hardware compared to previously reported works. An analysis of the image problem caused by the I/Q mismatches in a DCR is provided in section II. The proposed image-rejection technique, which involves the use of an I/Q mismatch compensator and a preceding DC offset compensator, is described in section III. Section IV presents the design considerations of the proposed image-rejection technique for optimum performance in terms of accuracy, speed, and hardware simplicity. Section V shows the measurement results of the proposed image-rejection circuit.

II. Image Problem in Direct Conversion Receivers

The block diagram of a typical direct-conversion receiver (DCR) is shown in Fig. 1. In this figure, each mixer of the I and Q paths multiplies the RF signal with local carriers with respective phase shifts of 0º and 90º. This mixing process is equivalent to the multiplication of the RF signal by a complex local carrier, expressed by $e^{j\omega_{LO}t} = \cos(\omega_{LO}t) + j\sin(\omega_{LO}t)$. However, due to the asymmetry between the I and Q paths of the analog circuits, the complex local carrier is modified as follows:

$$s_{LO}(t) = \left(1+\frac{\alpha}{2}\right)\cos(\omega_{LO}t+\frac{\theta}{2}) + j\left(1-\frac{\alpha}{2}\right)\sin(\omega_{LO}t-\frac{\theta}{2}), \quad (1)$$

$$= \frac{(1+\frac{\alpha}{2})e^{j\frac{\theta}{2}} + (1-\frac{\alpha}{2})e^{-j\frac{\theta}{2}}}{2} e^{j\omega_{LO}t}$$

$$+ \frac{(1+\frac{\alpha}{2})e^{-j\frac{\theta}{2}} - (1-\frac{\alpha}{2})e^{j\frac{\theta}{2}}}{2} e^{-j\omega_{LO}t}$$

$$\approx e^{j\omega_{LO}t} + \left(\frac{\alpha - j\theta}{2}\right)e^{-j\omega_{LO}t}, \quad (2)$$

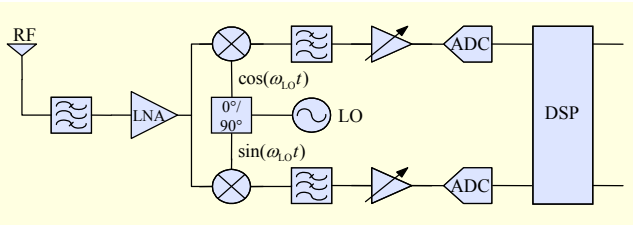

Fig. 1. Block diagram of typical DCR.

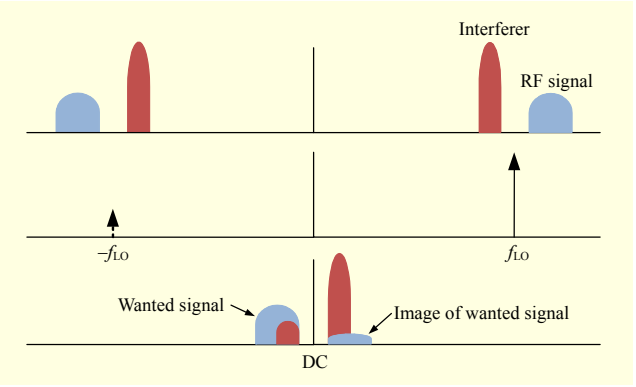

Fig. 2. Effects of mismatched local carrier on received IF signal spectra.

where gain mismatch α and phase mismatch θ between the I and Q paths are reflected symmetrically, and the values of α and θ are assumed to be very small. Assuming that the gain and phase mismatches are static over the frequency (f) of interest, the mismatches in the amplitude and phase generate unwanted leakage of the complex local carrier at the negative frequency $e^{-j\omega_{LO}t}$, as indicated in (2). The effects of the mixing process of the received RF signal and the mismatched local carrier on the received IF signal spectra are also investigated, as plotted in Fig. 2. The top portion of Fig. 2 shows the signal spectra of the RF signal and the interferer located at $\pm f_{RF}$. The middle portion of Fig. 2 shows the signal spectra of the LO signal located at $\pm f_{LO}$; the signal at $-f_{LO}$ is the leakage signal of the complex local carrier generated by the mismatches. The bottom portion of Fig. 2 shows the signal spectra of the down-converted RF signal and interferer by the LO signal; the unwanted image signals of the RF signal and interferer are also down-converted to $\pm f_{IF}$ due to the LO leakage.

We define the received RF signal as follows:

$$s_{RF}(t) = A_{sig}\cos(\omega_{sig}t) + A_{int}\cos(\omega_{int}t)$$

$$= \frac{A_{sig}}{2}\left(e^{j\omega_{sig}t} + e^{-j\omega_{sig}t}\right) + \frac{A_{int}}{2}\left(e^{j\omega_{int}t} + e^{-j\omega_{int}t}\right), \quad (3)$$

where A_{sig} (A_{int}) and ω_{sig} (ω_{int}) are the amplitude and the frequency of the wanted RF signal (interferer), respectively. Then, the received IF signal down-converted by the mismatched complex local carrier is obtained via

$$s_{IF}(t) = s_{RF}(t) \cdot s_{LO}(t)$$
$$= \frac{A_{sig}}{2} e^{-j\omega_{IF}t} + \left(\frac{A_{int}}{2} \cdot \frac{\alpha - j\theta}{2} \right) e^{-j\omega_{IF}t}$$
$$+ \frac{A_{int}}{2} e^{j\omega_{IF}t} + \left(\frac{A_{sig}}{2} \cdot \frac{\alpha - j\theta}{2} \right) e^{j\omega_{IF}t}, \quad (4)$$

where $\omega_{IF} = \omega_{RF} - \omega_{LO}$. We also assume that the high frequency components generated from the mixing process are eliminated by low-pass filters.

As shown in (4) and Fig. 2, the quality of the wanted signal that is down-converted by the mismatched complex local carrier is degraded by the image signal of the interferer. The degree of degradation can be expressed by an IRR, which is the ratio of the wanted signal power versus the image signal power, as given by

$$IRR_{dB} = 10\log\left(\frac{P_{sig}}{P_{img}}\right) = 10\log\left(\frac{A_{sig}/2}{A_{sig}/2 \cdot (\alpha - j\theta)/2}\right)^2$$
$$\approx 10\log\left(\frac{4}{\alpha^2 + \theta^2}\right). \quad (5)$$

To obtain an IRR of 60 dB, which is the typical requirement of current wireless communication systems, only a gain mismatch of 0.1% and a phase mismatch of 0.1° are allowed. Thus, extremely precise I/Q mismatch compensation can remove this image signal of the interferer from the signal band of interest, eventually increasing the signal-to-noise ratio (SNR).

III. Image Rejection Technique

In this section, we describe an image-rejection technique that resolves the problem mentioned in the previous section. As shown in Fig. 3, the proposed image-rejection circuit consists of a DC offset compensator and an I/Q mismatch compensator. The I/Q mismatch compensator utilizes the sign-sign least mean squares (LMS) algorithm, and the DC offset compensator precedes the I/Q mismatch compensator for a more accurate mismatch estimation. The details of the proposed image-rejection circuit shown in Fig. 3 will be explained in the following subsections.

1. Mismatch Estimation Based on Sign LMS Algorithm

A perfectly matched DCR is designed to receive both *I* and *Q* signals with the same gain but at 90° out of phase. Assuming that the two signals are wide-sense stationary, the magnitude of each signal can be obtained from its autocorrelation; hence, the difference between the two autocorrelations indicates the gain mismatch between them, as follows:

$$u_\alpha = E\{I^2 - Q^2\}$$
$$= E\left\{\left(1+\frac{\alpha}{2}\right)^2 \cos^2(\omega_{LO}t + \frac{\theta}{2}) - \left(1-\frac{\alpha}{2}\right)^2 \sin^2(\omega_{LO}t - \frac{\theta}{2})\right\}$$
$$= \frac{1}{2}\left(1+\frac{\alpha}{2}\right)^2 - \frac{1}{2}\left(1-\frac{\alpha}{2}\right)^2 = \alpha, \quad (6)$$

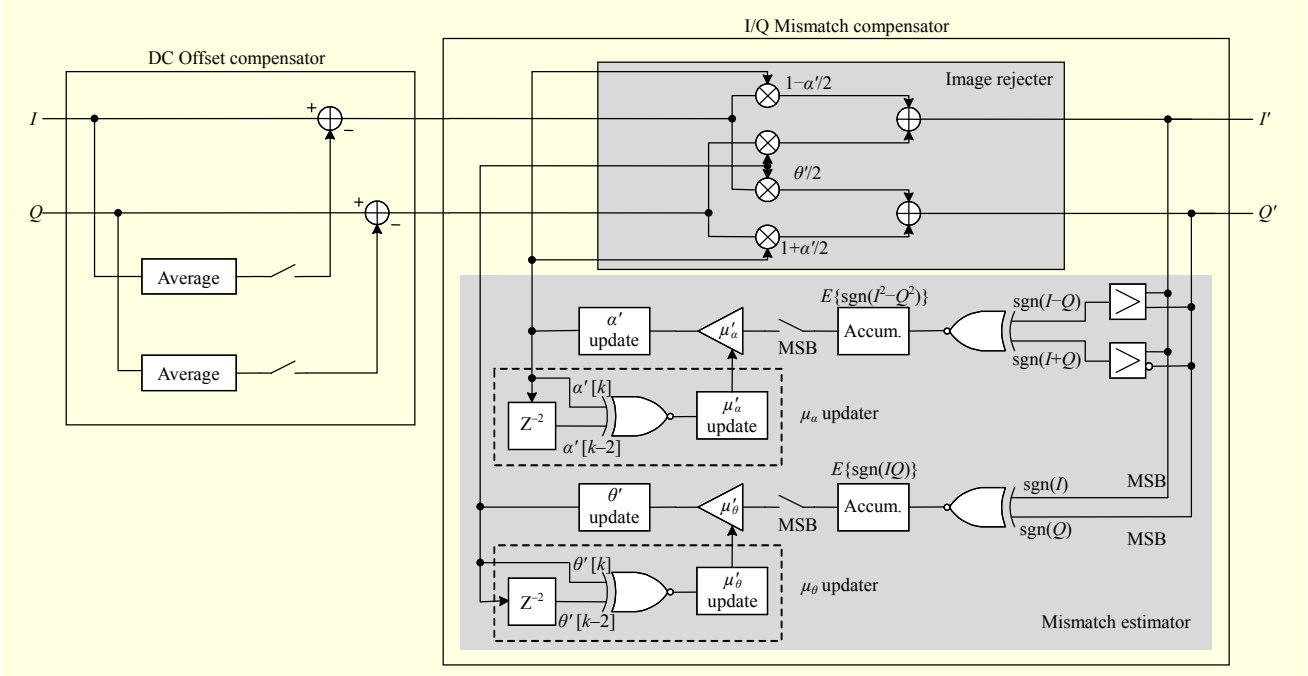

Fig. 3. Block diagram of proposed image-rejection circuit.

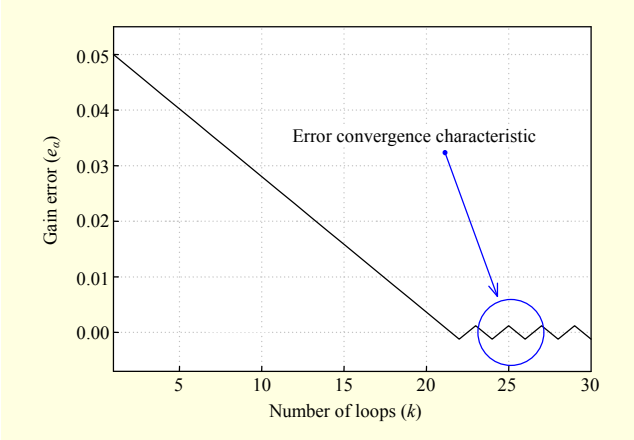

Fig. 4. Error convergence characteristics of sign LMS algorithm.

where $E\{\cdot\}$ is an expectation function, and signals I and Q are borrowed from (1). In a similar manner, because signals I and Q are orthogonal and uncorrelated with each other, the cross-correlation of the two signals indicates the amount of the phase mismatch between them, as follows:

$$\begin{aligned} u_\theta &= E\{I \cdot Q\} \\ &= E\left\{\left(1+\frac{\alpha}{2}\right)\cos(\omega_{\mathrm{LO}}t+\frac{\theta}{2})\cdot\left(1-\frac{\alpha}{2}\right)\sin(\omega_{\mathrm{LO}}t-\frac{\theta}{2})\right\} \\ &= -\left(1-\frac{\alpha^2}{4}\right)\frac{\cos\theta}{2} \approx -\frac{\theta}{2}. \end{aligned} \tag{7}$$

Based on this principle, the gain and phase mismatches of the I and Q signals can be estimated using the sign LMS algorithm. These are respectively given by

$$\alpha'[k+1] = \alpha'[k] + \mu_\alpha \,\mathrm{sgn}(u_\alpha) \tag{8}$$

and

$$\theta'[k+1] = \theta'[k] + \mu_\theta \,\mathrm{sgn}(u_\theta), \tag{9}$$

where $\alpha'[k]$ and $\theta'[k]$ represent the estimated gain and phase mismatches at the k-th loop, respectively, and μ_α and μ_θ represent the step size of the LMS algorithm for the gain and phase mismatch estimations, respectively. The expectation values, u_α and u_θ, will produce zero if the I and Q signals have the same magnitude along with being 90° out of phase.

Defining the gain error as the difference between the actual and the estimated gain mismatches (that is, $e_\alpha[k] = \alpha[k]-\alpha'[k]$) and the phase error as the difference between the actual and the estimated phase mismatches (that is, $e_\theta[k] = \theta[k] - \theta'[k]$), the sign LMS adaptation process converges when $e_\alpha[k]$ and $e_\theta[k]$ come within $\pm\mu_\alpha$ and $\pm\mu_\theta$, respectively. Figure 4 shows the error convergence characteristics for an example of a gain mismatch of 5% and a step size of 0.244%. The smaller the values of e_α and e_θ are, the more accurately α' and θ' can be estimated, leading to a greater amount of IRR. However, more accurate values of α' and θ' require smaller values of μ_α and μ_θ, which results in a longer adaptation time for convergence. Therefore, the IRR and the adaptation time of the sign LMS algorithm exist in a tradeoff relationship, which can explain the relatively long adaptation time for the high IRR in an image-rejection circuit in earlier work [10].

2. Proposed I/Q mismatch Compensator

The mismatch estimation process using the sign LMS adaptation method shown in (8) and (9) converges when $e_\alpha[k]$ and $e_\theta[k]$ come within $\pm\mu_\alpha$ and $\pm\mu_\theta$, respectively. Consequently, as shown in Fig. 4, the mismatch estimator displays a unique characteristic in that the errors converge to zero, at which point they oscillate between two different values once the errors are reduced within $\pm\mu$. In this work, as shown in Fig. 3, along with the convergence characteristics, the adoption of the proposed μ updater resolves the tradeoff relationship between the IRR and the adaptation time of the sign LMS algorithm. The proposed μ updater produces an adaptive step size of μ' when the error converges, that is, $e[k] = e[k-2]$. The adaptation process starts with a large initial step size to speed up the entire adaptation process; when the convergence characteristics are detected, the μ updater reduces the step size and continues the adaptation process until the next convergence is detected. The proposed mismatch estimator adopts a binary searching algorithm for a simple and fast estimation such that the μ updater reduces the step size by half at every convergence. The μ update process is repeated until the step size μ becomes small enough to satisfy the required IRR such that a high IRR and fast adaptation speed can be achieved simultaneously. In Fig. 5, the process of error

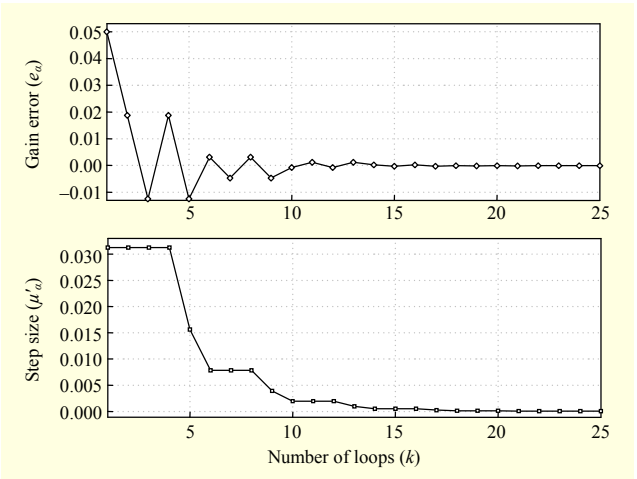

Fig. 5. Convergence characteristics of gain error and step size updates.

convergence in accordance with the step size update of the proposed mismatch estimator is demonstrated for an example of a gain mismatch of 5%. In the figure, the step size μ'_α is initially set to 0.03125(=2^{-5}) and is reduced by half when the error convergence characteristics are detected in e_α. The initial step size can be optimally determined by the process described in section IV. By virtue of the proposed μ updater, the gain error is appreciably reduced within only a few loops.

The proposed mismatch estimator including the μ updater, which is shown in Fig. 3, is now given by

$$\alpha'[k+1] = \alpha'[k] + \mu'_\alpha[k] \text{ sgn } [E\{\text{sgn}(I+Q) \cdot \text{sgn}(I-Q)\}] \quad (10)$$

and

$$\theta'[k+1] = \theta'[k] + \mu'_\theta[k] \text{ sgn } [E\{\text{sgn}(I) \cdot \text{sgn}(Q)\}], \quad (11)$$

where μ'_α and μ'_θ are the adaptive step sizes produced by the μ updater. The expectation values in (10) and (11) are implemented by a simple accumulation circuit, and the μ update is performed by a shift right operation. As shown in Fig. 3 and in (10) and (11), for a simple hardware implementation, the gain mismatch estimator is required to detect only the respective signs of I+Q and I–Q, instead of taking the entire magnitude of $I^2 - Q^2$. In the same manner, the phase mismatch estimator is required to detect only the respective signs of I and Q, referred to as the sign-sign LMS algorithm. As the error convergence characteristics of the sign-sign LMS algorithm are identical to those of the sign LMS algorithm, the proposed μ updater is also feasible for use with the sign-sign LMS algorithm.

As shown in Fig. 3, using the estimated gain and phase mismatches (α' and θ') from the proposed mismatch estimator, the image rejector compensates for the received signal against the image signal caused by the mismatches. The image rejector is implemented with just four multipliers and two adders because the compensated signals (I', Q') can be obtained by a linear combination of the mismatched signals (I, Q) [10].

Given that the proposed I/Q mismatch compensator adopts a blind estimation method that depends only on the statistical properties and the repeated error convergence characteristics, it has the advantage of application-independence.

3. DC Offset Compensator

The sign-sign LMS algorithm used in the proposed I/Q mismatch compensator accumulates errors at the DC [10]. As a result, the accuracy of the mismatch estimation is strongly affected by any possible signals or offset components at the DC. For a demonstration, the proposed I/Q mismatch compensator, which includes the proposed mismatch estimator expressed in (10) and (11), is simulated for a signal with an intentionally added DC offset. Figure 6 shows the average amount of IRR through 10,000 trials for the proposed I/Q mismatch compensator as a function of the normalized DC offset to the signal amplitude. The result demonstrates that the IRR is degraded severely with the DC offset. To resolve this problem, the proposed image-rejection circuit adopts a simple DC offset compensator [13] before the I/Q mismatch compensator, as shown in Fig. 3. The DC offset compensator consists of an offset estimator and a subtractor for each I/Q path. The offset estimator estimates the offset by averaging a certain period of the received signals based on the assumption that the transmitted signals are zero-mean stochastic signals, and the subtractor then removes the estimated DC offset from the received signals.

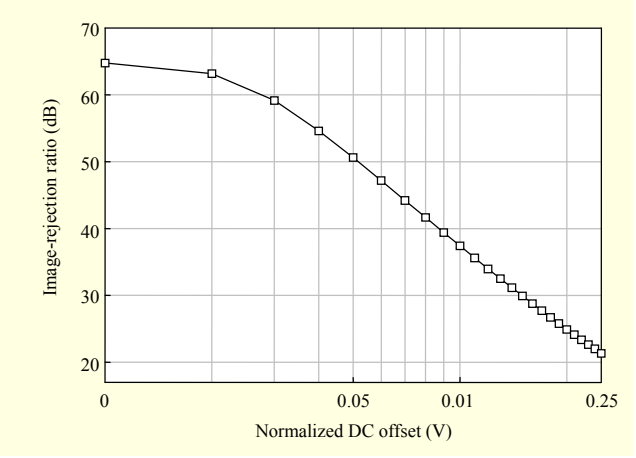

Fig. 6. IRR of proposed I/Q mismatch compensator as function of normalized DC offset.

IV. Design Considerations

The proposed I/Q mismatch compensator, which adopts the sign-sign LMS algorithm with a step size updater, improves the speed of the compensation process while keeping its accuracy intact. However, in some wireless transceiver systems that operate with low carrier frequencies, a low sampling rate is unavoidable such that the data accumulation time to obtain the expectations in (10) and (11) becomes longer. When such an unsatisfactory performance is predicted, it is better to use the magnitude detection method to implement a simple hardware setup, as shown in (8) and (9), so that a smaller amount of data is used for mismatch detection, than to use the sign detection method, as shown in (10) and (11). As a result of the simulation, the amount of IRR is plotted as a function of the amount of data for accumulation for a comparison of the magnitude detection and sign detection processes, as shown in Fig. 7. 10-bit 64-QAM I/Q signals with gain and phase mismatches of 5% and 3º, respectively, are used, and the IRR results are

ETRI Journal, Volume 36, Number 1, February 2014
http://dx.doi.org/10.4218/etrij.14.0113.0320

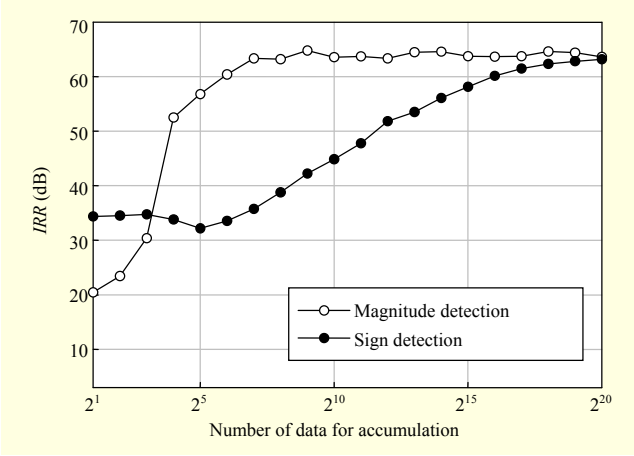

Fig. 7. Plot of IRR as function of number of data for accumulation for magnitude and sign detections.

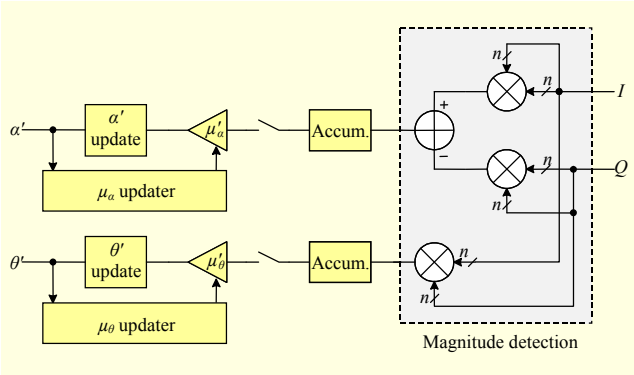

Fig. 8. Block diagram of mismatch estimator with magnitude detection.

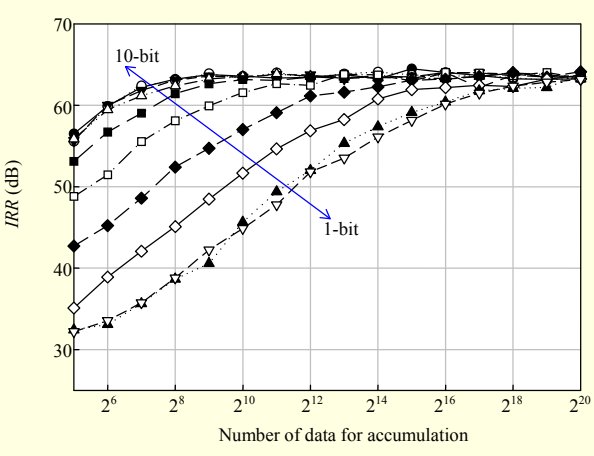

Fig. 9. IRR as function of number of data for accumulation for approximated resolutions of signals (from 10-bit to 1-bit).

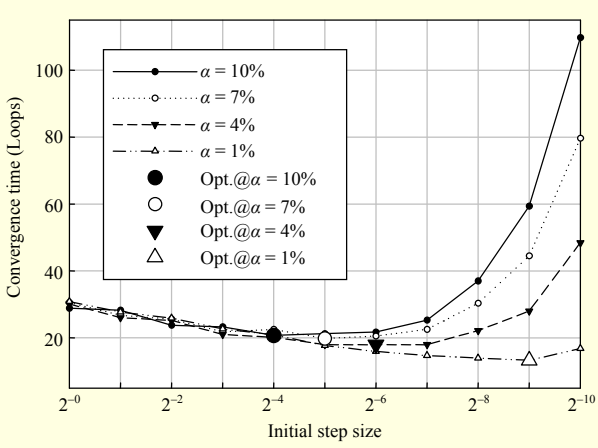

Fig. 10. Convergence time as function of initial step size for various gain mismatches.

averaged through 10,000 trials. The magnitude detection, that is, the sign LMS algorithm, can provide an IRR of 60 dB for a small amount of data accumulation, 2^6, while the sign detection method requires considerably more data accumulation, 2^{20}, to obtain the same IRR.

However, whereas a one-bit (sign) multiplication function can be implemented by a simple XNOR gate, as shown in Fig. 3, the magnitude detection function requires bulky multi-bit multipliers, as shown in Fig. 8. It is not easy to justify a higher speed while guaranteeing higher accuracy at the expense of a bulky chip size. This conflict can be mitigated by sacrificing the signal resolution for the accumulation time. To retain the accuracy, the approximation of the signal with a few most significant bits (MSBs) can shrink the chip size of the multiplier in the squared ratio, but at the cost of increasing the amount of data for accumulation. Figure 9 shows the average IRR through 100 trials as a function of the amount of data for accumulation for approximated resolutions of the signal (from 10 bits to 1 bit). This simulation is performed with a signal environment identical to that shown in Fig. 7; hence, the results from the approximated resolution of 10 bits and 1 bit correspond to the magnitude detection and the sign detection methods, respectively. It should be noted that the signal approximation process clearly induces another DC offset, which degrades the image-rejection performance. Therefore, an additional DC offset compensator needs to be added before the accumulation (expectation) process to obtain more accurate results.

The initial step size for the μ updater in the proposed I/Q mismatch compensator is also important to consider. A large initial step size increases the adaptation speed by tracing mismatches with a large step in the beginning. However, if the actual mismatch is smaller than the initial step size, adaptation time is wasted until the step size is reduced to its minimum value by repeating the convergence cycles. Figure 10 shows the convergence time (number of loops) as a function of the initial step size for various gain mismatches of 10%, 7%, 4%, and 1% when the phase mismatch is set to zero. The same

10-bit 64-QAM *I*/*Q* signals as those used in the previous simulations are used again, and the resulting values are the averages of the data collected through 100 trials. The optimum points marked in Fig. 10 demonstrate that the largest initial step size does not always result in the shortest adaptation time. Therefore, to ensure an optimum level of performance, the proposed image-rejection technique should be applied with a proper initial step size based on the roughly estimated mismatches.

V. Measurement Results

Figures 11(a) and 11(b) respectively show a block diagram and an image of the measurement setup used to test the proposed image-rejection circuit. As shown in Fig. 11(a), an LO signal of 457 MHz is generated from a signal generator (Agilent 83630B), and it goes through two phase shifters (JSPHS-661+ from Mini-Circuits), which produce a phase difference of (90º + θ) between the two LO paths. After these phase shifts, two variable gain amplifiers (VGAs) (VG025 from WJ Communications) produce a gain difference of α% between the two paths. The 256-QAM signal, modulated with a symbol rate of 400 ksps, is carried by an RF signal of 460 MHz generated from a vector signal generator (Agilent E4438C), after which it is down-converted to 3 MHz as a low-IF signal by two mixers (HMC585MS8G from Hittite) with a mismatched complex LO signal. The 256-QAM signal is chosen considering the susceptibility of the high-level modulation signals to the image signals. The low-pass filtered (PLP-10.7-75 from Mini-Circuits) IF signals are converted into a discrete form by two 14-bit I/Q ADCs (ADS62P49 from Texas Instruments) with a sampling clock of 32 MHz. The proposed image-rejection circuit is implemented into an FPGA (XC6SLX150T from Xilinx), and the measured FPGA output is then evaluated using MATLAB.

Figure 12 shows the magnitude spectra of the complex 256-QAM before and after image rejection from the measurement. As shown in the figure, the IRR of 35 dB before the image-rejection process is improved to 65 dB after this process, which is noted to be the highest degree among the reported measurement results using the modulated signal as the input. Also, the DC offset before the image rejection nearly disappears after the image-rejection process. The DC offset cancellation loop is updated at every 2^{14}-th instance of data. Because the DC offset compensator precedes the I/Q mismatch compensator, the proposed image-rejection system can also be applied to zero-IF receivers for self-image rejection.

In Fig. 13(a), the measured convergence times for the gain mismatch estimation of the proposed and sign-sign LMS [10] image-rejection circuits are compared. While the sign-sign

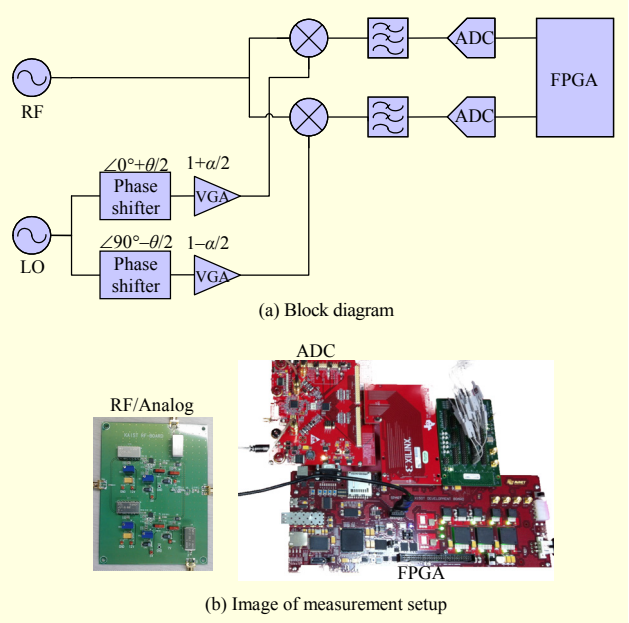

Fig. 11. Testing proposed image-rejection circuits.

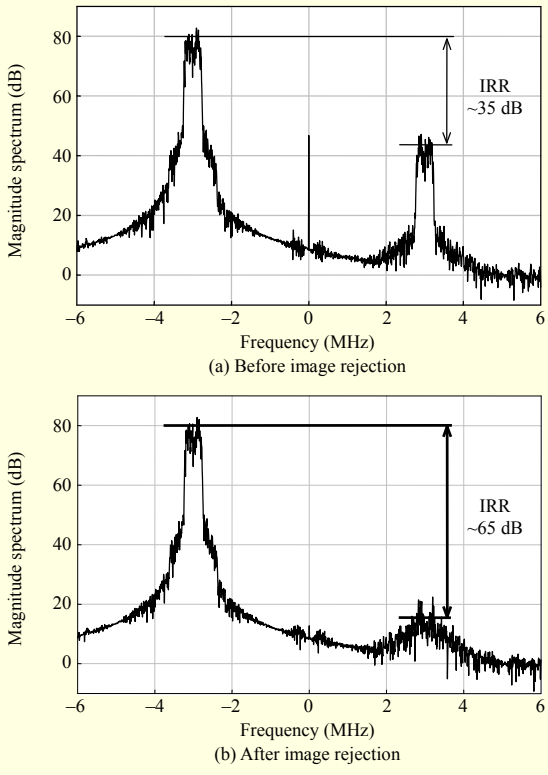

Fig. 12. Magnitude spectra of measured 256-QAM before and after image rejection.

LMS method takes 2.8 seconds to converge with a fixed step size of 0.0244%, the proposed method takes 0.7 seconds to converge with an adaptive step size from the initial value of1.56% to the final value of 0.0244%, which is four times

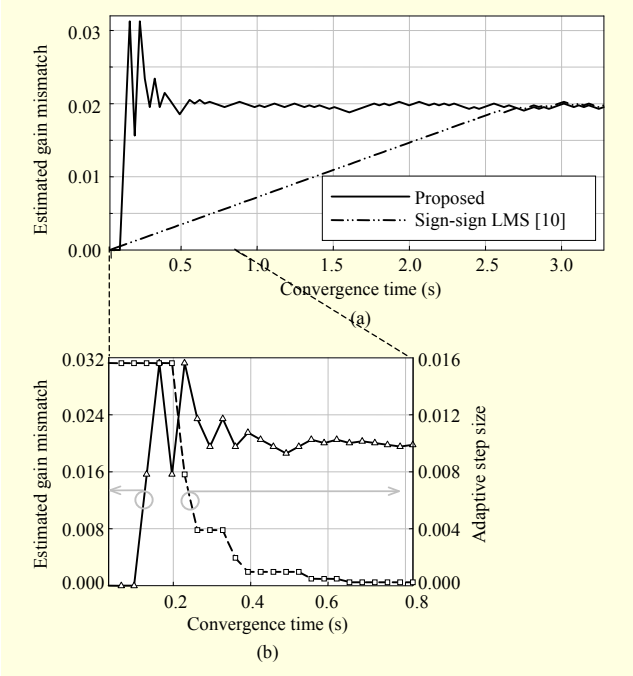

Fig 13. Gain mismatch adaptation: (a) comparison of convergence times and (b) adaptation process along with adaptive step size.

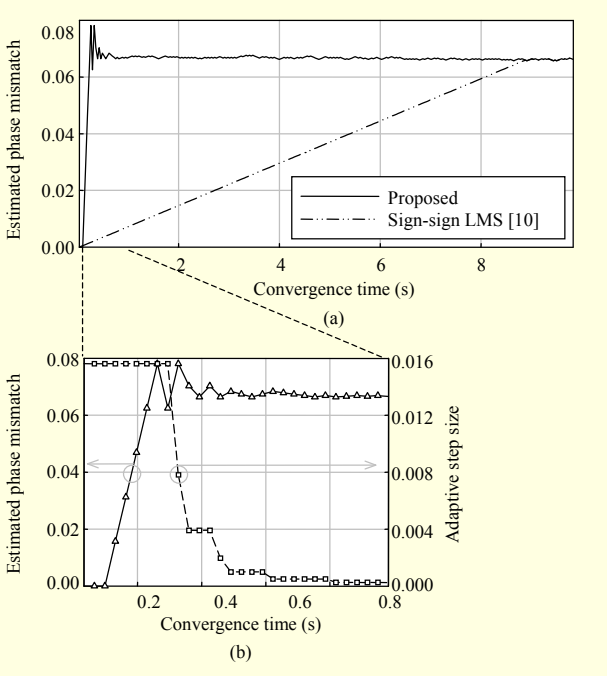

Fig 14. Phase mismatch adaptation: (a) comparison of convergence times and (b) adaptation process along with adaptive step size.

shorter. Both of the image-rejection circuits utilize data accumulation of 2^{20} for one loop with the same sampling clock of 32 MHz. Figure 13(b) shows the adaptation process of the gain mismatch estimation along with its adaptive step size in the proposed image-rejection circuit. As intended, the estimated gain mismatches approach rapidly toward convergence with a large step size in the beginning, while the final convergence gives more precisely estimated gain mismatches with a fine step size.

Figure 14(a) shows a comparison of the measured convergence times for the phase mismatch estimation of both the proposed and sign-sign LMS [10] image-rejection circuits. In Fig. 14(a), while the sign-sign LMS method in earlier work [10] takes 9 seconds to converge with a fixed step size of 0.0244%, the proposed method takes only 0.9 seconds to converge with an adaptive step size from the initial value of 1.56% to the final value of 0.0244%, which is ten times shorter. Both of the image-rejection circuits use the same number of data accumulation instances and the same sampling clock as those used in the gain mismatch estimation. Figure 14(b) shows the adaptation process of the phase mismatch estimation along with the adaptive step size in the proposed image-rejection circuit. Similar to the gain mismatch estimation, the phase mismatch estimation has shown both fast and precise adaptations.

The estimated phase mismatch in Fig. 14 (6.7% in radian,

Table 1. Performance comparison between this work and other works.

	This work	[10]	[9]	[8]	[12]	[3]
IRR	65 dB (digital)	65 dB (digital)	60 dB (digital)	57 dB (hybrid)	55 dB (digital)	63 dB (hybrid)
Adaptation time (mismatch)	0.9 s (6.7%)	6.7 s (6.25%)	-	5 ms (± 0.02 V)	5 ms (4.4%)	-
Sampling frequency	32 MHz	40 MHz	27 MHz	5 MHz	480 MHz -500 MHz	21.05 MHz
Modulation	256-QAM	256-QAM	NTSC	CW	CW+GSM	FM
Estimation method	NDA	NDA	NDA	NDA	DA+NDA	DA
Comments	Best IRR high speed	Best IRR low speed	Good IRR	High speed w/CW calibration	High speed w/CW factory calibration	Good IRR

3.8º in degree) is 3.4 times larger than the estimated gain mismatch in Fig. 13 (2%). Whereas the convergence time of the phase mismatch estimation process is only 1.3 times longer than that of the gain mismatch estimation process in the proposed method, the convergence time in the sign-sign LMS method is directly proportional to the amount of mismatch. Therefore, the proposed image-rejection circuit is more advantageous, especially in cases with a high degree of mismatch.

Lastly, the performance of this work is compared with the performances of previously reported image-rejection circuits, as summarized in Table 1. Overall, compared to the results in the other studies, this work shows the best performance in terms of the IRR, owing to the precise mismatch estimation. It also shows a high adaptation speed considering its modulation level. These outstanding results are attributed to the proposed adaptive step size scheme.

VI. Conclusion

In this paper, we proposed a new digital blind I/Q mismatch compensation technique for image rejection in a DCR. The proposed image-rejection circuit combines DC offset cancellation and an adaptive step size sign-sign LMS algorithm for fast and precise I/Q mismatch compensation. In addition to the need for a DC offset cancellation block prior to the I/Q mismatch compensation block, both the I/Q mismatch compensation and the step size update techniques were explained in detail. Moreover, the several design considerations to optimize the performances of the proposed image-rejection circuit were discussed in terms of its accuracy, speed, and hardware simplicity. Finally, the implementation of the proposed technique in a low-IF receiver system showed a desirable IRR of 65 dB along with a significant reduction in the adaptation time compared to the results in earlier studies. Thus, the proposed technique appears to be a promising solution for image rejection issues in that it increases both the speed and the accuracy of the output by adopting a unique step size updater. Moreover, it is feasible for use with a simple hardware configuration via a sign detection-only method.

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