isolation between copolarization and cross-polarization is found to be −17 dB along the bore sight. The *yz*-plane reveals that it is a directional antenna. The gain of the antenna is 3.7 dBi over the entire band calculated using the gain comparison method.

5. CONCLUSION

A novel via free directional zeroth-order resonant antenna suitable for WLAN applications based on asymmetric coplanar strip fed CRLH TL with a dimension of 29 × 16.5 × 1.6 mm^3 (when printed on a substrate of dielectric constant 3.7) is fabricated and its results are presented. The asymmetry in feeding is effectively utilized to enhance the directivity of the antenna. An IDC is used for making unit cell of CRLH TL. The technique is very simple and it can be easily integrated with other microwave integrated circuits. The proposed antenna exhibits relatively high directivity, good bandwidth, and gain characteristics as compared to the existing single band antennas.

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STI EDGE EFFECT ON THE SERIES RESISTANCE OF CMOS SCHOTTKY BARRIER DIODES

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ABSTRACT: *An analysis of the shallow trench isolation (STI) edge effect on CMOS Schottky barrier diode (SBD) is reported in this article. The STI edge effect, which includes the impact of the fringing electric field and the nonplanar intersection of STI, significantly distorts the performance of SBDs with a small junction. Due to this effect, when an array SBD is formed by connecting several SBDs with a small junction in parallel, the series resistance of the array SBD is not reduced as expected. Therefore, the cut-off frequency of an array SBD with a small unit junction SBD degenerates quickly. This phenomenon is observed in measurements of fabricated CMOS SBD prototypes.* © 2014 Wiley Periodicals, Inc. Microwave Opt Technol Lett 56:932–935, 2014; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.28218

Key words: *array; edge effect; Schottky barrier diode; series resistance; shallow trench isolation*

1. INTRODUCTION

The recent research interest in RF circuits is higher frequency operation in these circuits. For these circuits to operate at a high frequency, it is essential to consider the switching speed of the relevant devices. Traditionally, compound semiconductor technology is used at high frequencies owing to its high mobility. However, studies based on CMOS technology have been performed recently due to its low cost and high integrability. In particular, the CMOS Schottky barrier diode (SBD) has been studied. It has a Schottky contact on the anode formed by a junction between the metal and a low-doped semiconductor and an ohmic contact on the cathode [1, 2].

SBD is referred to as a majority carrier device because only a majority carrier affects the current transportation at the Schottky contact. Because it needs no time for minority carrier storage, the switching speed of a SBD is very fast.

The equivalent circuit of a SBD is represented in Figure 1 [1]. Here, R_s is the series resistance, R_j is the junction resistance, and C_{j0} is the junction capacitance. The switching speed of a SBD can be indicated by the cut-off frequency, f_T, which is represented as

$$f_T = \frac{1}{2\pi R_s C_{j0}} \tag{1}$$

As shown in Eq. (1), f_T is determined by the values of R_s, and C_{j0}, and these two factors are related to the anode size [3]. Therefore, several researches for various shapes of junction have been conducted. With the same total anode junction size, a single square junction SBD and an array of 8 × 8 minimum-sized parallel junction SBD has been compared, as shown in Figure 2(a) [4]. In this study, f_T of the array-junction SBD is higher than that of the single square junction SBD, because the parallel connection of the array decreases R_s while C_{j0} maintain its current value. However, as the size of the unit junction becomes smaller as shown in Figure 2(b), series resistance reduction is not significant in array SBDs. In this article, the reasons behind the limitation of the series resistance reduction of CMOS SBDs are introduced.

In Section 2, an analysis of the STI edge effect on series resistance is given. In Section 3, the fabrication of the CMOS

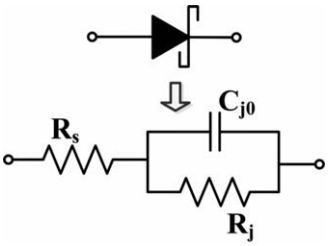

Figure 1 Equivalent model of SBD

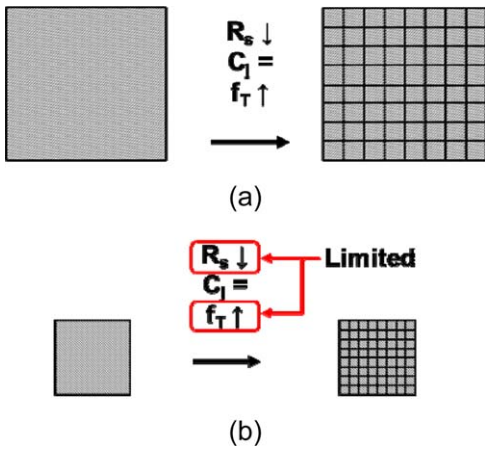

Figure 2 Parameters change of anode for (a) large total size [4] and (b) small total size. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

SBD and measurement results which show the limitation of the series resistance reduction are presented.

2. STI EDGE EFFECT ON THE SERIES RESISTANCE

As we make the anode junction size smaller to increase f_T, various side effects appear. In particular, the edge effect affects the series resistance R_s. Figure 3 represents the distribution of the electric field for different anode lengths. As shown in Figure 3(a), most of the current flow through the center field in the SBD with a long anode length. However, when the anode length is short as Figure 3(b), the fringing electric field near the edge of the anode is greater than the field in the center. Therefore, most of the current flow close to the polysilicon gate, the boundary between the anode and cathode. As a result, the current density becomes greater on the edge of the anode rather than at the center. This is known as the edge effect [3]. As a result, R_s is not "scaled" with the anode area. Consequently, it is reasonable that R_s is not halved when the anode length doubles.

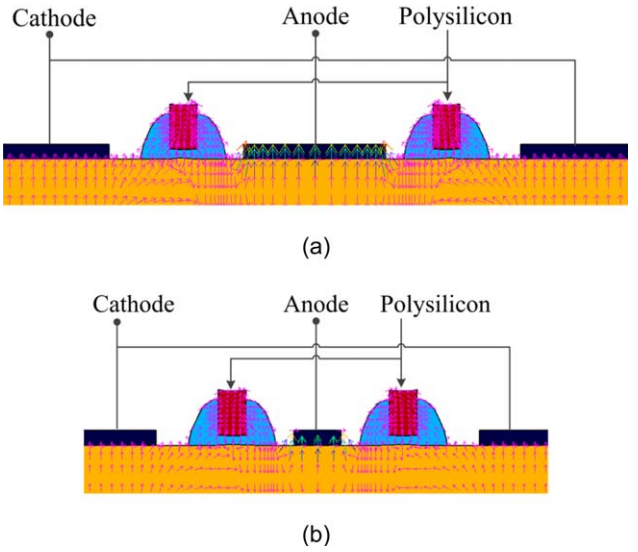

Figure 3 Electric field distribution in the SBD anode for (a) a long anode length and (b) a short anode length. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

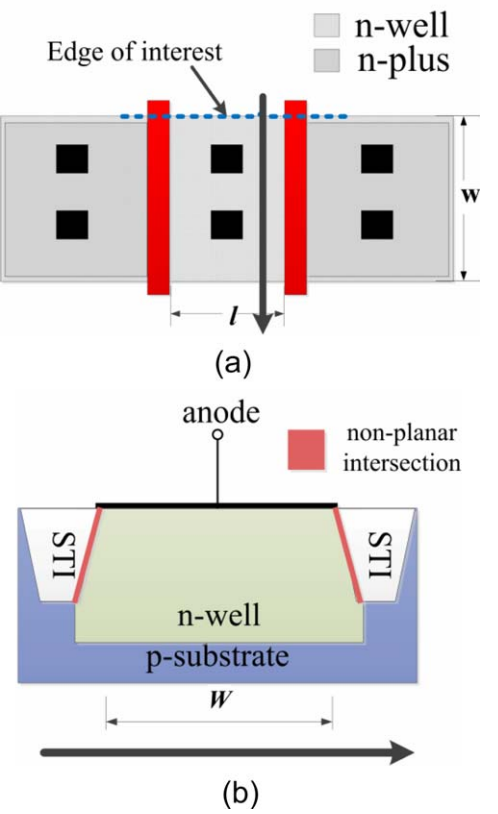

Figure 4 (a) The layout of the unit cell and (b) vertical cross section of the anode region. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

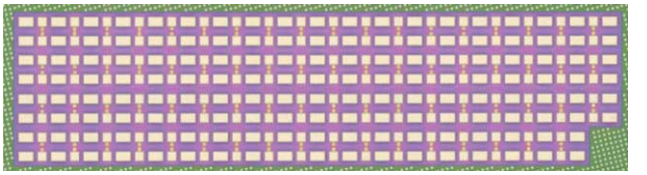

Figure 5 Micrograph of several patterns of CMOS. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

Particularly, the edge effect in the direction of the width is significant. In Figure 4(a), both ends of the anode width direction touch the shallow trench isolation (STI) region. To realize

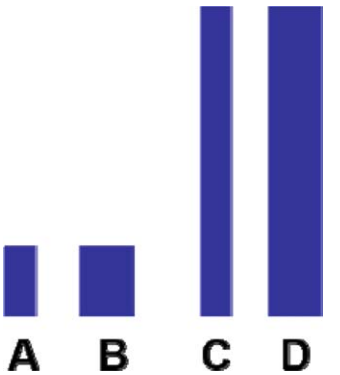

Figure 6 Diagram of each anode type (scaled). [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

TABLE 1 Anode Width and Length of Each SBD Pattern

Pattern Type	Length (μm)	Width (μm)
A	0.46	1.04
B	0.8	1.04
C	0.46	4.54
D	0.8	4.54

STI, etching and masking are done. During these processes, a nonplanar intersection is formed between the silicon active region [n-well in Fig. 4(b)] and STI [5, 6]. For a short anode width, the effect of nonplanar intersection is significant, as indicated in Figure 4; therefore, this interrupts the current flow in both the anode and the cathode. This is referred to as the STI edge effect [7]. The STI edge effect, which depends on the isolation oxide structure and the slope of the trench isolation oxide, decreases the threshold voltage of a MOSFET; here, it reduces the R_s reduction of the array SBD. Overall, the reduction of R_s in an array structure is limited in both the length direction and the width direction.

3. FABRICATION AND MEASUREMENT

Micrograph of the fabricated chip is shown in Figure 5. Several patterns of CMOS SBD were fabricated in a 0.13 μm CMOS process. Figure 6 shows the top view and the cross-section of the fabricated CMOS SBD. The anode is formed in the n-well region and the cathode is formed in the n+ region. The anode and the cathode are separated by a polysilicon gate so that the series resistance can be minimized [1]. To confirm the analysis in Section 2, four SBD patterns with different anode widths (w) and lengths (l) are fabricated. In addition, each pattern is fabricated in the form of a one unit-size anode and a 2 × 1 unit-sized array anode. The anode width and length of each pattern are specified in Table 1 and Figure 6.

The S-parameters of the 0V-biased SBDs are measured in a one-port configuration with a vector network analyzer over the frequency range of 10–20 GHz. R_s and C_{j0} are extracted from the measured S_{11} value using (2), and the cut-off frequency is calculated using (1).

$$Z=\frac{1-S_{11}}{1+S_{11}}=R_s+\frac{1}{j\omega C_{j0}} \tag{2}$$

Calibration substrate and open dummy patterns are used in the calibration process. Table 2 shows the measurement results of R_s, C_{j0}, and f_T. As shown in Table 2, for the unit cell patterns, R_s is not inversely proportional to the anode size due to the edge effect. Series resistance of each patterns and reduction rates are indicated on Figure 7. For patterns A and B, which have a short anode width, the reduction of the series resistance between the unit cell and the 2 × 1 array is not proportional as expected. The series resistance reduction levels are only 19 and 23%, respectively. Conversely, for patterns C and D, which have relatively long anode widths, the series resistance reduction rates are 40 and 50%, respectively, as expected. For the case with the same anode width, the pattern which has the smaller anode length has a smaller reduction rate. All of the measurement results are well matched with the analysis in Section 2.

TABLE 2 Series Resistance (R_S), Junction Capacitance (C_{j0}), and Cut-Off Frequency (f_T) of Each Patterns

	Unit Cell			2 × 1 Array		
Pattern Type	R_s (Ω)	C_{j0} (fF)	f_T (GHz)	R_s (Ω)	C_{j0} (fF)	f_T (GHz)
A	199	3.1	256	161	53	183
B	181	4	214	138	7.4	154
C	124	9.1	139	74	17.8	120
D	92	13.8	124	46	26.9	126

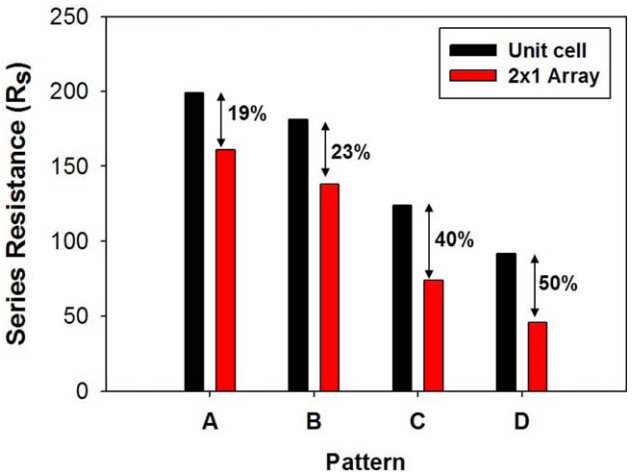

Figure 7 Series resistance of each patterns and reduction rate. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

4. CONCLUSION

The series resistance of a CMOS SBD as affected by the STI edge effect is analyzed. Due to the STI edge effect, the series resistance does not change proportionally according to the size of the anode and changes in the number of unit cells in the array SBD. To avoid this effect, the anode width of the SBD should be sufficiently long. This should be considered when the unit cell is connected in parallel. Otherwise, the SBD array structure will have higher series resistance than expected, causing the performance of the device to deteriorate.

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DEVELOPMENT OF ADAPTIVE STRUCTURES INCORPORATING MEMS DEVICES TO BE USED AS REFLECTARRAYS OR TRANSMITARRAYS

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ABSTRACT: *The concept of adaptive array antenna is presented, where the array can be switched between a reflectarray state and a transmitarray state. Several configurations are discussed including a basic geometry comprising of just a slotted ground plane with MEMS bridges over each slot and a slotted ground plane with square patches or rings on both sides of the ground plane. In the later cases, the slots on the ground plane need to be shorted when a reflectarray is desired; otherwise, the array will behave as a transmitarray. The detail unit cell study is discussed for each case for the performance of the array. Experimental study is presented to verify the concept.* © 2014 Wiley Periodicals, Inc. Microwave Opt Technol Lett 56:935–938, 2014; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.28217

Key words: *adaptive array; reflectarray; transmitarray; MEMS: Micro Electro-Mechanical System; PEC: Perfect Electric Conductor; PMC: Perfect Magnetic Conductor; MEMS-bridge; MEMS device*

1. INTRODUCTION

Reflect-array and transmit-array are examples of structures, which reflect and transmit electromagnetic waves, respectively. However, in many practical applications, one may require a structure to do both, but at different times. It is, therefore, worth to investigate the design of a structure that can be adaptively reflective or transparent. On the incidence of an electromagnetic wave on such a structure, if it reflects it will be visible; and if it transmits totally it will be transparent like a window. The proposed adaptive structure has to have a dynamic control mechanism to change its property from one state to the other. It can have many useful applications in science and engineering, such as in displays, detection technology, and imaging systems.

The concept of reflect-array is not new and was first proposed in 1963 using waveguide elements [1]. Other radiating elements can be dipoles or patches. The reflect-array became very popular at the advent of printed antennas because of low-reflecting surface profile, small mass, and low cost [2]. Using microelectronic techniques, thousands of printed patches can be etched on a dielectric substrate to form an array to mimic a parabolic reflector [3]. The feed antenna illuminates each element that are arranged to radiate the incident electromagnetic wave. By controlling the reflection phase of each element, the beam of the reflected energy can be controlled, which is its main advantage over the parabolic reflector antenna [4]. It also has the advantage over the phased-array in terms of not requiring a complex feed network having high insertion loss [2].

Conversely, the transmit-array acts like a lens and can be realized using patch arrays as well. An electromagnetic wave is received at one side of the surface, and the phase of each element is adjusted to retransmit it from the other side [5–9]. The objective of this work is to obtain an array, which can be made to transmit the electromagnetic energy when needed, therefore, making it a transparent surface, or reflect the energy thus making it a reflective surface.

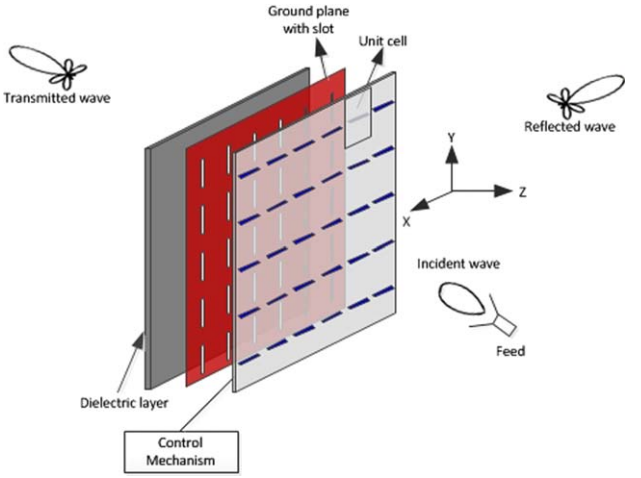

Figure 1 General concept of the adaptive array consisting of slotted ground plane along with the control mechanism for switching between reflectarray and tranmitarray states. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

The design of a reflectarray is straight-forward and consists of a ground plane and some radiating elements. The ground plane works as a screen to completely reflect any incident ray on the array, whereas the radiating elements provide only the necessary phase compensation for the incident ray [5]. Conversely, the transmitarray comprises of radiating elements either without any ground plane [10], or a ground plane with apertures and the radiating elements on both sides of it [11]. In the latter case, while the radiating element provides both transmission and phase compensation, the slotted ground plane behaves as a frequency selective surface (FSS) to ensure the transmission of the energy. Therefore, when both transmitarray and reflectarray operations are intended from the same structure, it is imperative to have a ground plane with apertures in the system, as shown in Figure 1, which can be blocked by the control mechanism, so that it can operate as a reflectarray. Moreover, additional ground conductor or dielectric layers may be needed for the control mechanism, which is the key component in this study. As aforementioned, the ground plane in this adaptive structure is like an FSS, the mechanisms to tune FSS can be employed here to change its states between reflectarray and transmitarray. Some tuning techniques available in the literature are: the use of on-unit-cell active-control devices, advanced substrate materials, ferrites, MEMS devices, and so forth [12–19]. Of particular interest, are the MEMS devices because of their reduced size, mass and cost, and advancement in the fabrication process. In this letter, a few antenna configurations are discussed which can be potentially used as both transmitarrays and reflectarrays, with the possibility of using MEMS-based control mechanism suitable for achieving the adaptability.

The article is organized in the following sections: in Section 2, the simplest possible configuration as an adaptive surface is discussed, where a MEMS bridge is used to change the state of the surface. To have more design freedom and control, more configurations based on patches and rings are presented in Section 3,