A High Performance CMOS Direct Down Conversion Mixer For UWB System

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ABSTRACT
This paper represents a high performance wideband CMOS direct down-conversion mixer for UWB based on 0.18 µm CMOS technology. The proposed mixer uses the current bleeding technique and an extra resonant inductor to improve the conversion gain, noise figure (NF) and linearity. Also, with an extra inductor and the careful choosing of transistor sizes, the mixer has a very low flicker noise. The shunt resistor matching is applied to have a 528MHz bandwidth matching at 50 Ohm. The simulation results show the voltage conversion gain of 20.5 dB, the double-side band NF of 5.6 dB. Two-tone test result indicates 11.25 dBm of IIP3 and higher than 70 dBm of IIP2. The circuit operates at the supply voltage of 1.8 V, and dissipates 11.5 mW.

Categories and Subject Descriptors
B.7.1 VLSI (*very large scale integration)*

General Terms
Design.

Keywords
Mixer, Direct down conversion mixer, Flicker noise, UWB

1. INTRODUCTION
Ultra Wideband (UWB) system adopted by FCC has emerged as an attractive future technology for wireless communications and local area networks. This is a short range, low power, high data rate and wide band wireless system [1]. With the bandwidth of 528 MHz and other characteristics, UWB transceivers have to meet the stringent requirements of 802.15.3a standard [2]. Our research group approach for UWB transceivers is to use the dual conversion architecture [3].

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The direct down conversion mixer in this architecture was designed, the center operating frequency is chosen at 1.32 GHz for image reduction. The mixer translates the RF signal at the frequency band from 1.056 GHz-1.584 GHz to the base band signal.

In a receiver system, the down-conversion mixer is the key building block since it dominates the system linearity, noise figure, and determines the performance requirements of its adjacent blocks.

Among many proposed active mixers, the Gilbert-cell mixer has been widely used so far, and the double-balanced mixer topology has been preferred since it can suppress (LO) leakage signals at the output (Fig. 1). The down-conversion mixer is required to provide a high linearity, low noise figure, and enough power conversion gain. The simultaneous achievement on these requirements is a very challenging task in the mixer design. Especially, the high linearity requirement is the most difficult one to achieve since the mixer is required to operate at a very low supply voltage and low power consumption.

Higher gain and better linearity can be achieved by increasing the bias current through the transconductance stage [4], but the power consumption can be excessive. Better techniques to improve conversion gain have been introduced, where some sort of current bleeding techniques are utilized [5,6].

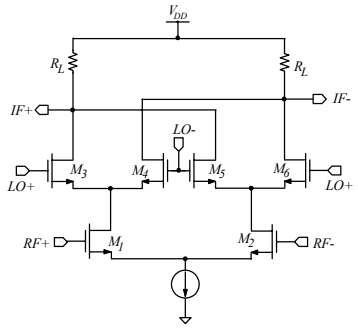

Figure. 1. Double-balanced Gilbert-type mixer topology

Besides, 1/f noise is also one of the critical issues in the direct down conversion mixer. We have found that, in the mixer the switching transistors primarily determine the flicker noise performance. There are two dominant mechanisms that the flicker noise of the switching transistors appears at the mixer output, they are direct and indirect mechanisms [7]. In the indirect mechanism, output flicker noise depends on the frequency and circuit capaPcitance at the common source node of the switching stage.

Our approach is to reduce this capacitance by adding an extra inductor that helps to reduce 1/f noise and improve the linearity.

In this paper, a novel down conversion mixer design technique applied in DCR for UWB is introduced. The conversion gain is improved by applying the current-reuse bleeding technique in [6]. A critical improvement in linearity and very low 1/f noise can be achieved by using an extra inductor. The proposed direct-converted mixer achieves a very good performance with the voltage conversion gain of 20.5 dB, double-side band NF of 5.6 dB, IIP3 of 11.5 dBm, and IIP2 is higher than 70 dBm. The proposed mixer is implemented based on 0.18 μm CMOS technology under a supply voltage of 1.8V supply, and dissipates dc current of 6.4 m A.

2. PROPOSED MIXER TOPOLOGY AND DESIGNS

The double-balanced Gilbert-type mixer topology shown in Fig. 1 is preferred in CMOS mixer design since it suppresses the LO signal and the even order distortion products at the output.

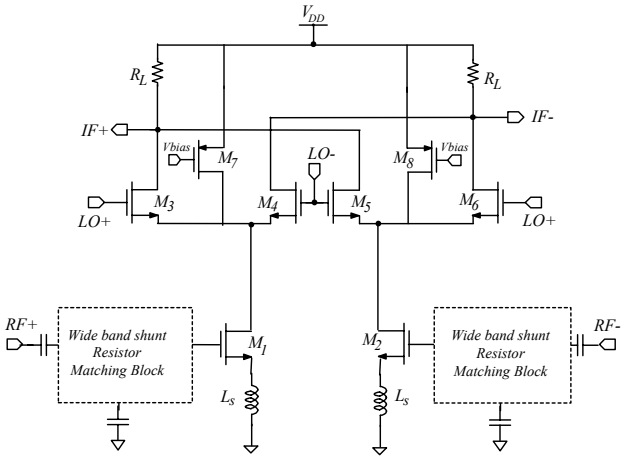

Figure. 2. Double-balanced Gilbert-type mixer with current-reuse bleeding technique

In overall mixer design, higher gain, higher linearity, lower noise and low power consumption are required. However, these parameters are not easy to achieve simultaneously. Higher gain and better linearity can be achieved by increasing the drive current through the transconductance stage [4], but power consumption will be increased. Furthermore the larger current through the switching quads causes voltage headroom problems especially if resistive loads are used. The larger amount of current through the switching quads mandates the larger LO drive voltage, which is troublesome in the CMOS technology, since it is not easy to get the large enough voltage swing at high LO frequency.

Voltage gain equation:

$$G_v = \frac{2}{\pi}.g_m.R_L \qquad (1)$$

where g_m is the transconductance, R_L is the load resistor.

From (1), conversion gain is increased with higher load resistors, but the supply voltage is kept constant. That can be realized by using bleeding technique. In this design, PMOS transistors M7 and M8 create the bleeding currents under the gate bias voltage as shown in Fig. 2.

With the bleeding technique, the current through switching transistor is reduced, such that the 1/f noise is improved and the output load resistance is increased leading to a higher gain [6]. Also, the bias current through the transconductance stage can be increased without increasing the current through the switching transistors. The bleeding technique relaxes the voltage headroom problem, and allows smaller LO drive voltage applied to the switching transistors for switching efficiency.

However, the mixer topology shown in Fig. 2 has some drawbacks due to the parasitic capacitance at the drain nodes of the transistors pair M1-M7 and M2-M8. Those parasitic capacitances lead to the reduction of the transconductance and cause the flicker noise such that the conversion gain and NF of mixer are degraded. This paper proposes a technique that can be used as the solution to overcome the drawback caused by those parasitic capacitances. This issue can be seen more clearly by using the simplified single balance mixer in Fig. 3.

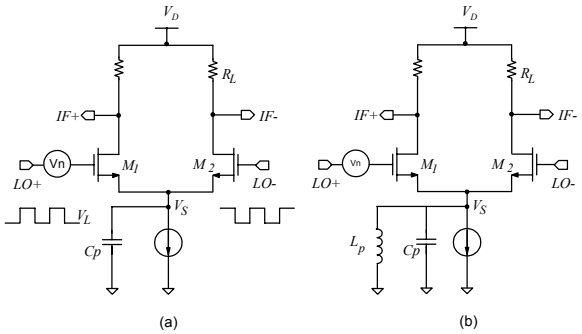

Figure. 3. Indirect mechanism for 1/f noise

As mentioned above, in indirect mechanism, output flicker noise depends on the capacitance at the common source node of the switching stage C_p. The tail voltage (V_s) wave forms charge exponentially to V_n in half cycle and discharge to zero in the other half cycle. This voltage produces the current through C_p. So the output current alternates at twice the LO frequency with non-zero DC value, it means the base band flicker noise appears at the mixer output [7]. $i_{o,n}$ is presented as follows:

$$i_{o,n} = \frac{2}{T}.C_p.V_n.\frac{(C_p w_{LO})^2}{(g_{ms})^2 + (C_p w_{LO})^2} \qquad (2)$$

Where g_{ms} is the transconductance of switching transistors and w_{LO} is the LO frequency. In order to reduce flicker noise we have to reduce C_p. In Fig. 3, Lp is added in parallel with C_p, by resonating, C_p is suppressed. The proposed mixer topology is shown in Fig. 4. In this topology, the inductor L1 is added, the value of L1 is twice the value of Lp. L1 actually consists of two Lp in series, the middle point of L1 is the virtual ground. With the same mechanism, L1 resonates with input capacitors of the switching stage (C_p) such that the overall transconductance is

not degraded. By parallel resonating with the capacitor C_p at LO frequency, C_p is reduced as well as the effects of current through it. The voltage swing at node X (V_s) will be reduced when L1 is used. The flicker noise caused by this effect is suppressed. Under resonant conditions, the conversion gain and NF of the mixer are improved.

L1 is an off chip inductor, it is connected to the circuit by the pads and bonding wires. Considering the parasitic capacitances of these the pads and the inductances of the bonding wires, the value of L1 is 10nH.

Furthermore, with the presence of L1, the impedance at twice the signal frequency is lower, in other words the current components at the high order harmonic frequencies and intermodulation products running through node X are suppressed, so IIP3 is improved.

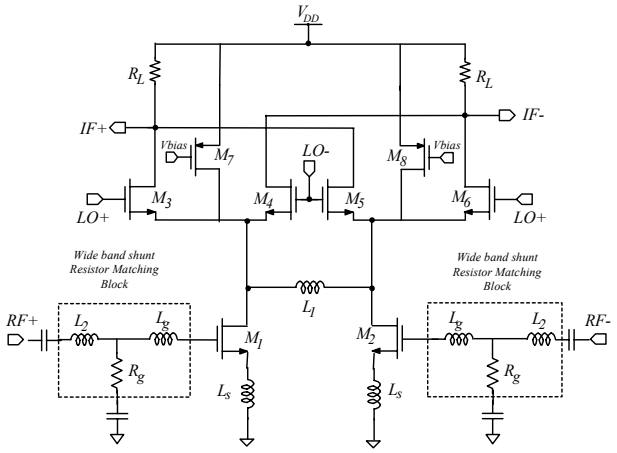

Figure. 4. The proposed down-conversion mixer topology

The resistive load is used because it is free of flicker noise. To restrict the power consumption, the size and V_{gs} of transistor M1 and M2 are chosen carefully. But if V_{gs} is too low, the gain and linearity will be degraded. For switching transistors, the width needs to be large to reduce 1/f noise [7].

Also, the gates of switching transistors are biased near threshold in order to minimize the switching time, this factor permits the reduction of LO power and makes the switching more ideal. Non-ideal switching, such as when the switch is not completely turn on and off, will reduce the conversion gain and increase the noise figure [4, 5].

For the measurements, the input of mixer is required to have the impedance matching at 50 Ohm at a band width of 528 MHz. Since the operating frequency is low compared to the bandwidth, the shunt resistor is the best input matching method. According to the theory, this method will lose 3dB of gain and noise. However, by adding L1, the proposed mixer has very good performances compared to previously reported designs in terms of linearity, noise figure and gain, shown in Table. 1. The matching block is off-chip, the source degeneration Ls helps to increase the gain which is degraded by R_g. Ls combining with the matching block is for input matching. This inductor is the bonding wire, it helps decrease the noise figure and increase the third order input intercept point (IIP3) [4].

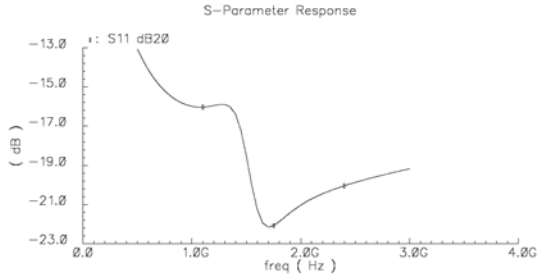

Figure. 5. Input matching characteristics, S11.

S11 is less than –16 dB, 50 Ohm input matching at 528 MHz bandwidth, shown in Fig. 5.

The LO to RF isolation is 57.3 dB, this isolation helps to reduce the DC offset in the down mixer. The LO to IF port isolation is 115 dB, the high isolation is to prevent the saturation of signal at output stage that degrades P1dB.

3. SIMULATION RESULTS AND DISCUSSION

The proposed mixer in Fig. 4 is simulated in a TSMC 0.18 μm CMOS process by Cadence. The results are shown below.

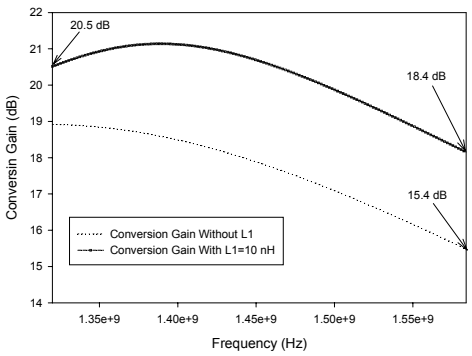

Figure. 6. Conversion Gain

In Fig. 6, the simulation shows the conversion gain increases by 3 dB when L1 is added in the circuit, 20.5 dB at center frequency band. In the circuit, L1 is an off chip inductor with the optimum value of 10 nH.

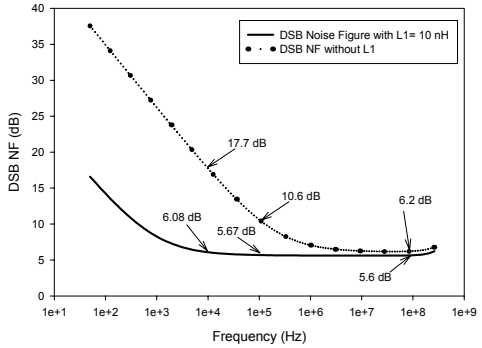

Figure. 7. DSB Noise Figure

The flicker noise is very low, at the frequency of 10 kHz the noise is only 6.08 dB, the corner frequency is reduced from more than 100 kHz to a less than 10 kHz. With an extra inductor L1, the overall thermal noise or NF is improved by 0.6 dB, DSB NF simulated at 100 MHz is 5.6 dB. The flicker noise at 10 kHz is improved by 11.62 dB, at 100 kHz is by 4.97 dB and much more near DC, about 20 dB. DSB NF simulation is shown in Fig. 7.

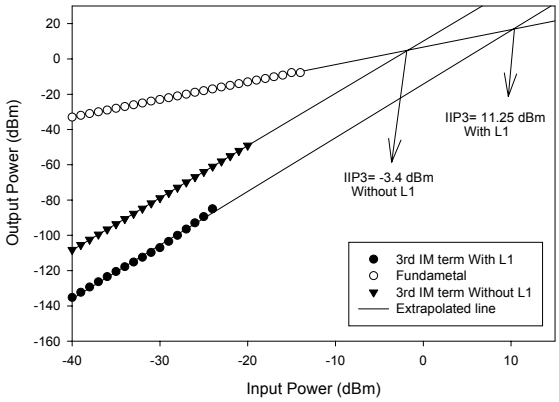

Figure. 8. Third Order Intercept Point, IIP3.

From the Fig.8, the IIP3 shows a very impressive value of 11.25dBm, improved by 14.6 dB, among the highest results for the Gilbert-based topology mixers. This significant improvement is due to an extra inductor L1.

In Table.1, important parameters like linearity, conversion gain and NF of the proposed mixer are compared with those in [4,5], [8]-[11]. The table shows that the performance is much better than previous works however power consumption is still at a reasonable level.

Table. 1. Performance Comparison

Parameters	This Work	[4]	[5]	[8]	[9]	[10]	[11]
Frequency (GHz)	***1.32***	2.45	2	0.435	2	5.8	1.8
Supply Voltage (V)	***1.8***	1.8	1.8	2.5	-	1.5	2.2
Power Consumption (mW)	***11.5***	-	12.06	5.4	5 mA	6.89	10.34
(1) Input IP3 (dBm)	***11.25***	-3.7	10	-13.4	-2.5	-2.94	6.7
(2) Voltage Conversion Gain (dB)	***20.5***	27	14	20.8	7.2	7	10.6
(3) DSB NF (dB)	***5.6***	12.5 (SSB)	9.5	9.2	9.15	14.3 (SSB)	10.3
(1) + (2) - (3)	***26.15***	13.8	13.5	-1.8	-4.45	-7.24	7

From the above table, the designed down conversion mixer has an outstanding performance, especially the IIP3 value, compared to other previously reported designs.

4. CONCLUSION

This paper introduces a new downconversion mixer topology and compared its performance to those of previously published papers. The proposed mixer topology, designed and manufactured in 0.18 μm CMOS process, shows an excellent performance. It is suitable for UWB systems as well as direct conversion architecture since it provides high linearity, low 1/f noise and high conversion gain. To achieve higher conversion gain, the bleeding technique is applied. Linearity is increased critically and 1/f noise is lowered by using an extra inductor. This inductor helps the proposed mixer overcome with the parasitic capacitance at the source terminal of the switching stage such that the conversion gain and NF are improved furthermore.

At this moment only simulation data is available, but simulated performance is good enough to allow successful receiver designs. Also, some simulated parameters, like NF and IIP3 are better than reported papers. Predicted mixer's DSB NF as low as 5.6 dB and IIP3 of 11.25 dB is particularly interesting. The newly proposed mixer can be utilized in a variety of applications other than UWB system.

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