A Linear 10-bit DAC for LCD Drivers ICs using Charge Subtraction Interpolation

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ABSTRACT
A linear 10-bit digital-to-analog converter (DAC) has been designed for LCD driver ICs. The proposed architecture suggests the charge subtraction interpolation technique based on the 2-bit sub-DACs and a switched-capacitor adder. Therefore, the size of DAC will be decreased around half. The DNL and INL simulation results are smaller than 0.04LSB. The DAC has been designed for 0.18-μm 3.3V CMOS technology.

1. Introduction
Nowadays, TFT-LCDs are widely used from mobile to large size displays. The DAC size of small display is not a big problem, because it has low resolution. Normally, the driver ICs DAC used the resistor string cell, however, an increase of the bit depth results in an exponential increase of the DAC area [1]. Therefore, many use the interpolation technique to reduce the size. There are so many works published about interpolation of DAC [1]-[4]. Among works, the capacitor DAC with SC adder type is more efficient way to reduce the size [5]. Even though, the capacitor DAC use the capacitor, the switch size will be decreased dramatically, therefore, it has big advantage in the size issue. The proposed architecture is reduced the DAC size of dominant component in driver ICs by adopting the new concept. The charge subtraction method is based on the C-DAC, however, one more interpolation is possible by adopting charge subtraction method. We add one more interpolation to each capacitor and decoder, therefore, the decoder size will be reduced by half.

2. Proposed DAC Architecture
Figure 1 shows the previous presented DAC architecture, which consists of resistor string for global, decoder for interpolation and an SC adder. The DAC is divided three kinds of interpolation blocks such as two 4-to-16 decoders and a 2-to-4 decoder with three capacitors in the normal ways. The SC adder type interpolation DAC used two clocks, during phase 1, the each voltage charges the each capacitor (C₁, C₂ and C₃) after that we collect the charge in each capacitor to one capacitor (C₄) during phase 2. We can add the one more interpolation technique by adopting charge subtraction based on this interpolation. The proposed architecture is shown in figure 2. The basic operation is same with normal interpolation technique; however the difference is that the charge subtraction method is adopted in the phase 2. By adopting the charge subtraction method, the 4-to-16 decoder is possible divided to two 2-to-4 decoders. Therefore, the number of transistors used in the decoder is decreased from 36 to 20, the size of decoder is reduced by half in each cell by using charge subtraction method. The normal transistor size for switch cell is 4.8um² in low voltage. The size comparisons are shown in table I.

In the SC adder interpolation type, the DAC used two different phases. Each interpolation voltage charges in each capacitor during phase 1. The difference is occurred in phase 2. Normally, the whole charge in each capacitor is transferred to one capacitor (C₁), the proposed method doesn’t transferred whole charges. The second interpolation voltages (V₅ and V₁) are applied in the capacitors (C₂, C₃). Therefore, the capacitors C₂ and C₃ have charges during phase 2. The subtraction charges are transferred to the capacitor C₁ during phase2, the one more interpolation is possible using same architecture.

This mechanism is proved by equations. The whole charges are same in capacitors between phase 1 and 2. Therefore, the output voltage is derived by charge conservation principle. The offset voltage of the buffer also considered in below equations.

During Φ₁ phase:

\[ Q₁ = C₁(V₅ - V₄ - V₃ₖₐₜₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅ₖₐₚ₅₆
V_5 = \frac{V_{DD}}{2^2} D_1 \\
V_4 = \frac{V_{DD}}{2^3} D_2 \\
V_3 = \frac{V_{DD}}{2^4} D_3 \\
V_4 = \frac{V_{DD}}{2^5} D_4 \\
V_5 = \frac{V_{DD}}{2^6} D_5 \tag{5}

Therefore, the final equation is given by

V_{OUT} = \frac{V_{DD}}{2^2} D_1 + \left( \frac{V_{DD}}{2^3} - \frac{V_{DD}}{2^5} D_2 \right) + \left( \frac{V_{DD}}{2^4} D_3 - \frac{V_{DD}}{2^6} D_4 \right) \tag{6}

This means that all kinds of voltage will be expressed by the charge subtraction method with removing the offset voltage.

Now, the digital codes for interpolation will be recalculated, however we don’t need to consider the whole digital codes, because the codes are repeated in the lowest 4 level decoders. If the two levels of decoder are calculated, the remaining part is just same with this. The value is consisted of 0 to 15 in 4 bit decoder, however, The 4 bit decoder is divided to 2 bit decoder to adopt charge subtraction interpolation. If we assume that 10 value is needed in the charge summation, we first charge 8 and 2 value of each capacitor during phase 1, after the charges are combined from two capacitor to one capacitor during phase 2. However, it is different in the charge subtraction, 12 value of voltage will be charged during phase 1, and after 2 value is subtracted during phase 2 in the capacitor. Figure 3 shows the digital codes and example of upper case.

3. Circuit Implementation and Simulation Results

The linear 10bit interpolation DAC for LCD driver is designed using 0.18 µm, 3.3V CMOS technology. The digital ramp signal for the column driver simulation has been inserted with full code from 0000000000 to 1111111111.

The positive and negative buffers are designed by class AB opamp for DAC. The low-frequency gain of the opamp is around 70dB to achieve the 10-bit resolution. Each buffer consumes 6 µA static current and no slew enhancement technique is needed.

The proposed linear 10-bit DAC was simulated with spectre. Figure 4 shows the DNL and INL simulation of the proposed DAC. The maximum DNL and INL are around 0.04 LSB, respectively. The error may be due to the finite gain-bandwidth of the opamp and parasitic capacitor in the switch. In spite of this, the proposed DAC shows better linearity in comparison with others. Figure 5 shows the transfer curves. The table 2 summarize the whole performance of proposed DAC.

4. Conclusion

The new interpolation method is presented to reduce the DAC size. If we use this method in the capacitor DAC, we reduce the number of switches in decoder by half. The proposed DAC also shows better linearity performance. The features of linearity and settling time show that the proposed column driver is suitable for LCD applications.

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REFERENCES

Fig. 2 Proposed DAC Architecture

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<td>1 2 3 4 5</td>
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Wanted Value | MSB Code | LSB Code |
-------------|----------|----------|
0 1 2 3      | 0 0 0 0  | 0        |
4 5 6 7      | 1 1 1 1  | 1        |
8 9 10 11    | 0 1 2 3  | 3        |
12 13 14 15  | 3 3 3 3  | 3        |

Fig. 3 Charge subtraction digital code (a) summation case, (b) subtraction case

Fig. 4 Simulated DNL and INL
Fig. 5 Transfer curves for the positive and negative polarities